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Dkt No. 1744.0920001; Group Unit: 2634
Inventors: SORRELLS et al.
Tel. No.: 202-371-2600
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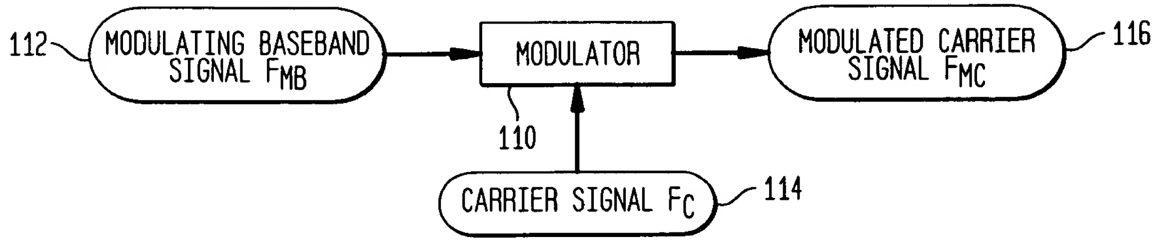
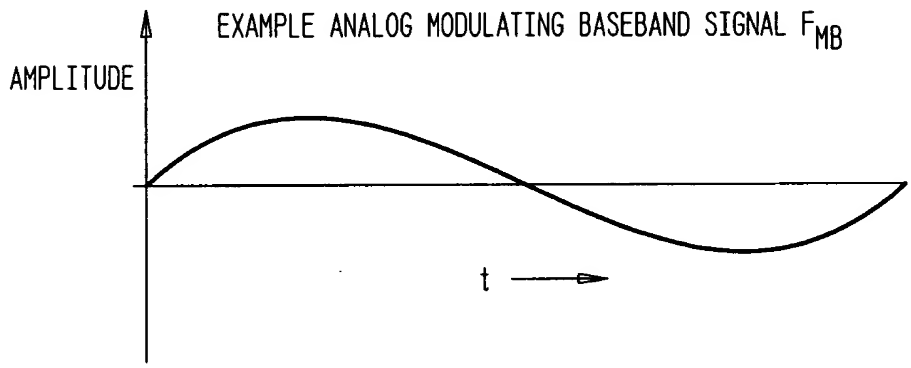
FIG. 1



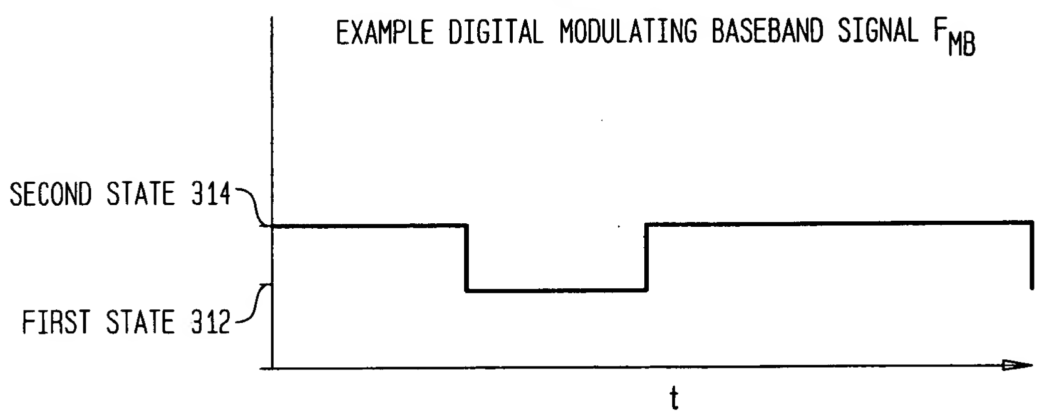
210

FIG. 2



310

FIG. 3



CARRIER SIGNAL
(e.g. 900 MHz)
410

FIG. 4

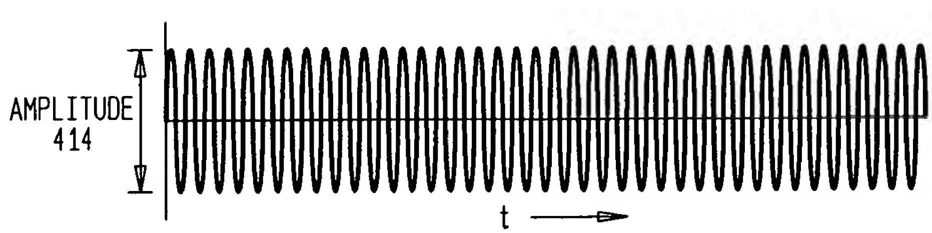


FIG. 5A

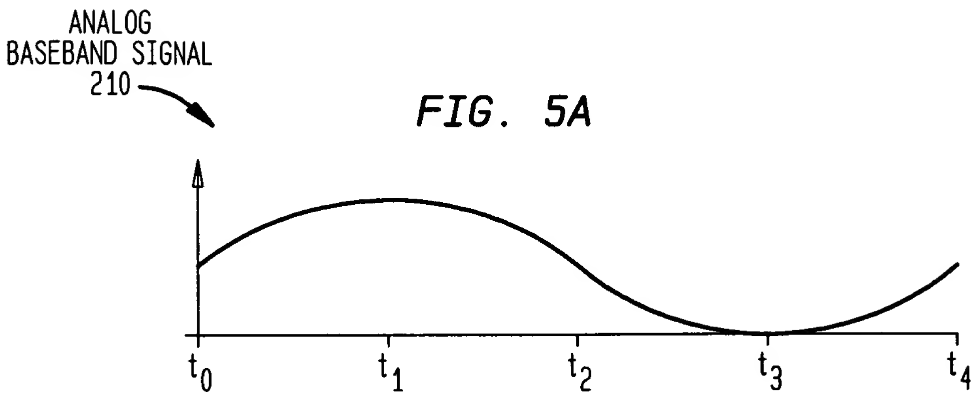


FIG. 5B

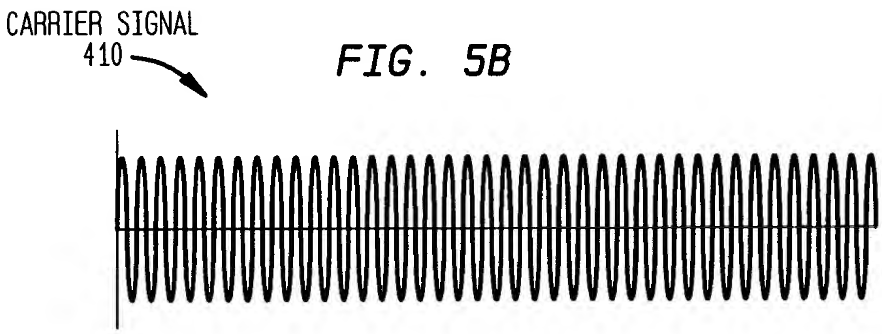


FIG. 5C

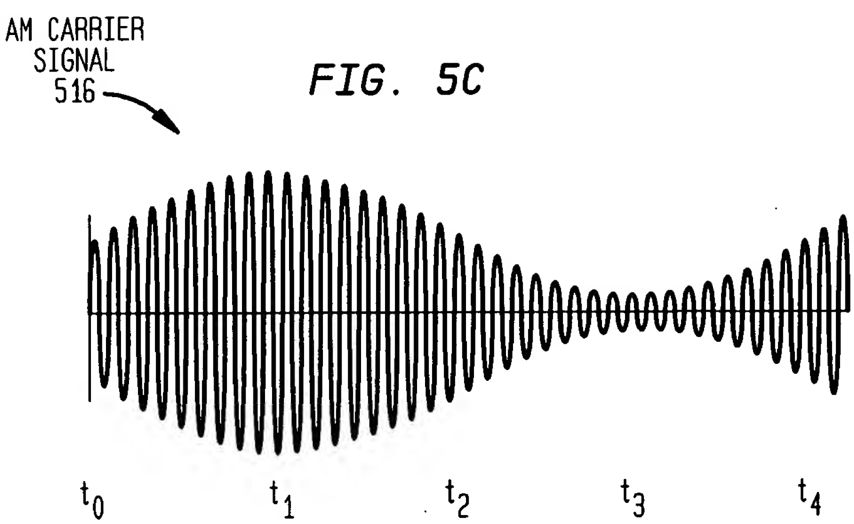


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FIG. 6A

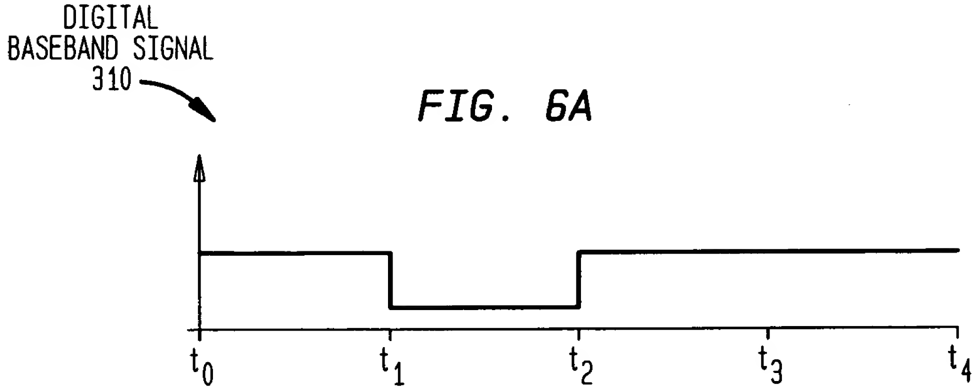


FIG. 6B

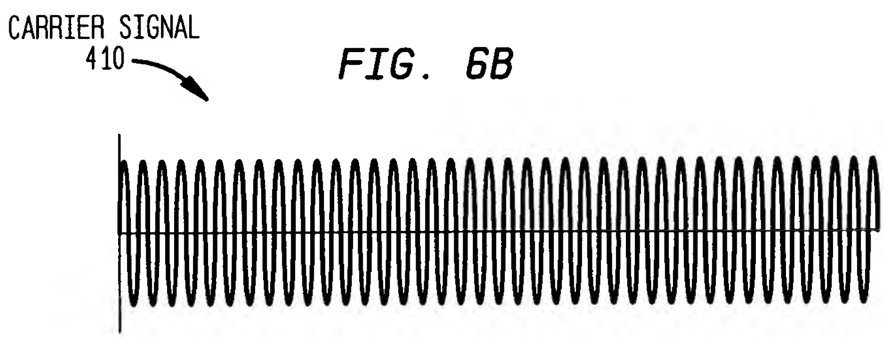


FIG. 6C

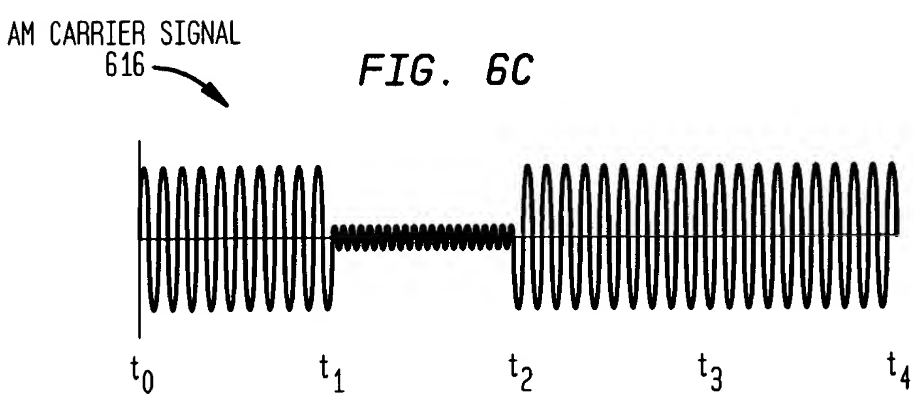


FIG. 7A

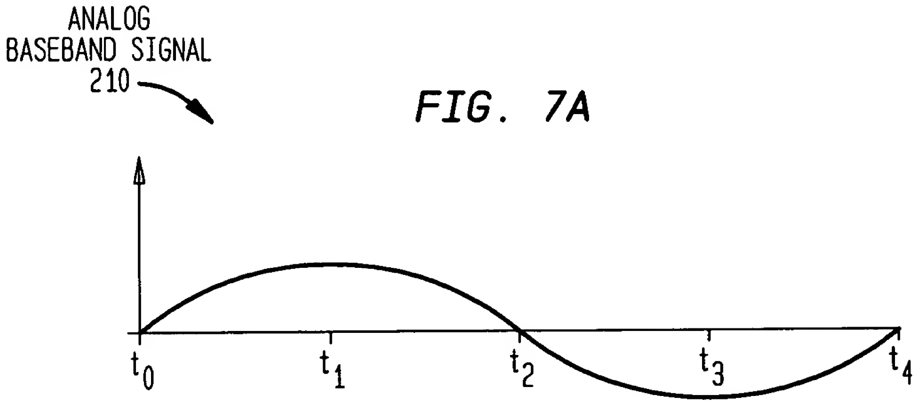


FIG. 7B

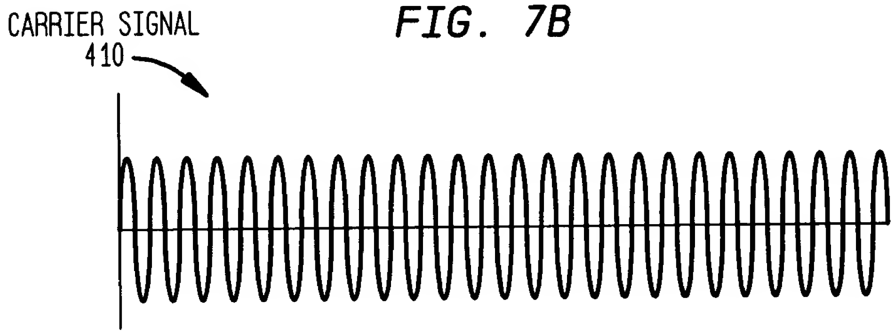
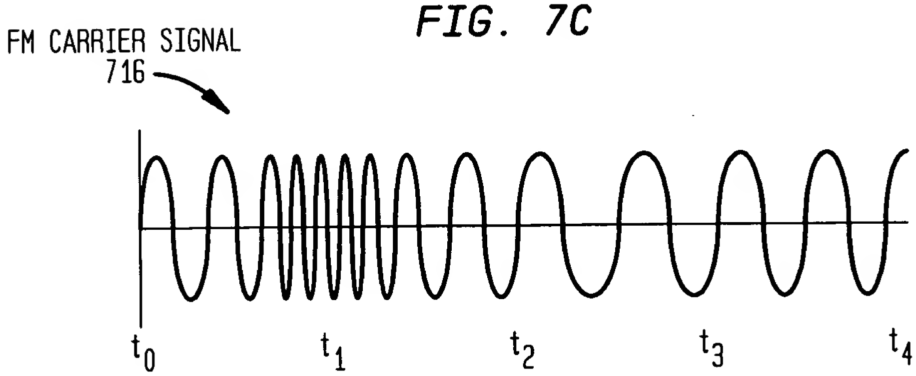


FIG. 7C



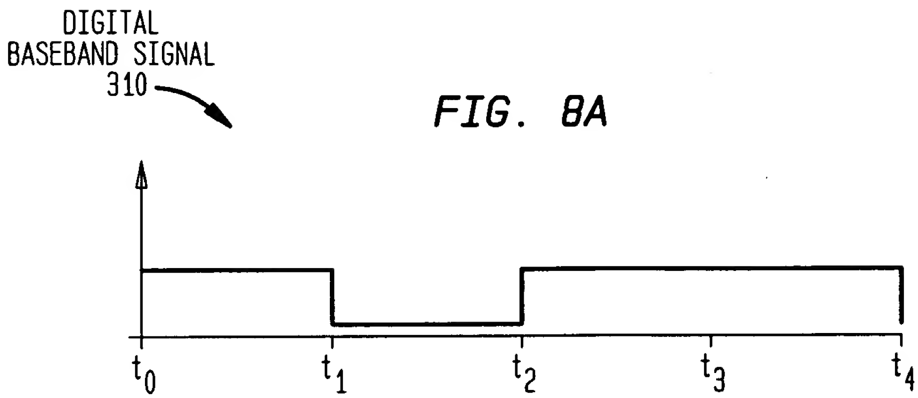


FIG. 8A

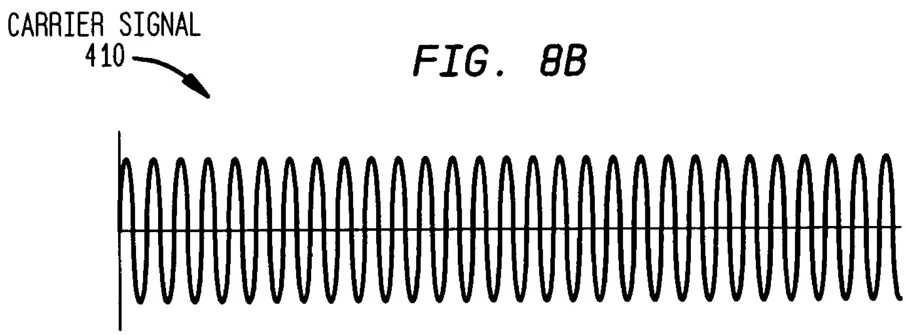


FIG. 8B

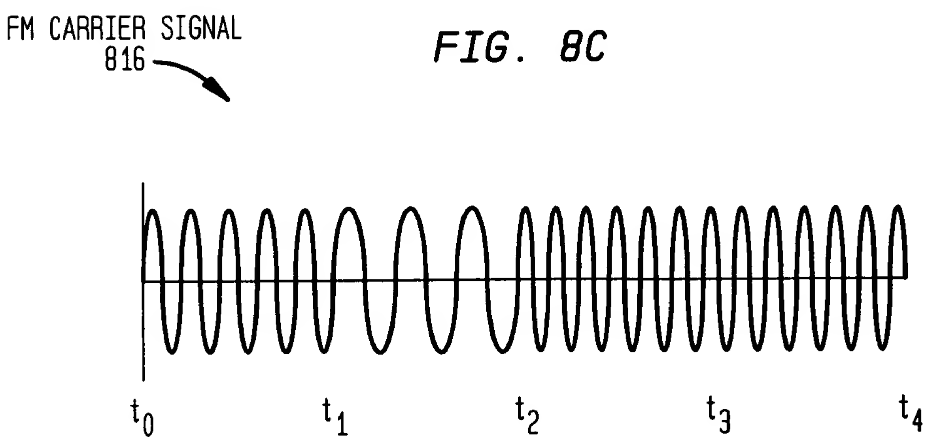


FIG. 8C

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FIG. 9A

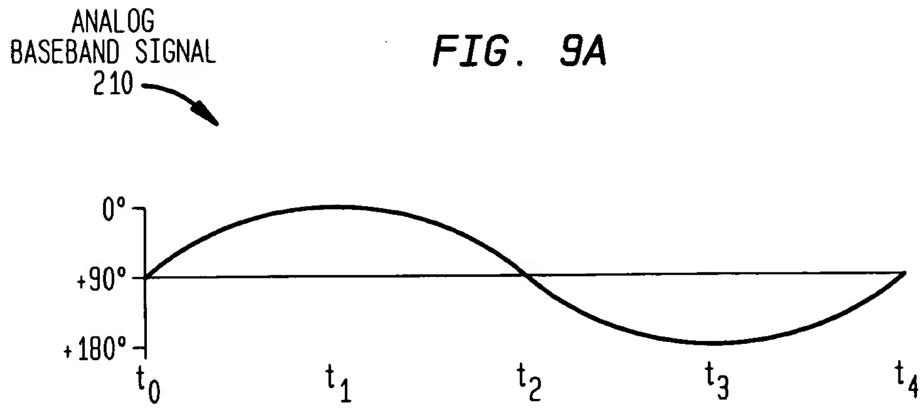


FIG. 9B

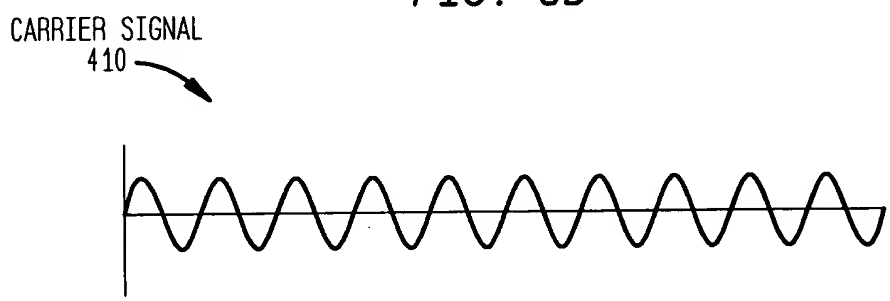


FIG. 9C

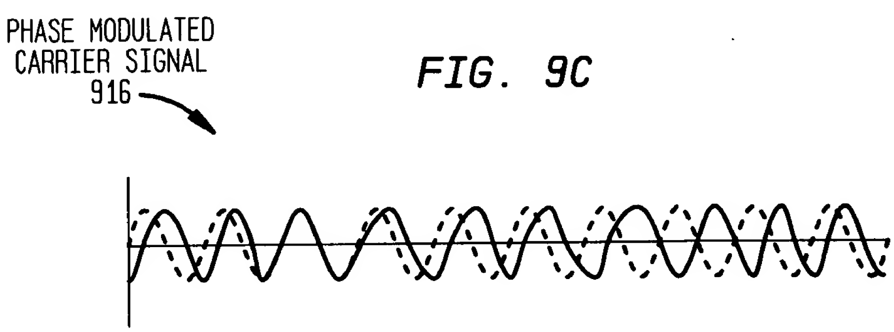


FIG. 10A

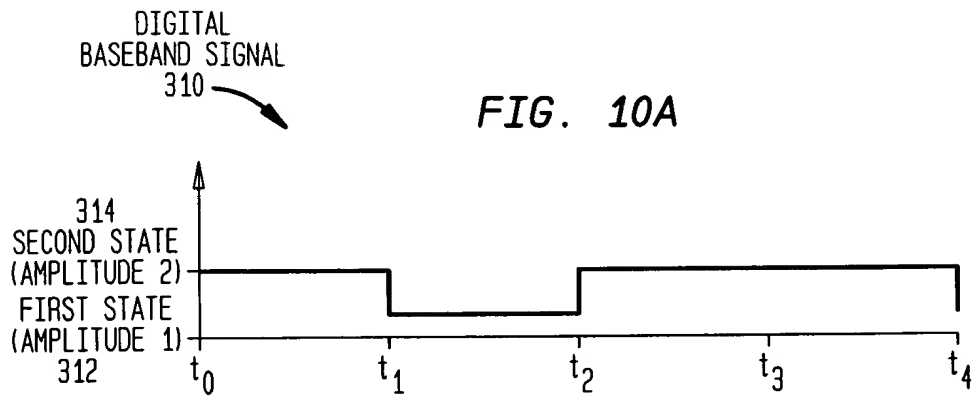


FIG. 10B

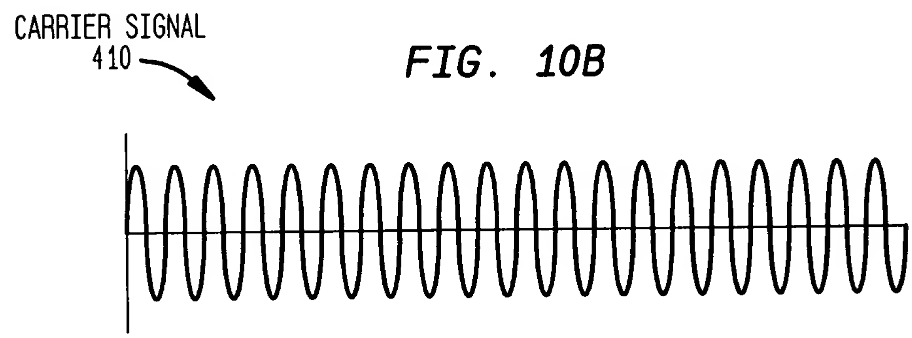
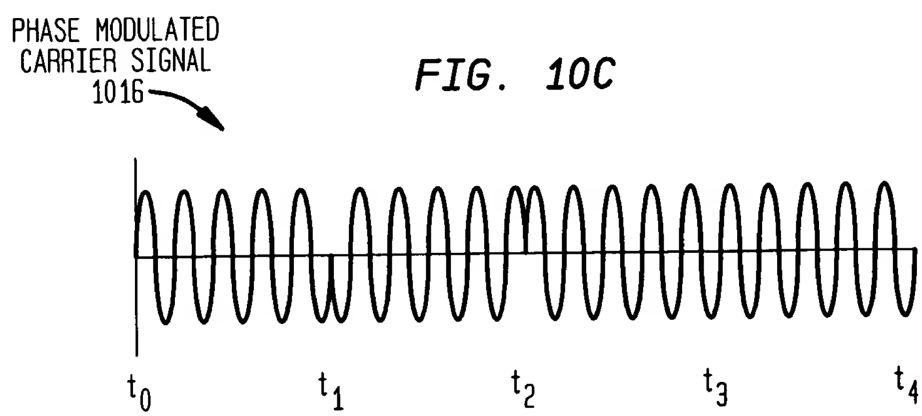


FIG. 10C



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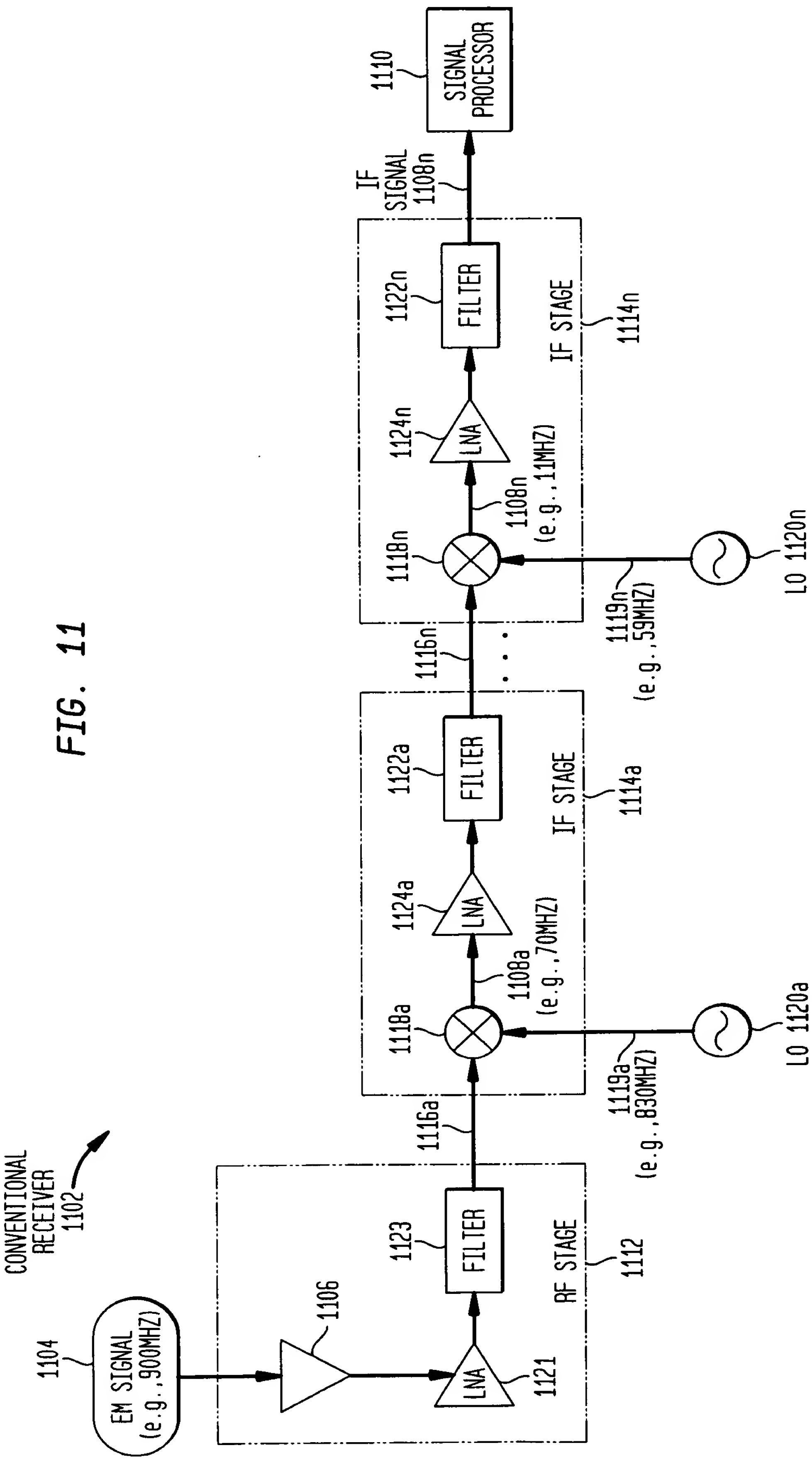
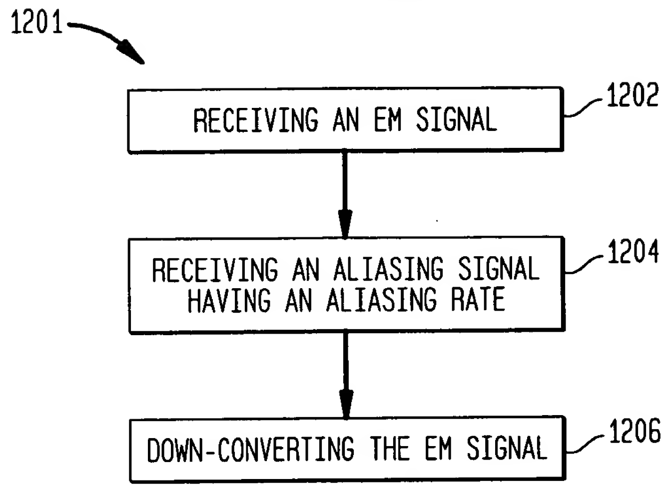


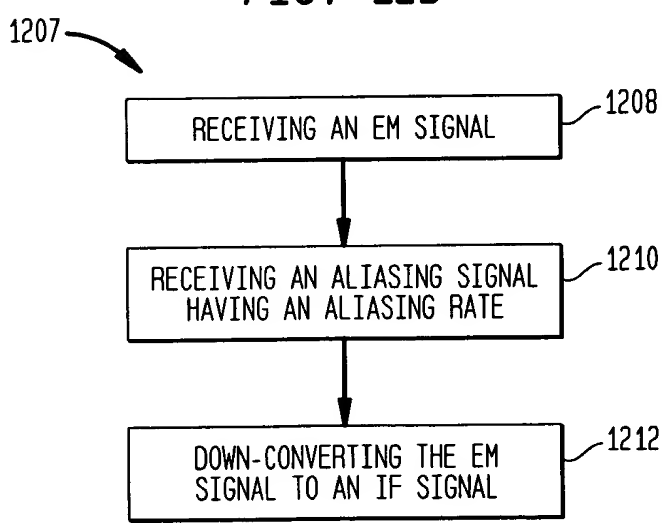
FIG. 11

FIG. 12A



GENERIC DOWN-CONVERTING FLOWCHART

FIG. 12B



DOWN-CONVERTING AN EM SIGNAL TO AN IF SIGNAL

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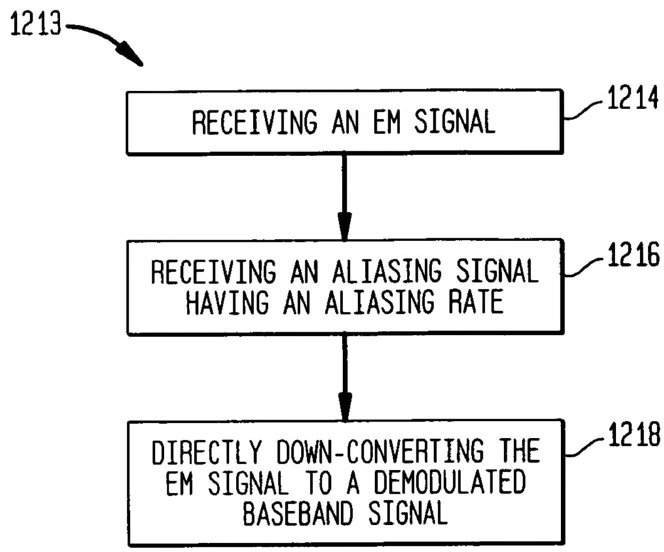
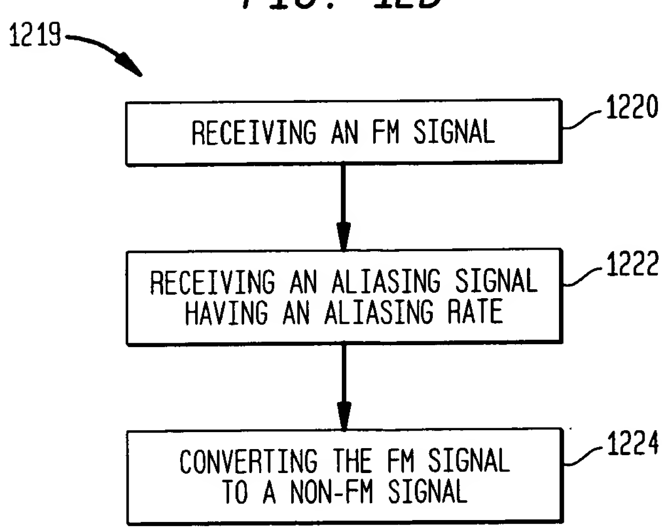
FIG. 12C



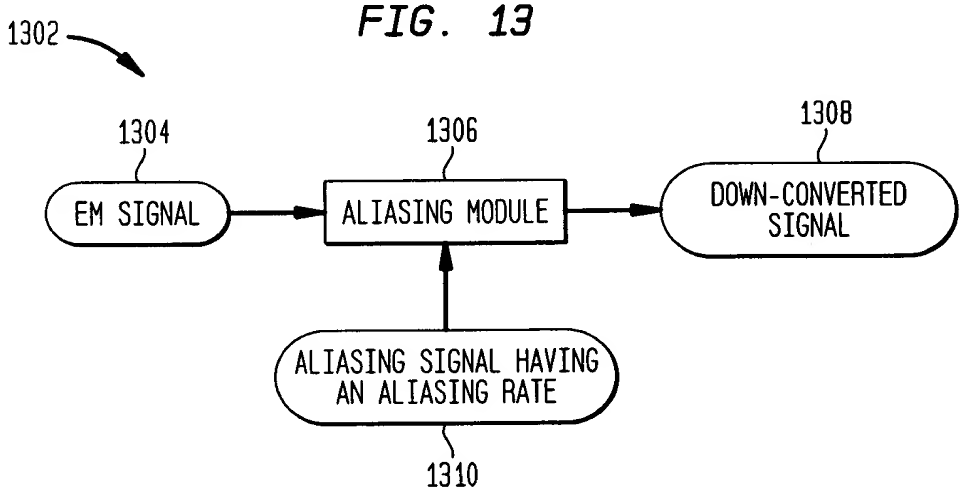
DIRECTLY DOWN-CONVERTING AN EM SIGNAL TO A DEMODULATED BASEBAND SIGNAL

FIG. 12D



MODULATION CONVERSION

FIG. 13



GENERIC DOWN-CONVERTING SYSTEM

FIG. 14A

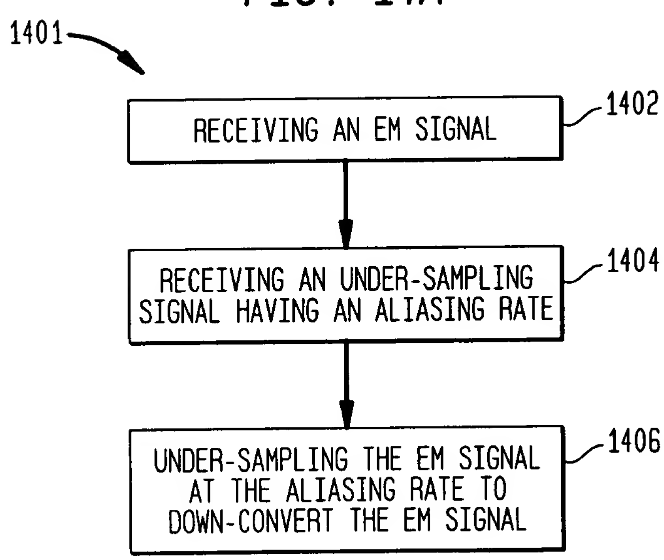


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FIG. 14B

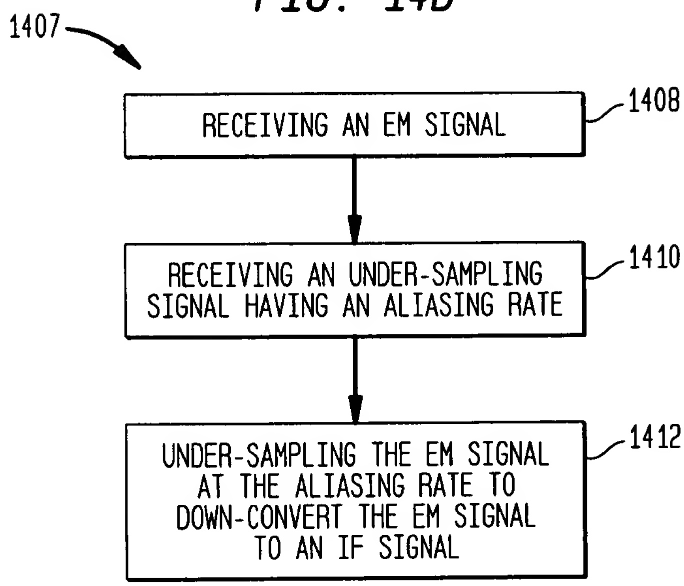

FIG. 14C

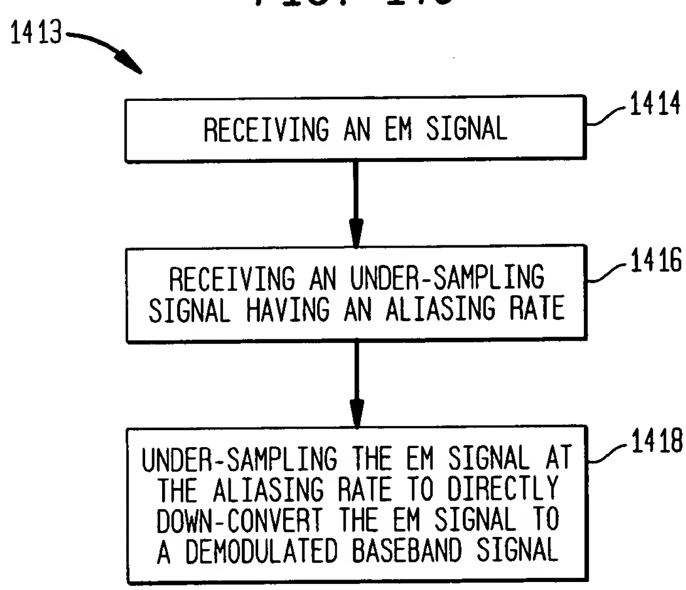

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FIG. 14D

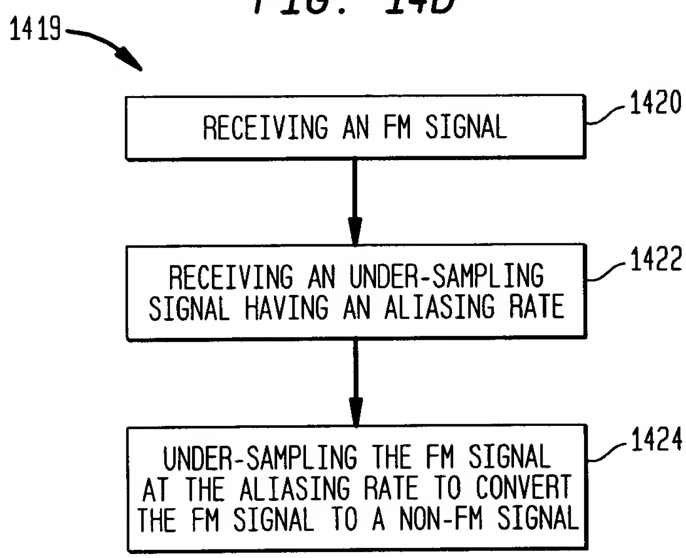

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FIG. 15E

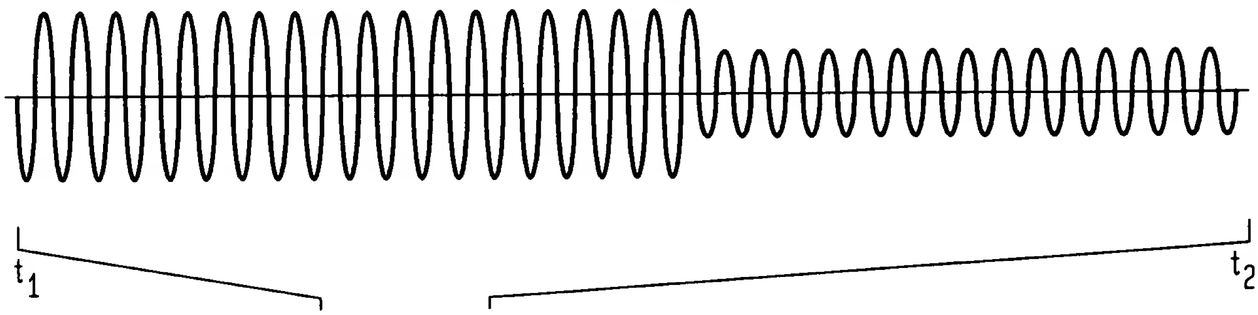

FIG. 15A

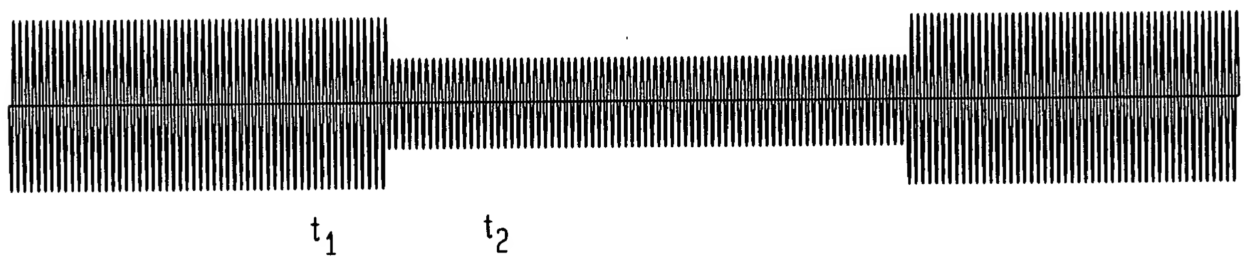

FIG. 15B

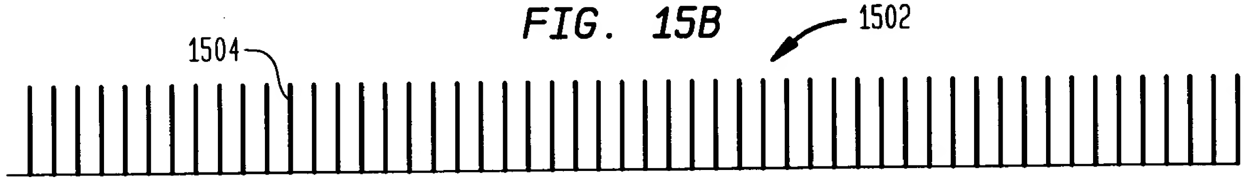

FIG. 15C

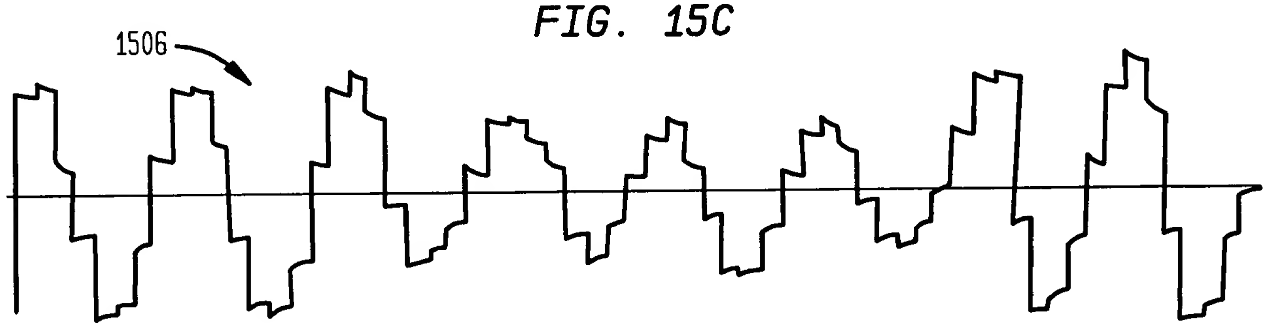

FIG. 15D

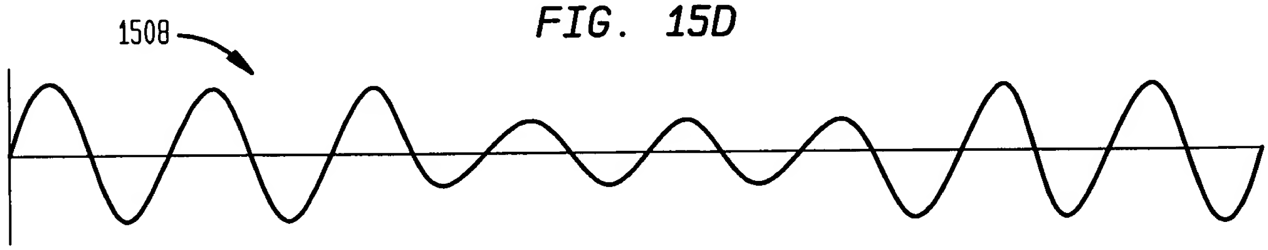

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FIG. 16

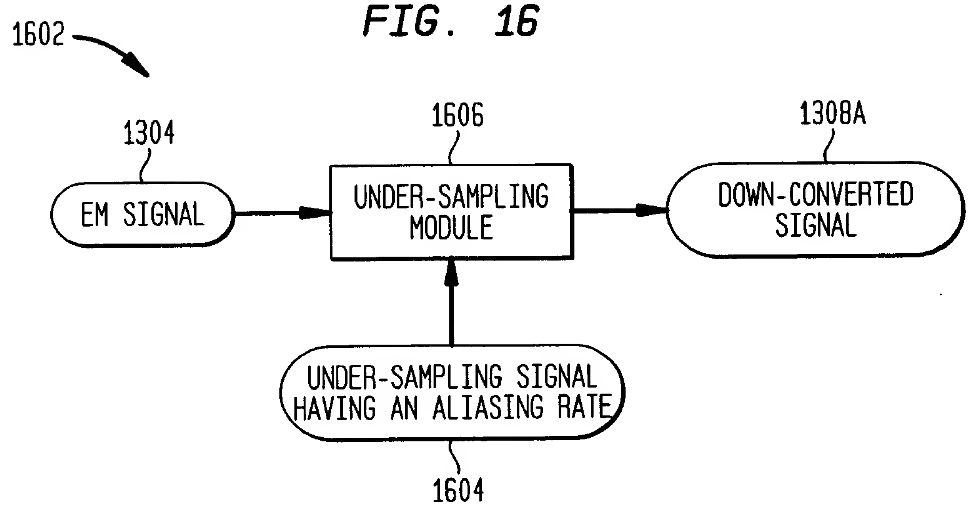

FIG. 17

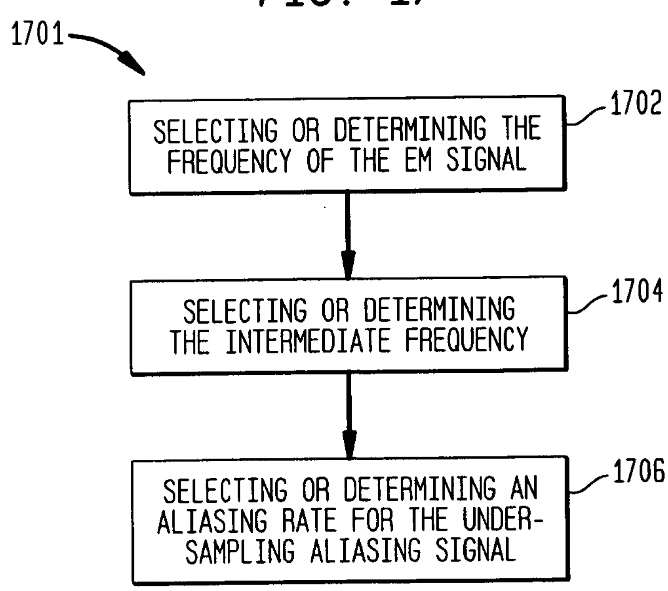

FIG. 18A

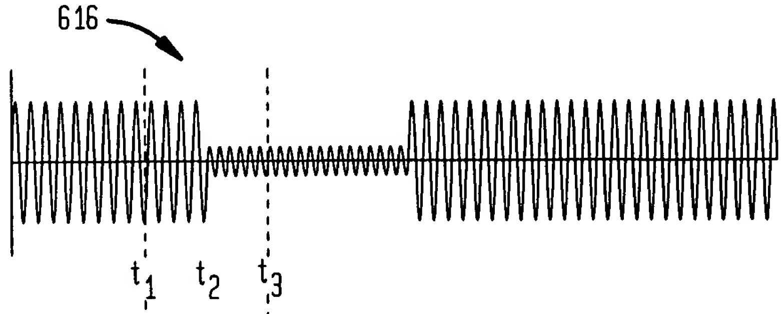

FIG. 18B

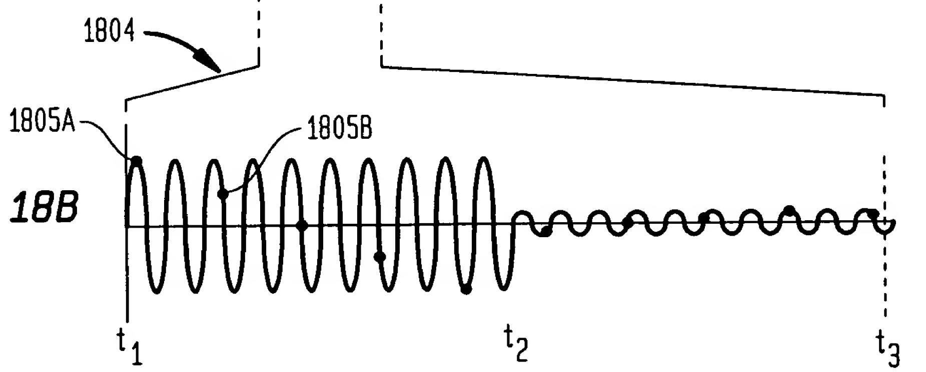

FIG. 18C

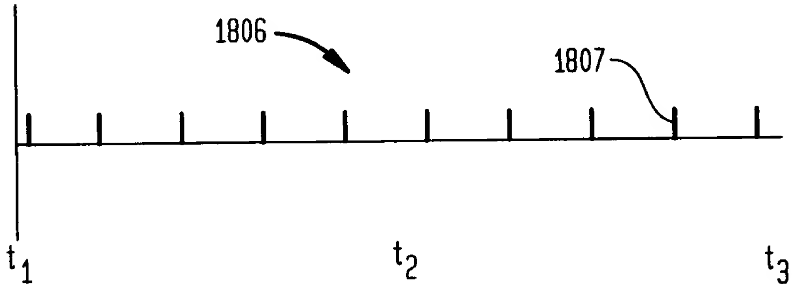

FIG. 18D

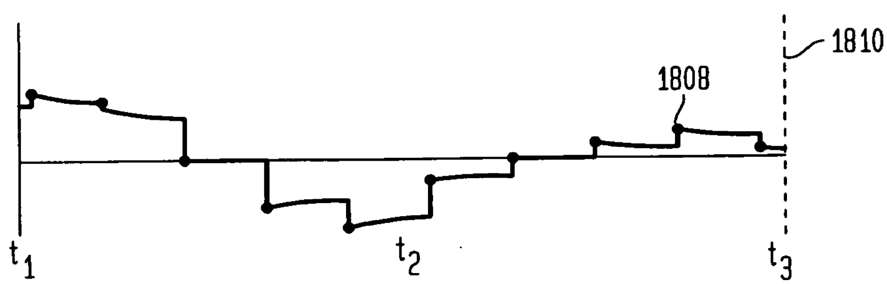

FIG. 18E

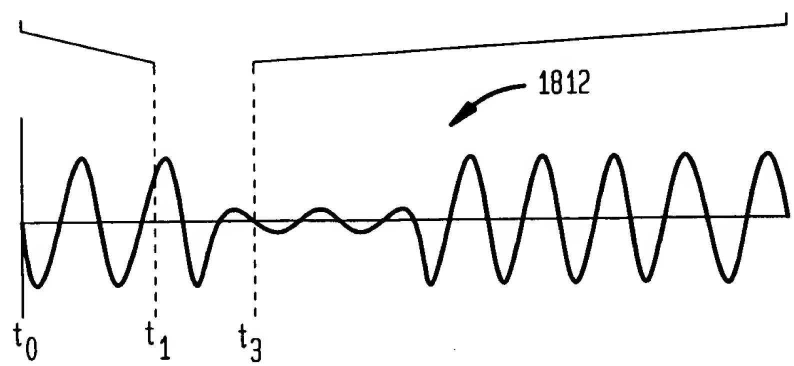

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FIG. 19A

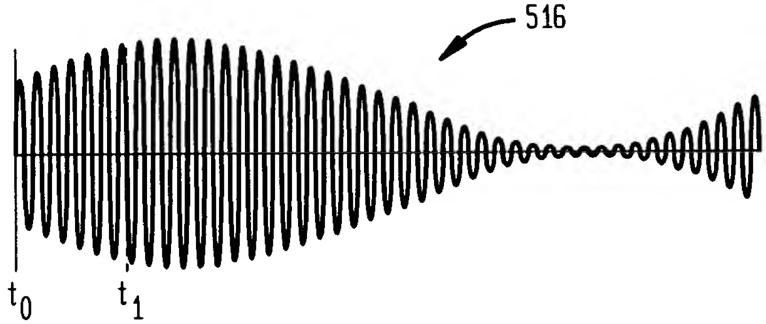

FIG. 19B

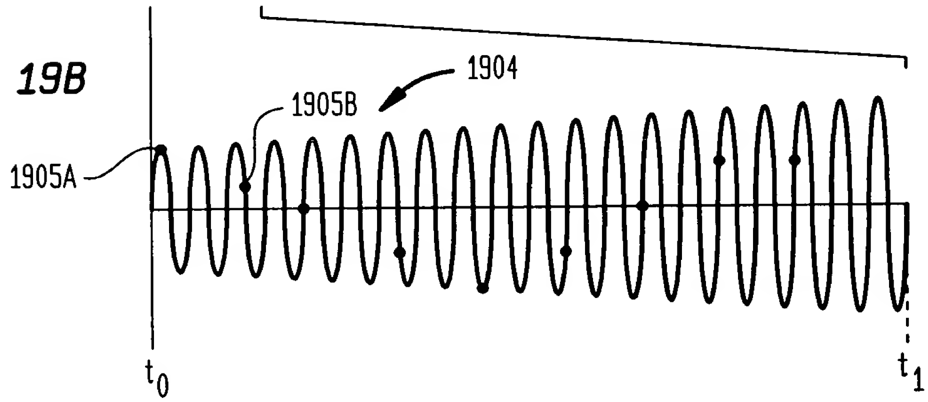

FIG. 19C

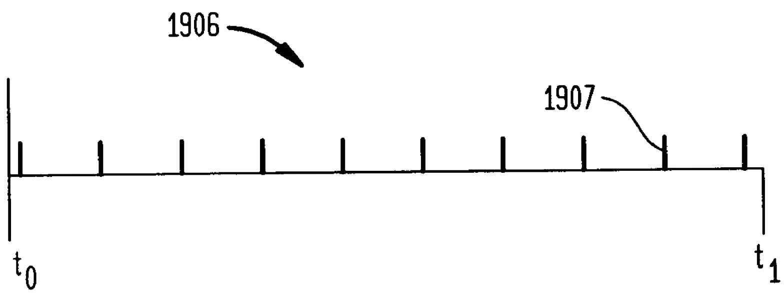

FIG. 19D

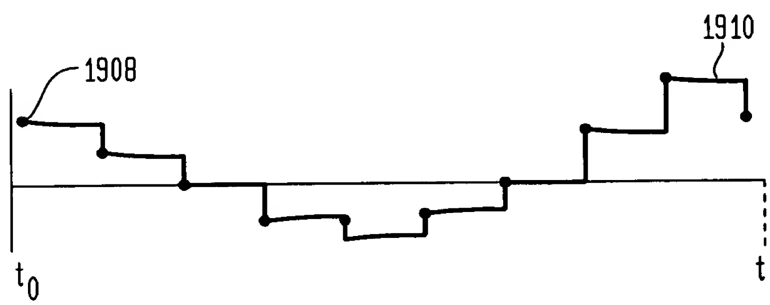

FIG. 19E

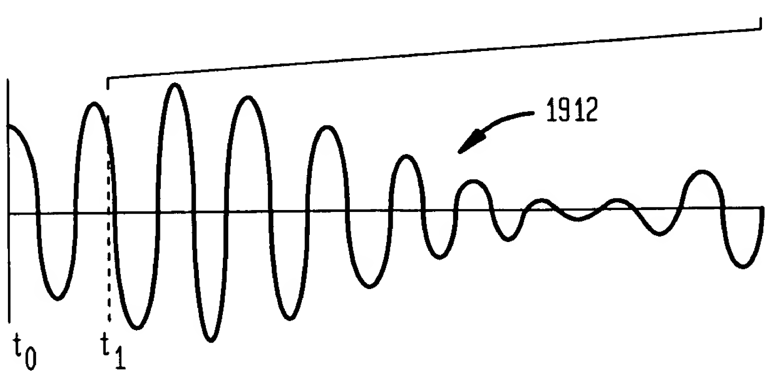

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FIG. 20A

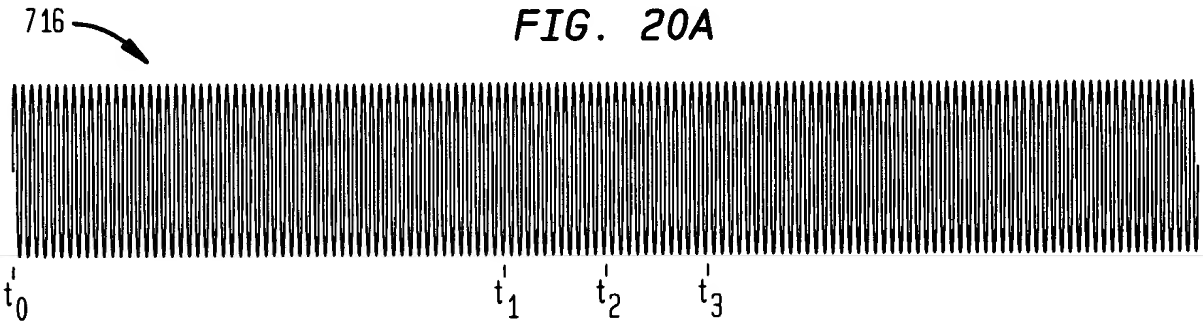

FIG. 20B

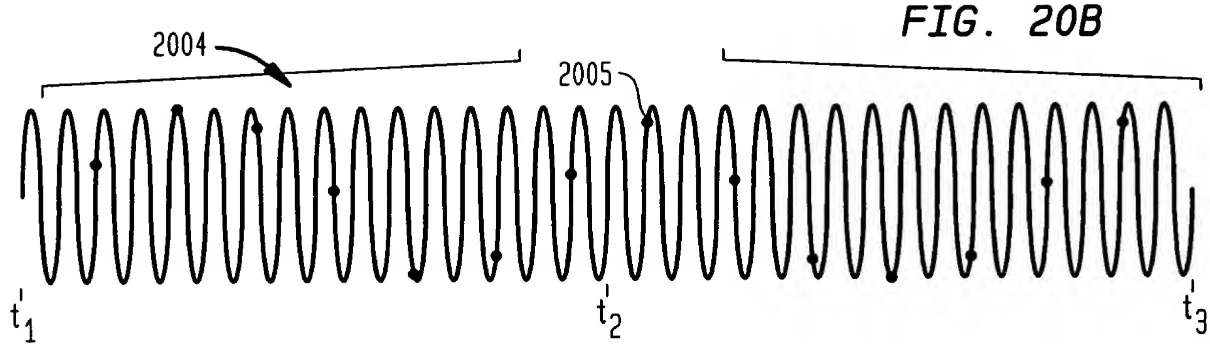

FIG. 20C

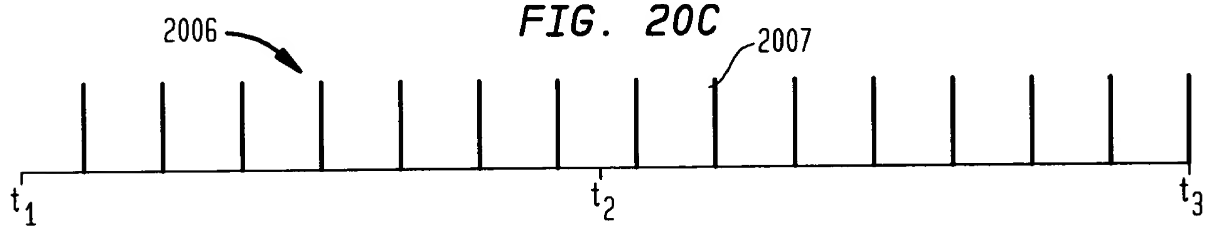

FIG. 20D

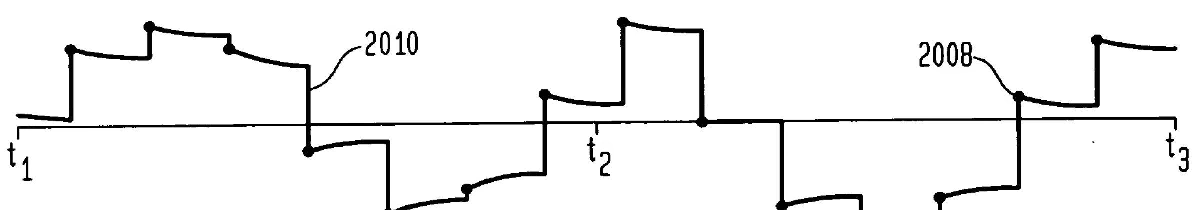

FIG. 20E

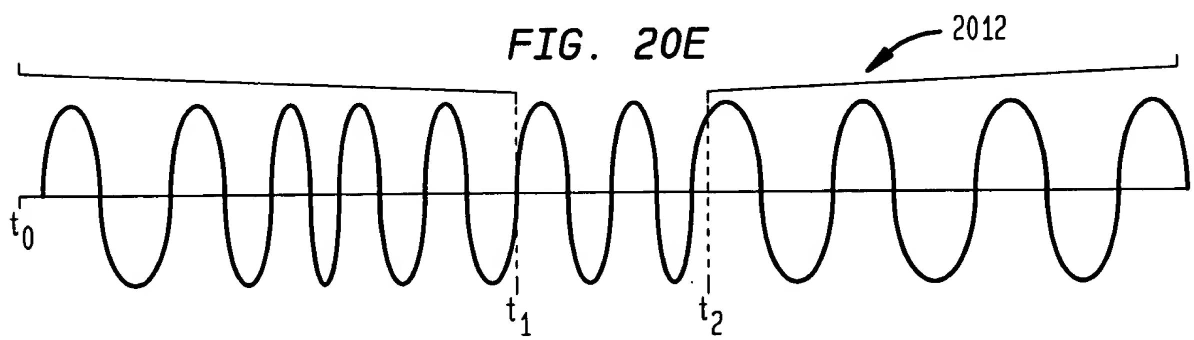

FIG. 21A

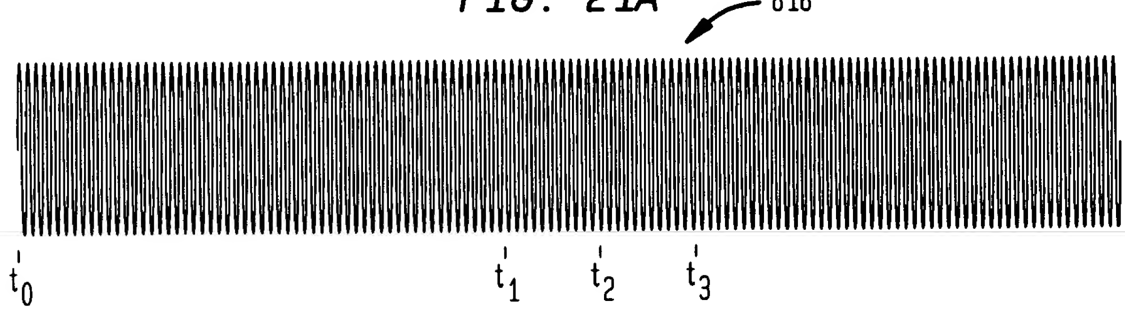

FIG. 21B

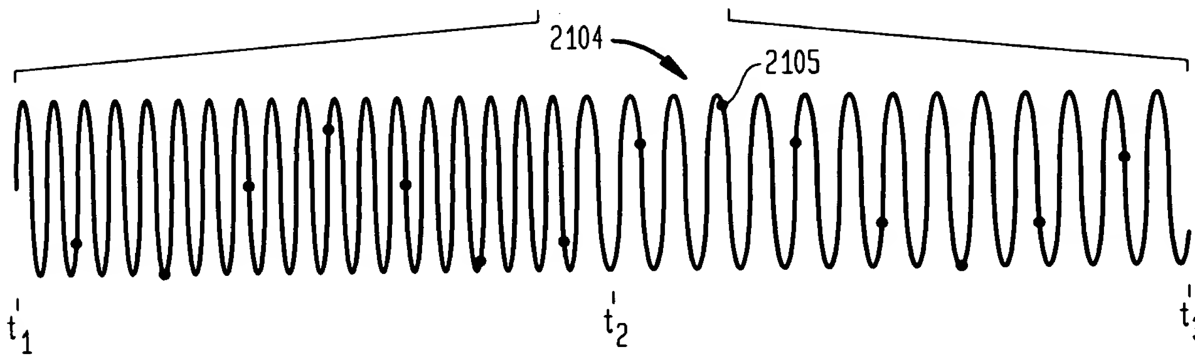

FIG. 21C

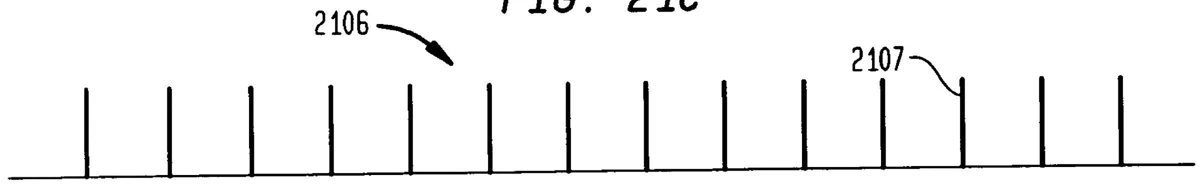

FIG. 21D

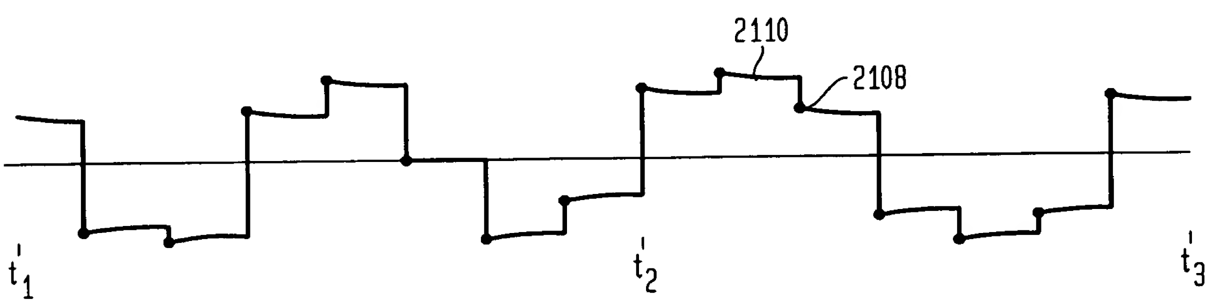

FIG. 21E

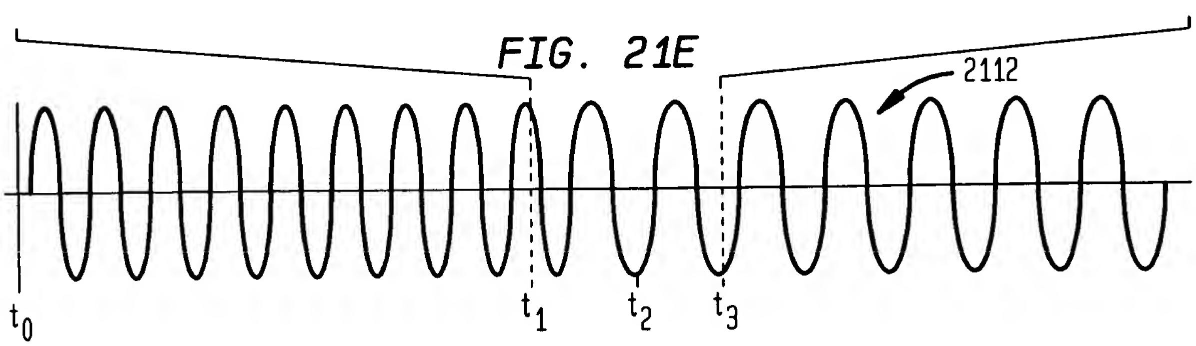

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FIG. 22A

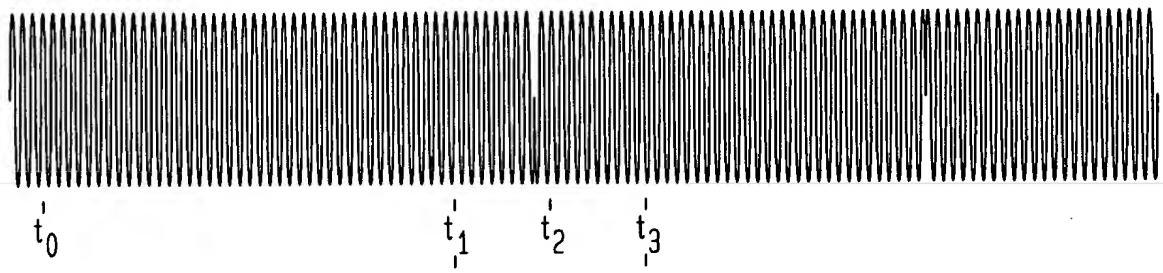

FIG. 22B

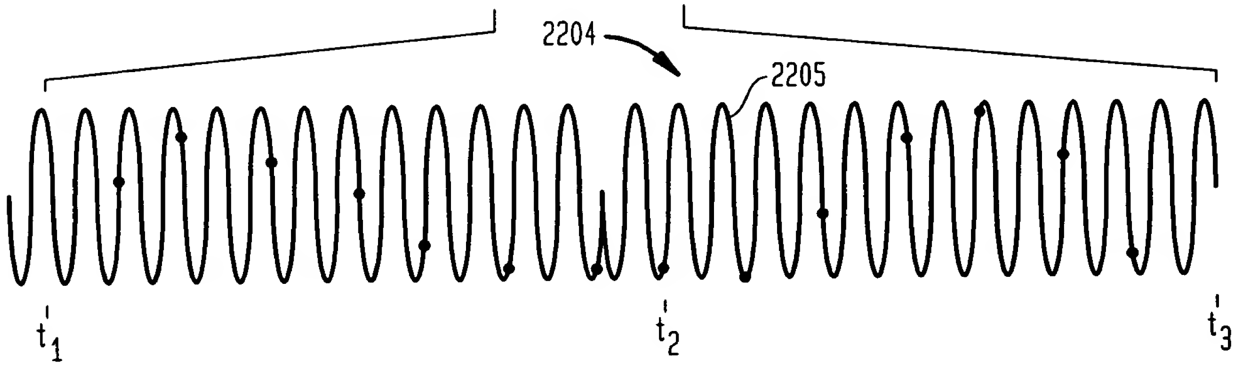

FIG. 22C

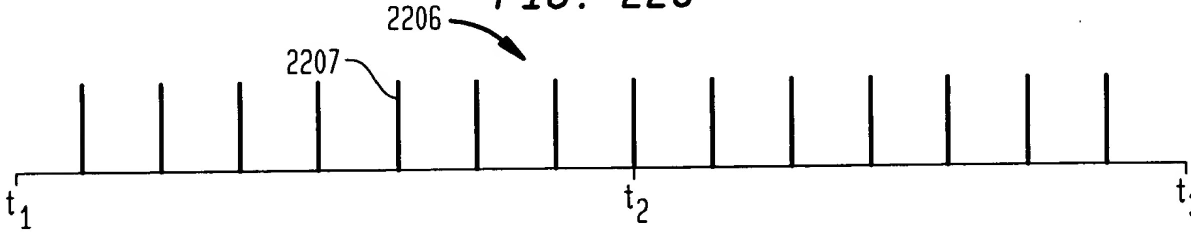

FIG. 22D

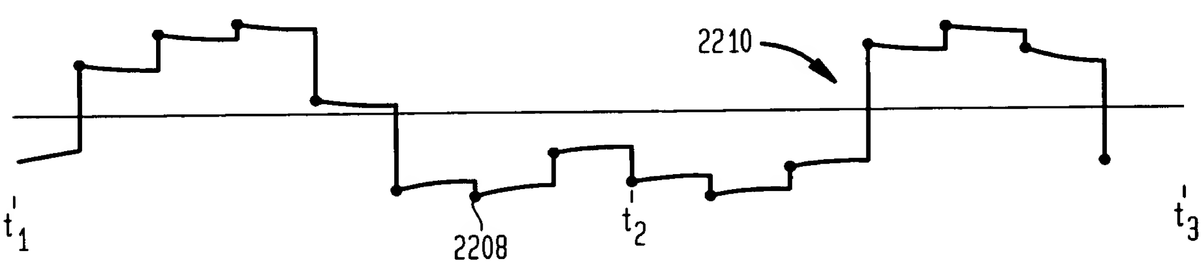

FIG. 22E

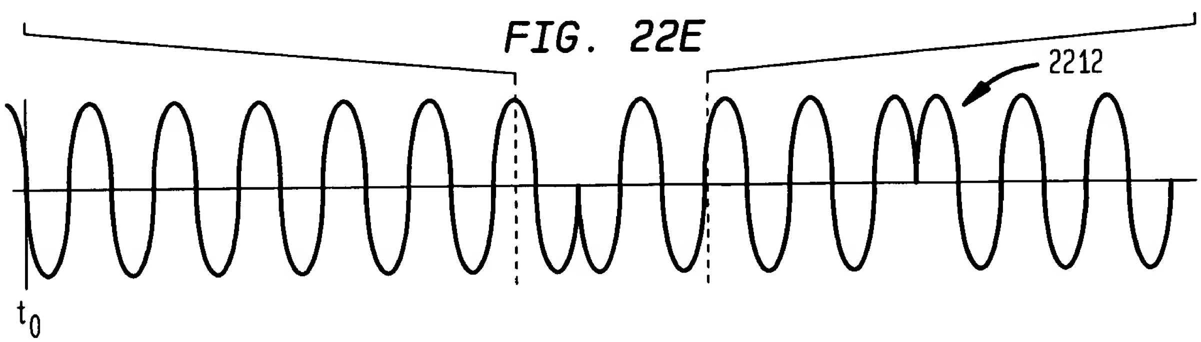

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FIG. 23A

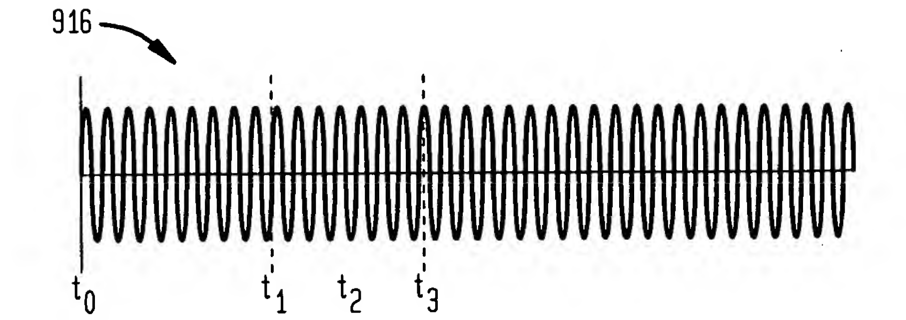


FIG. 23B

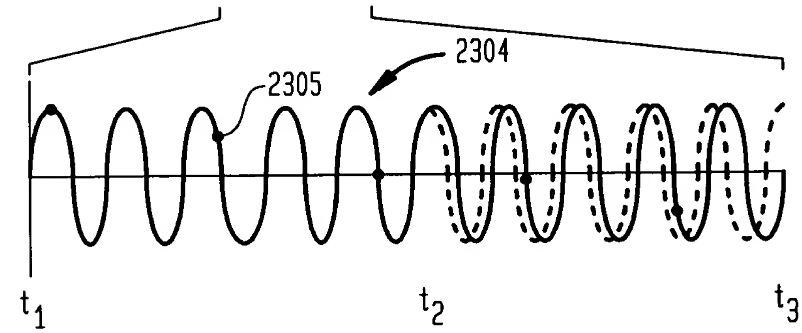


FIG. 23C

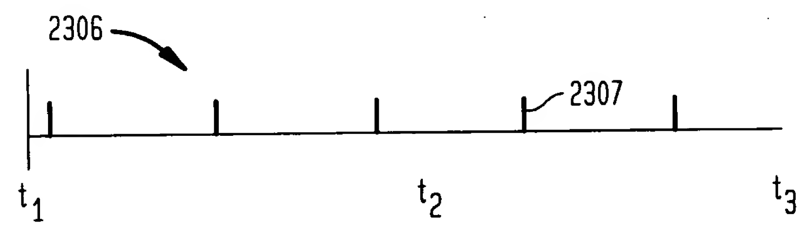


FIG. 23D

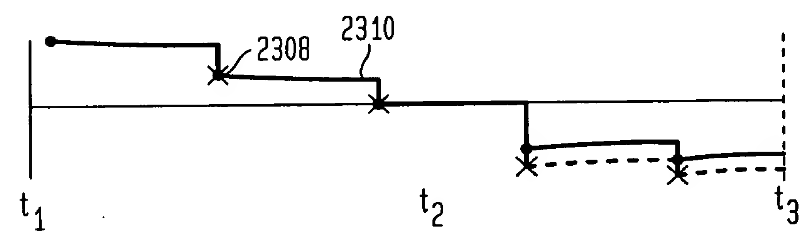
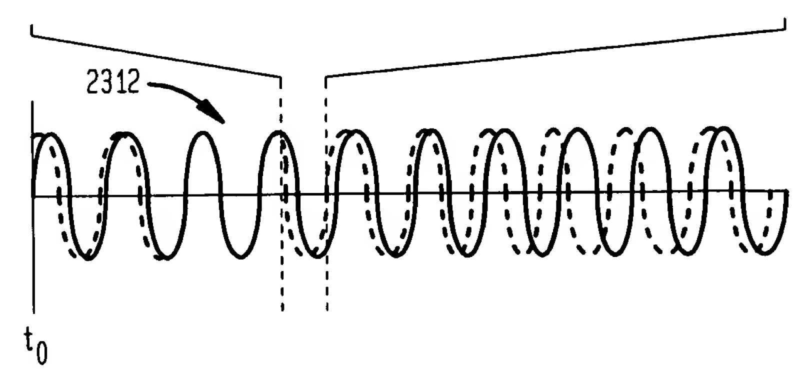


FIG. 23E



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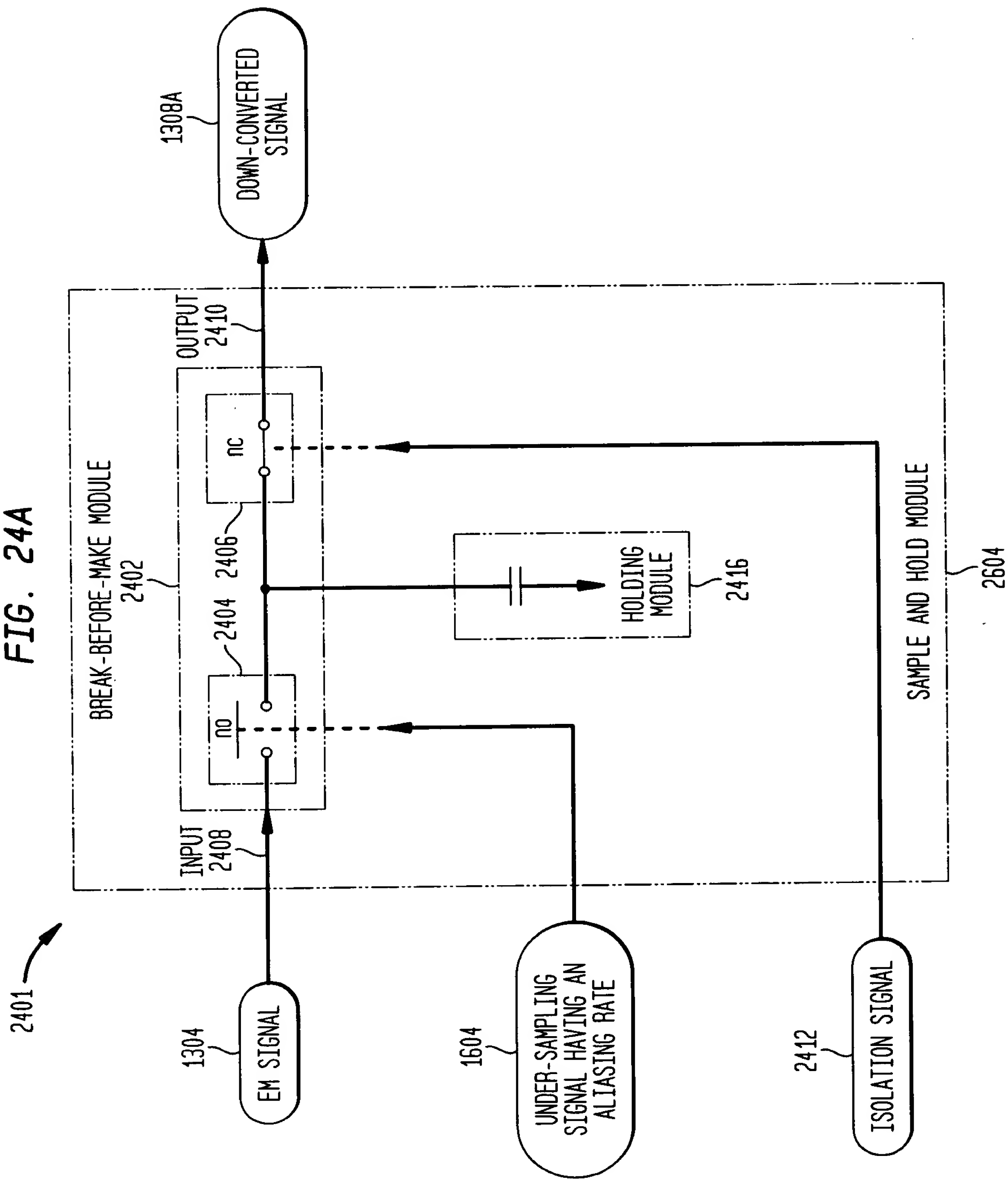

FIG. 24A

FIG. 24B

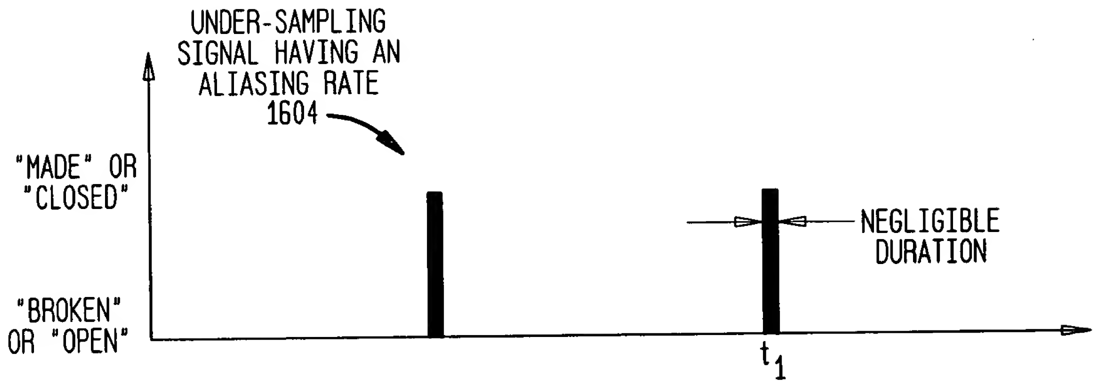

FIG. 24C

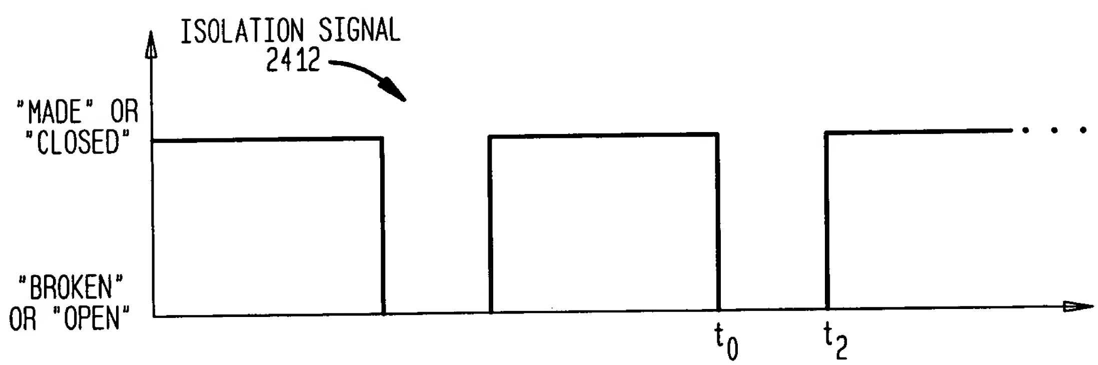

FIG. 25A

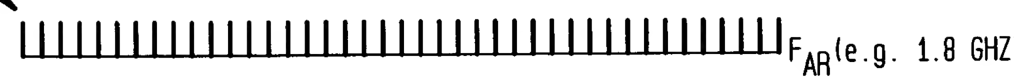

FIG. 25B

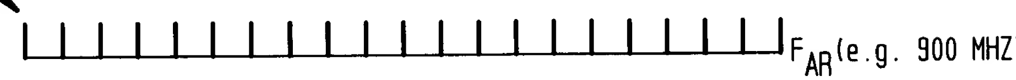

FIG. 25C

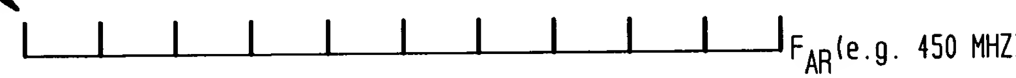

FIG. 25D

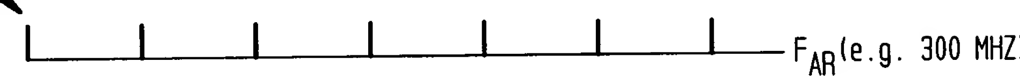

FIG. 25E

FIG. 25F

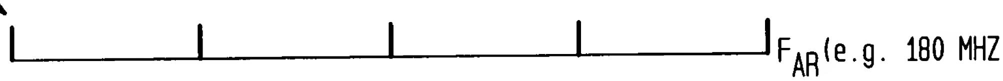

FIG. 25G

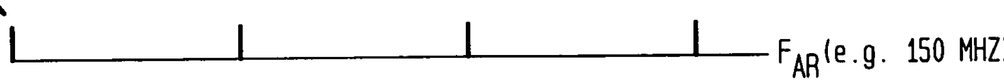

FIG. 25H

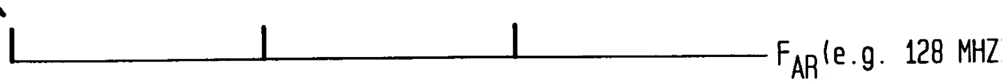

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FIG. 26A

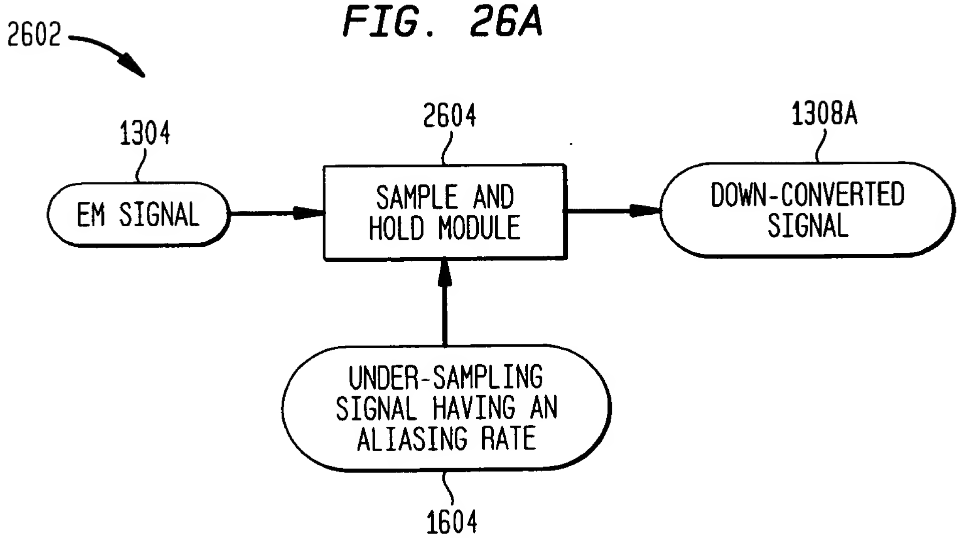

FIG. 26B

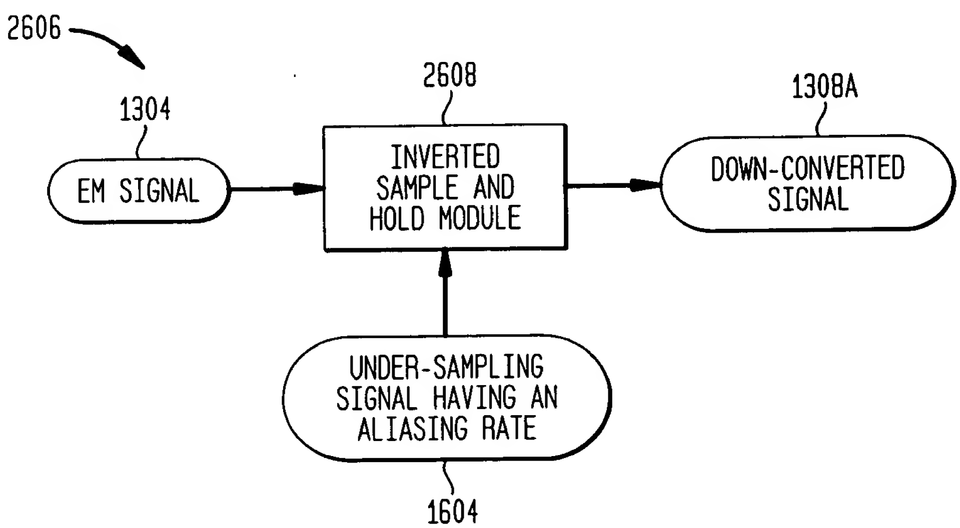

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FIG. 27

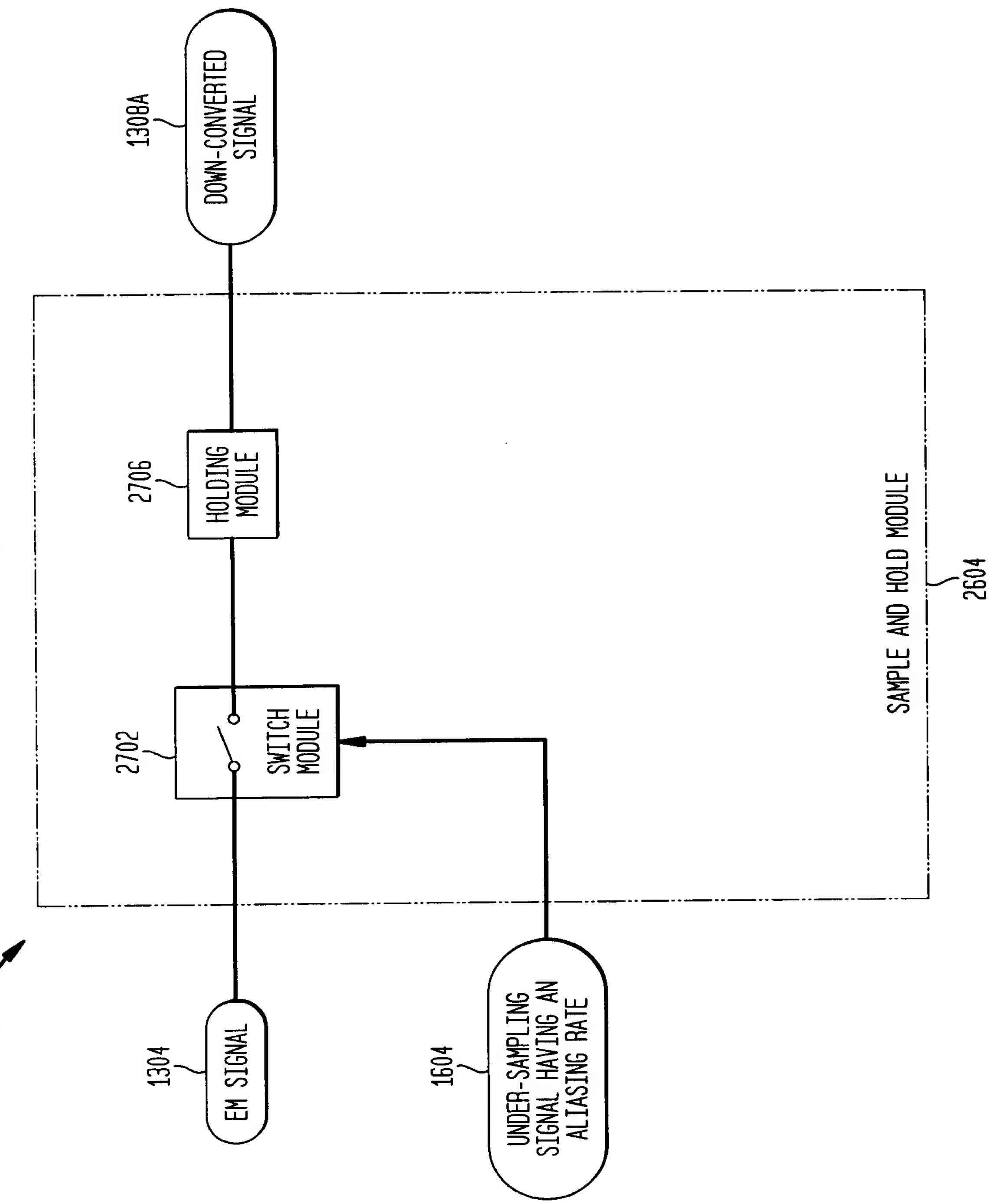

FIG. 28A

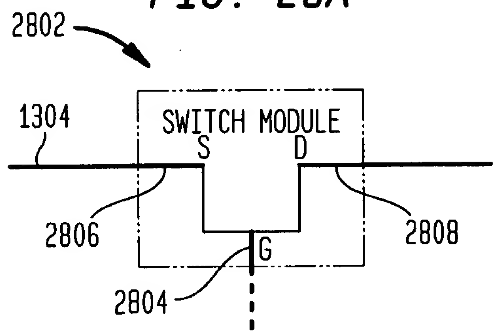

FIG. 28B

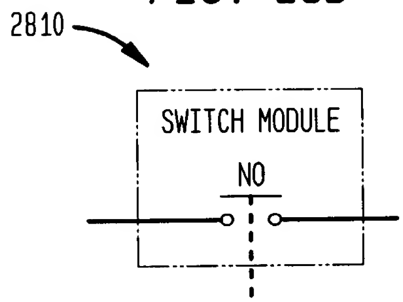

FIG. 28C

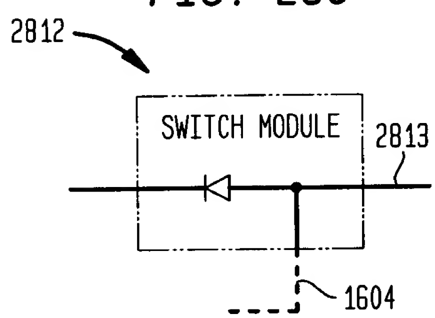

FIG. 28D

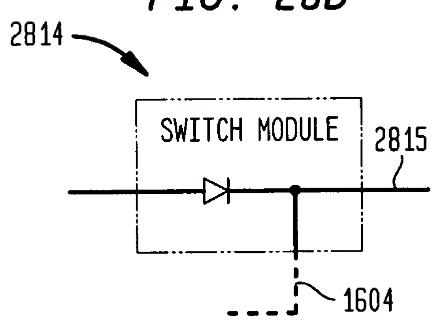

FIG. 29A

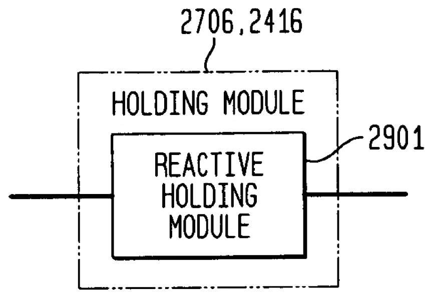

FIG. 29B

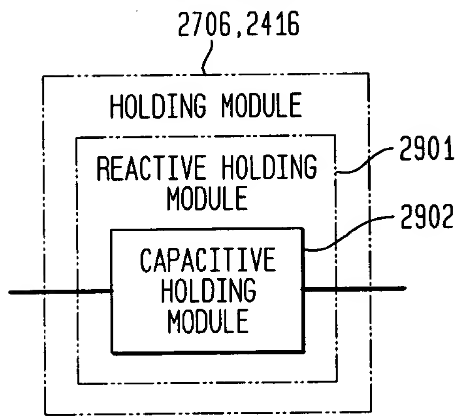

FIG. 29C

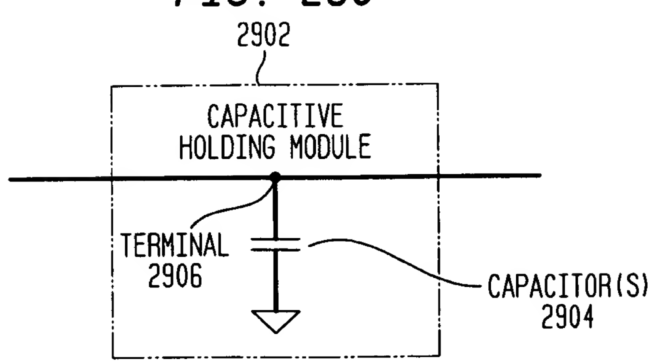

FIG. 29D

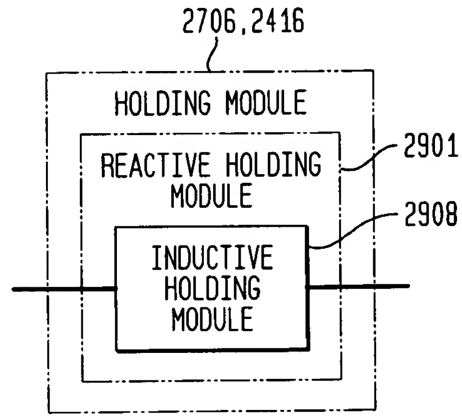

FIG. 29E

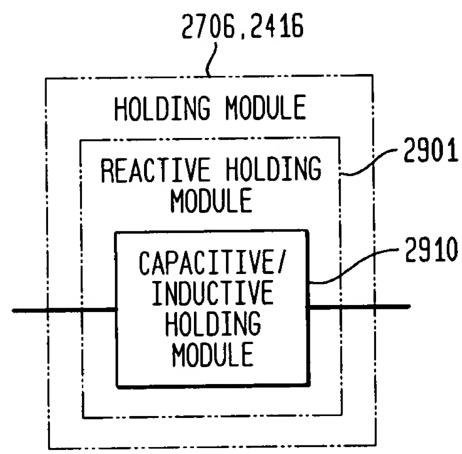

FIG. 29F

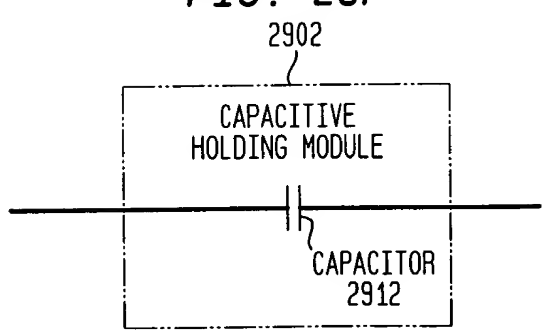

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FIG. 29G

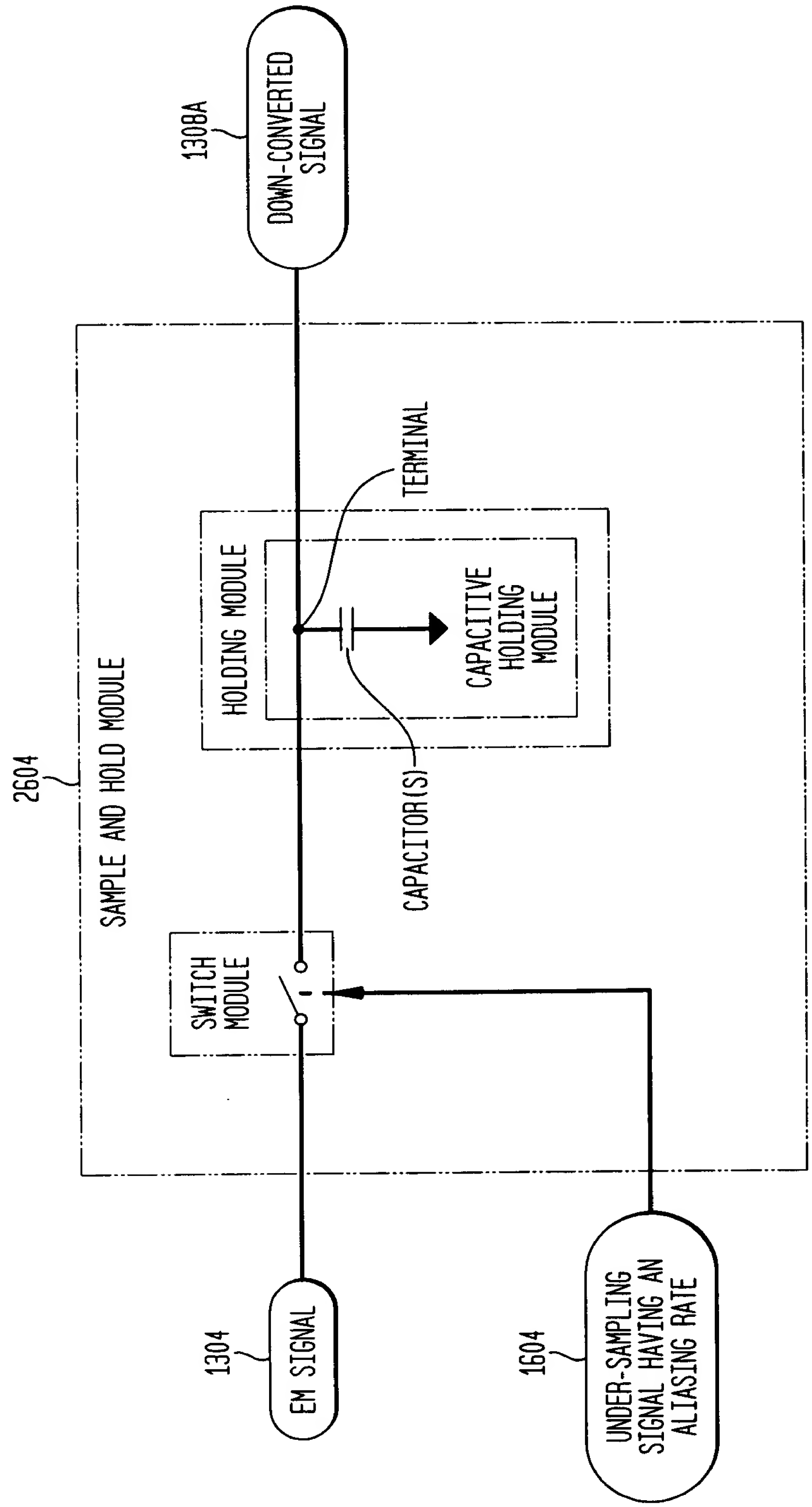

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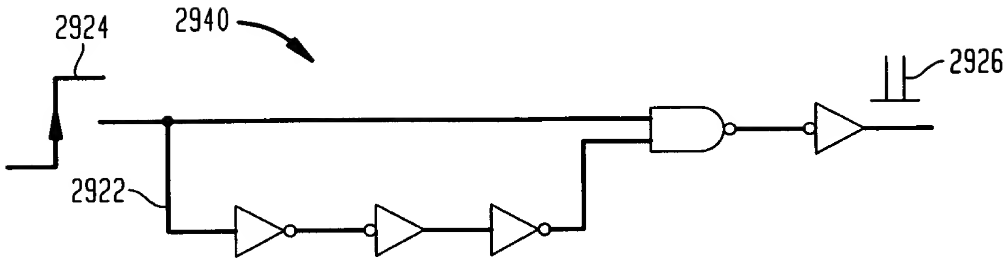
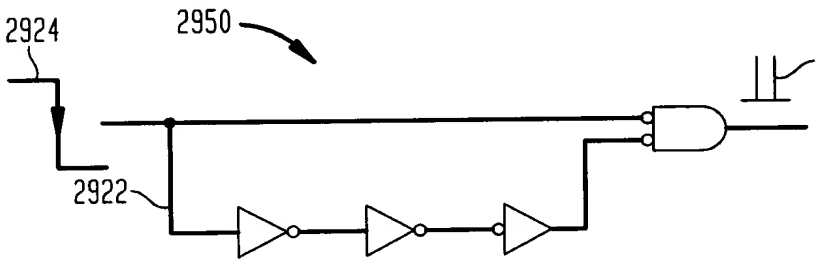
FIG. 29H



A. RISING EDGE PULSE GENERATOR

FIG. 29I



B. FALLING-EDGE PULSE GENERATOR

FIG. 29J

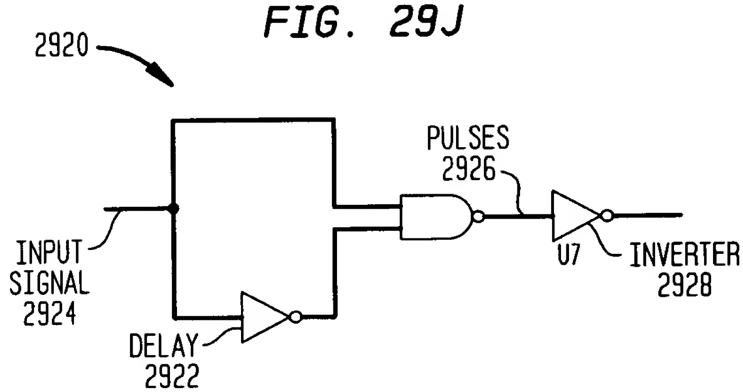


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FIG. 29K

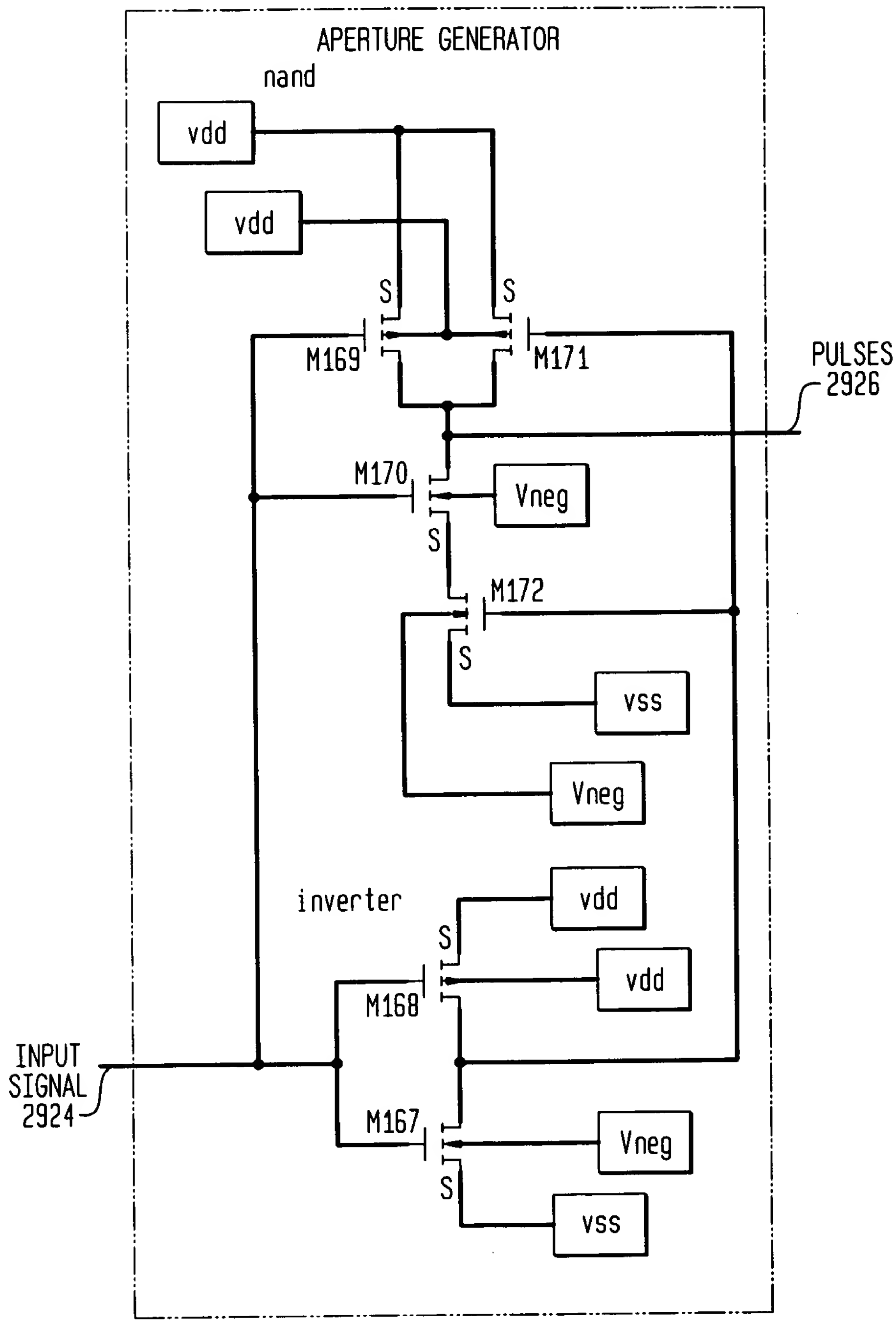

FIG. 29L

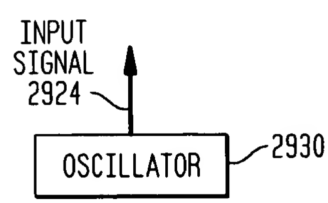

FIG. 30

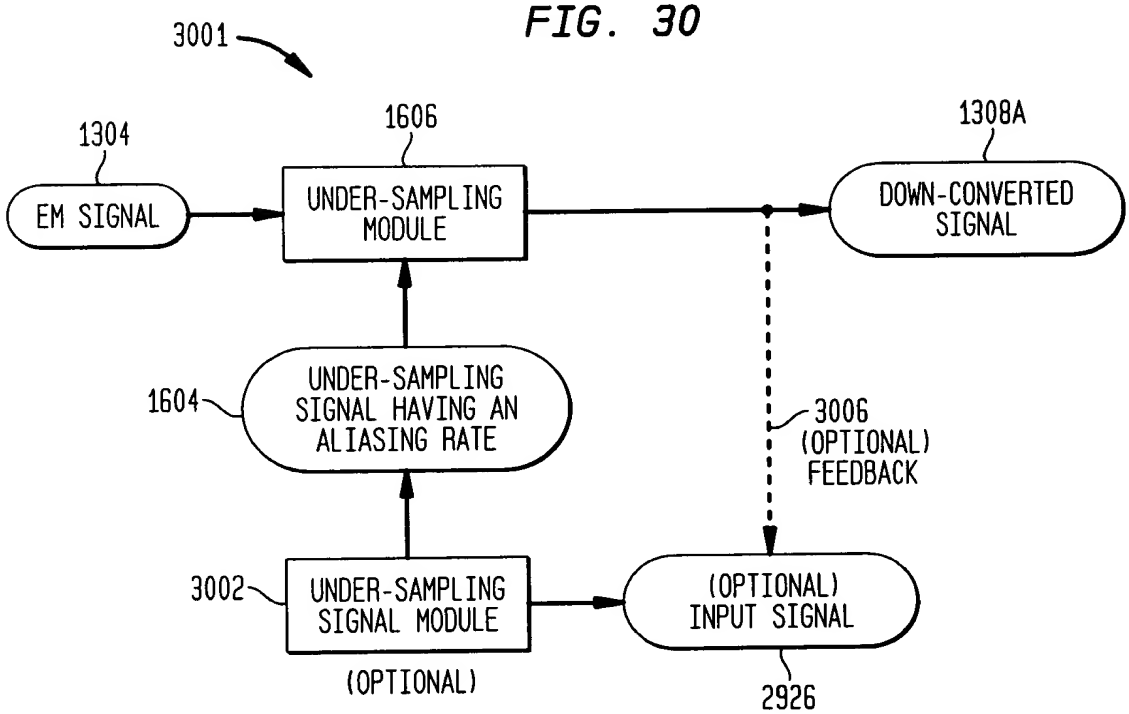
3001
1304
EM SIGNAL
1606
UNDER-SAMPLING MODULE
1308A
DOWN-CONVERTED SIGNAL
1604
UNDER-SAMPLING SIGNAL HAVING AN ALIASING RATE
3006
(OPTIONAL) FEEDBACK
3002
UNDER-SAMPLING SIGNAL MODULE
(OPTIONAL)
(OPTIONAL) INPUT SIGNAL
2926

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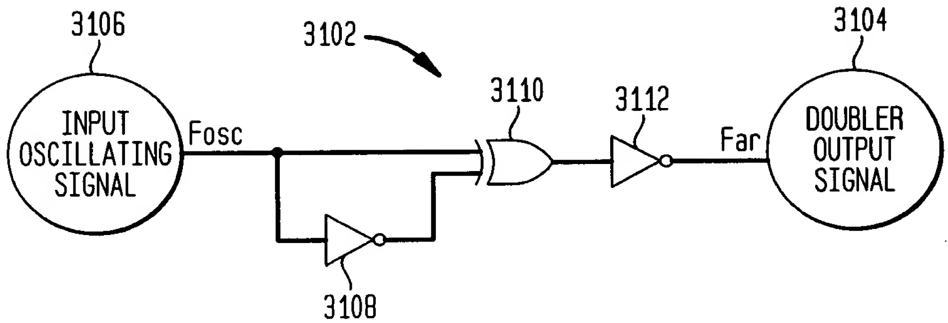
FIG. 31A



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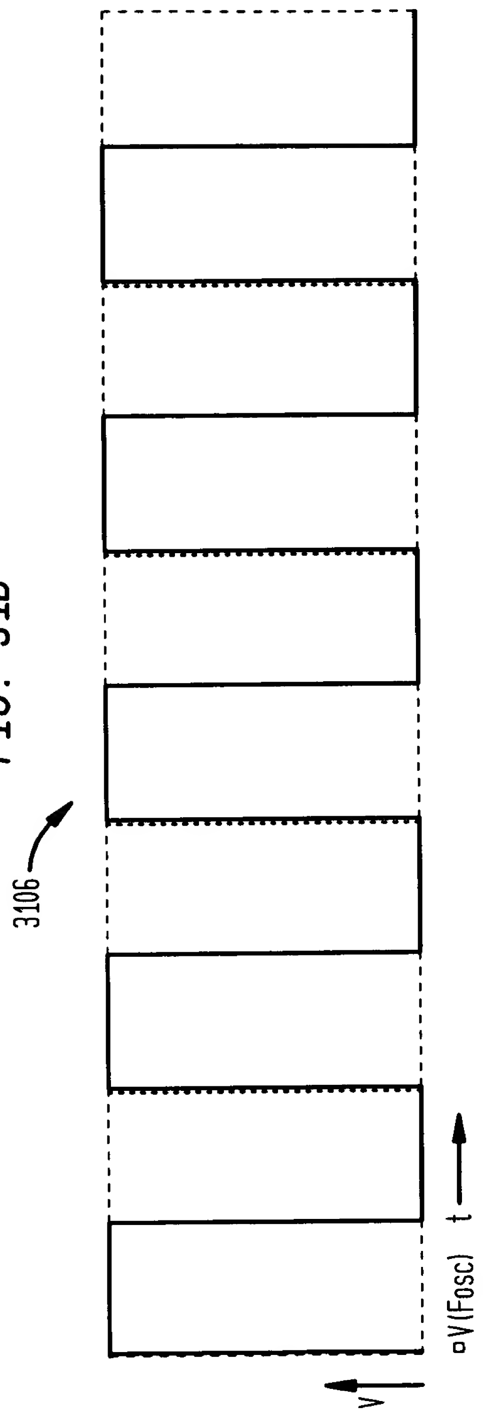

FIG. 31B

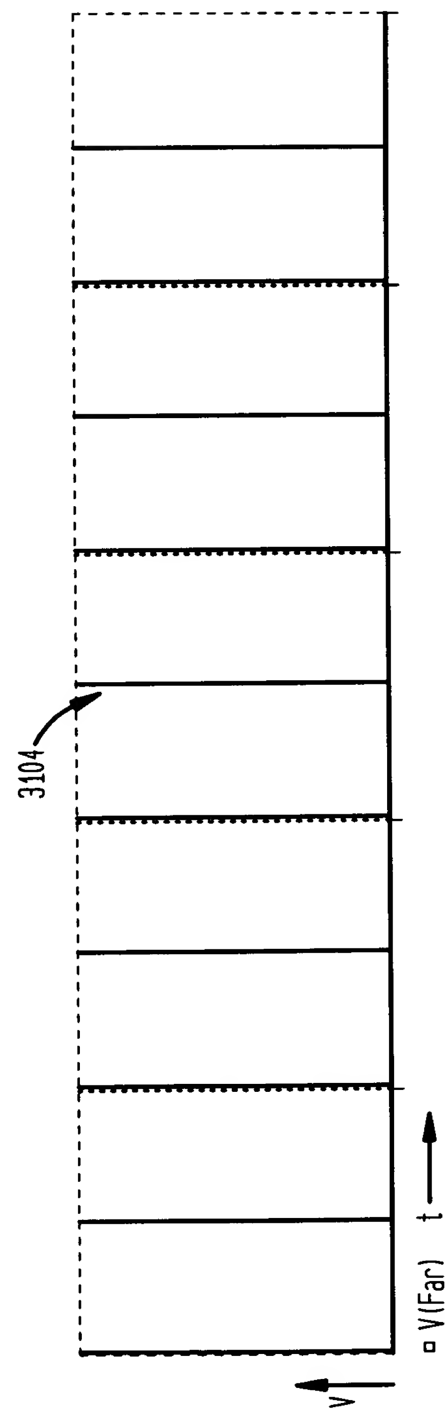

FIG. 31C

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FIG. 32A

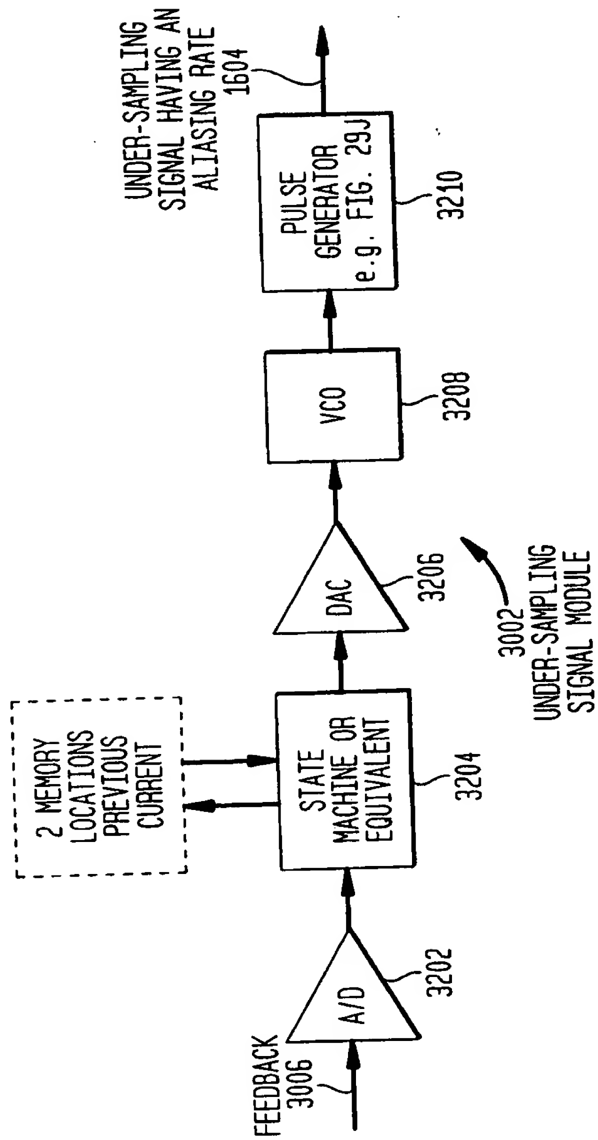

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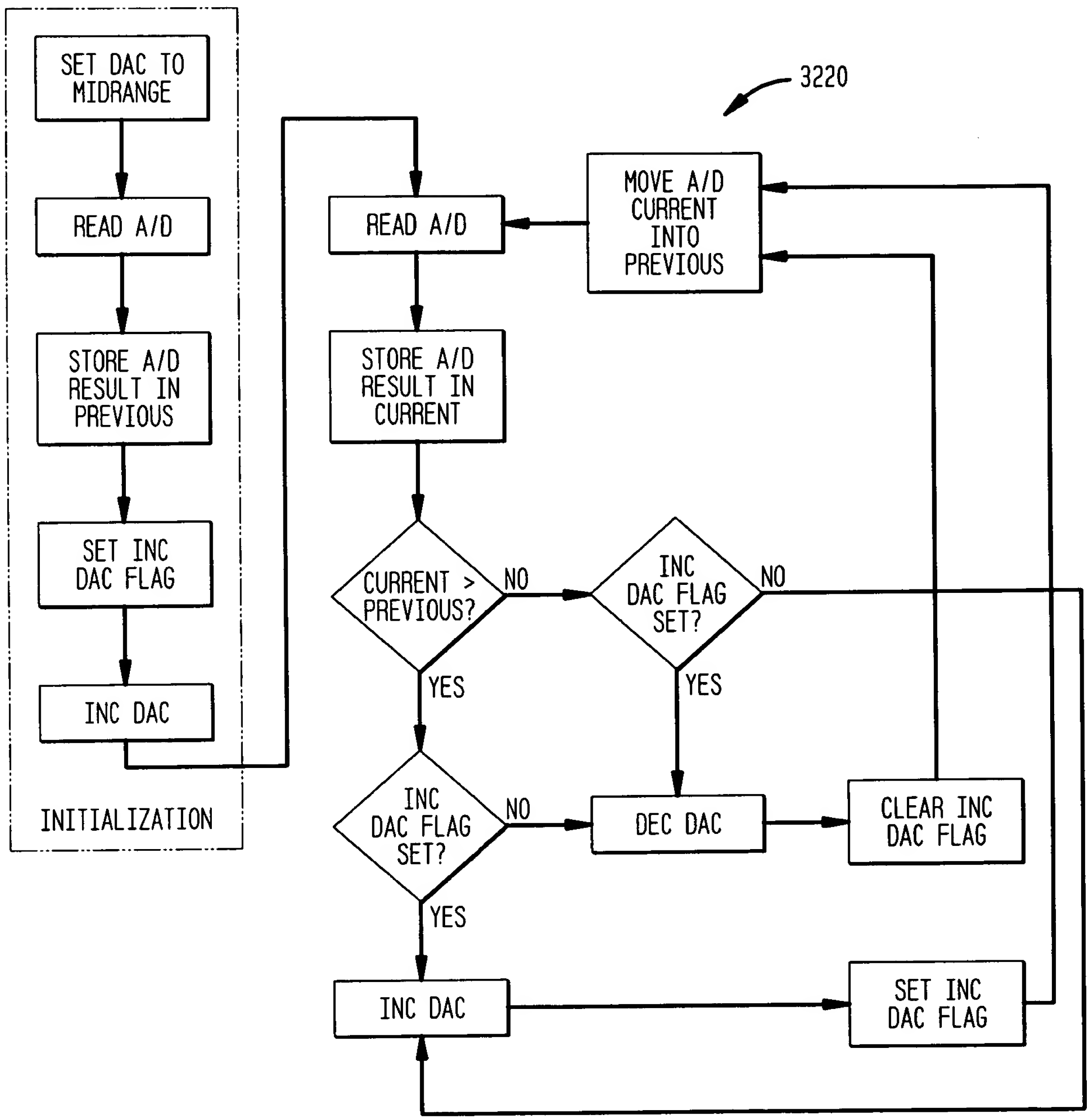
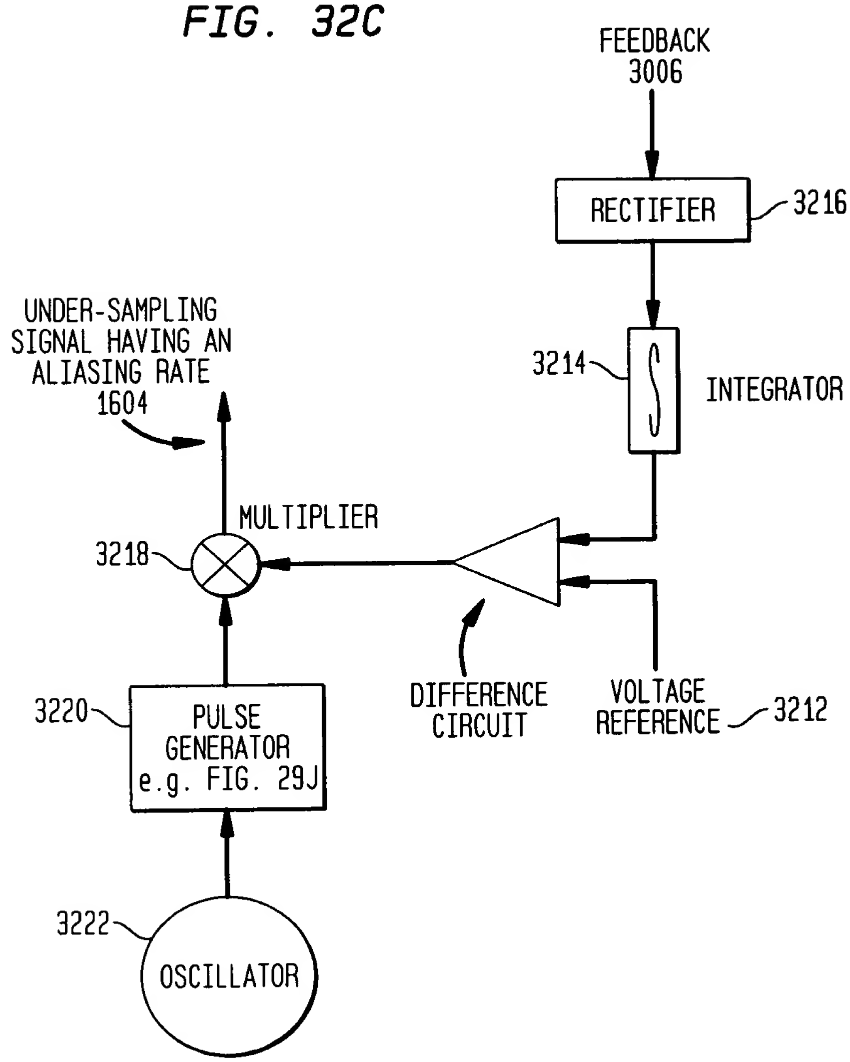
FIG. 32B



STATE MACHINE FLOWCHART

FIG. 32C



ENERGY TRANSFER SIGNAL MODULE 3002

FIG. 33A

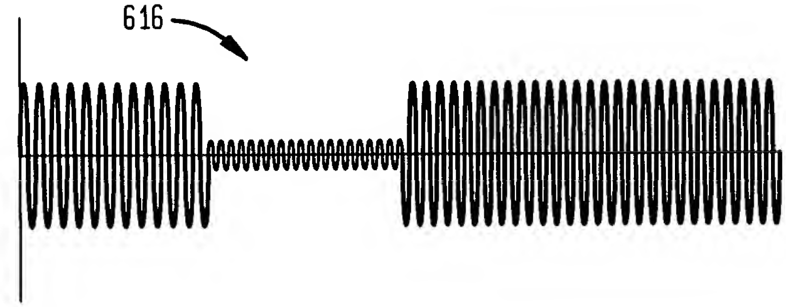


FIG. 33B

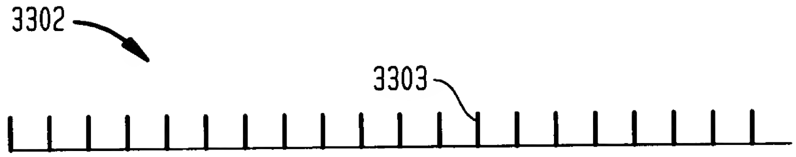


FIG. 33C

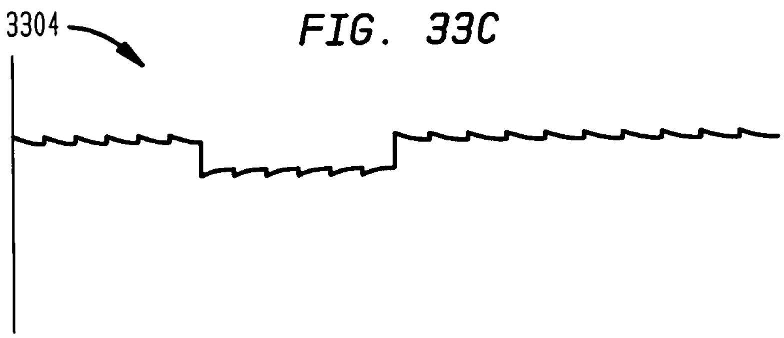
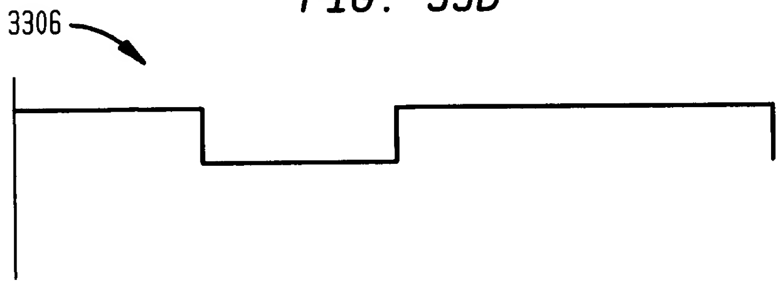


FIG. 33D



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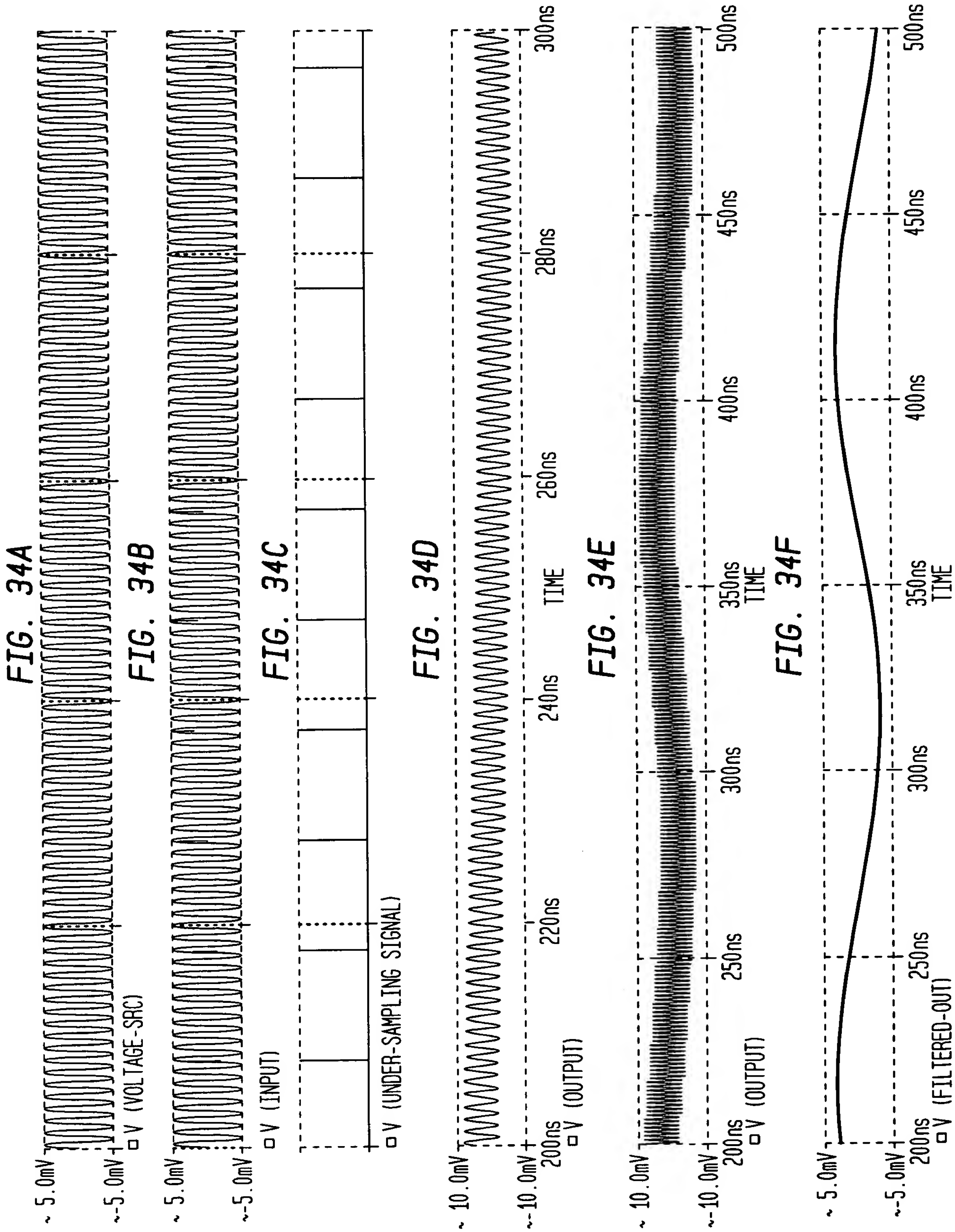

FIG. 34A

FIG. 34B

FIG. 34C

FIG. 34D

FIG. 34E

FIG. 34F

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FIG. 35A

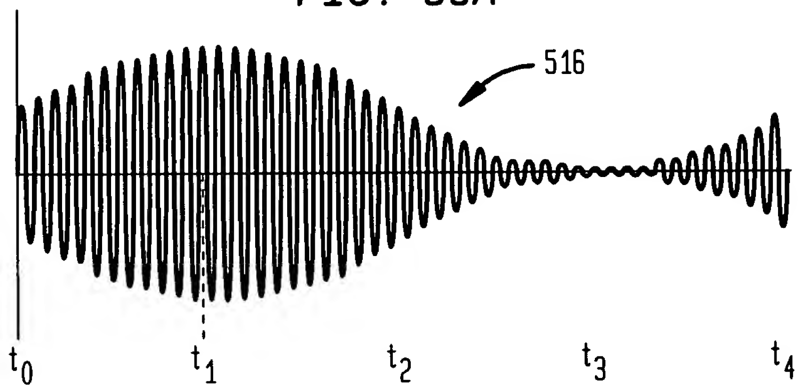

FIG. 35B

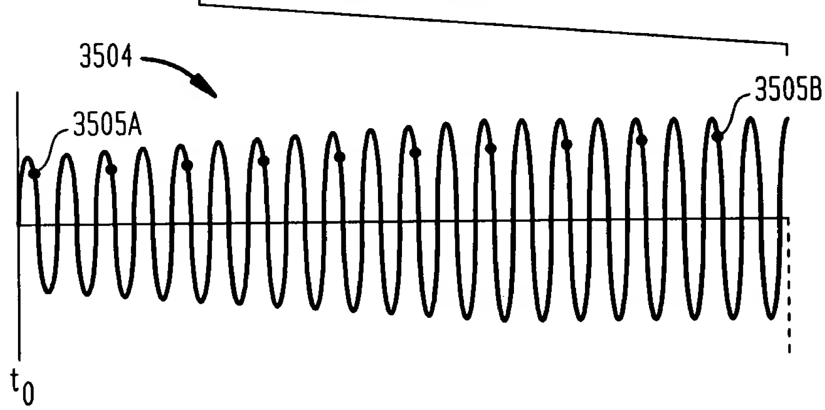

FIG. 35C

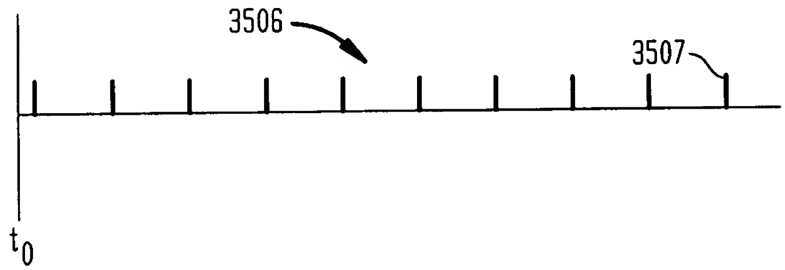

FIG. 35D

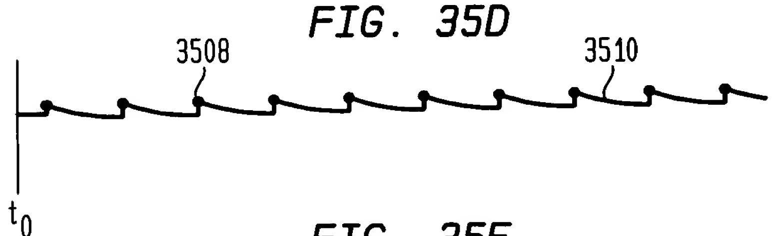

FIG. 35E

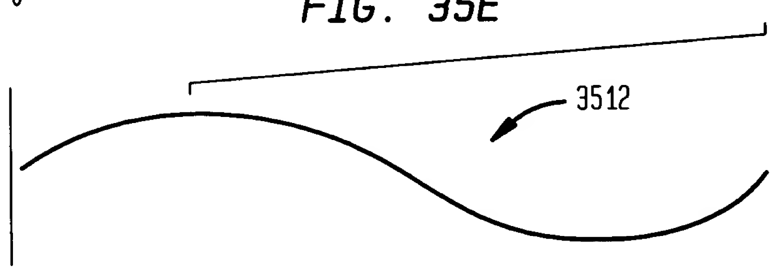

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FIG. 36A

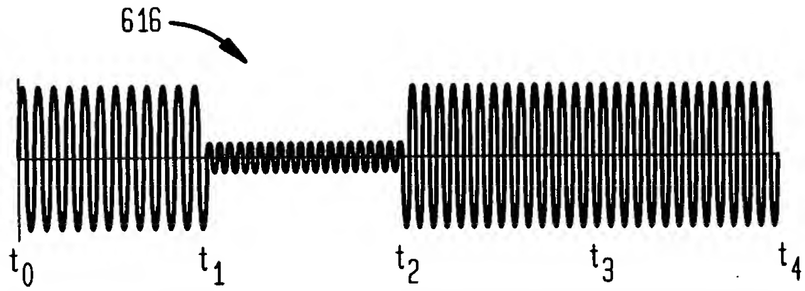

FIG. 36B

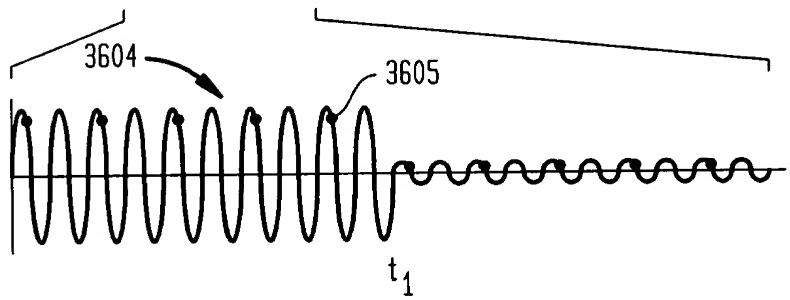

FIG. 36C

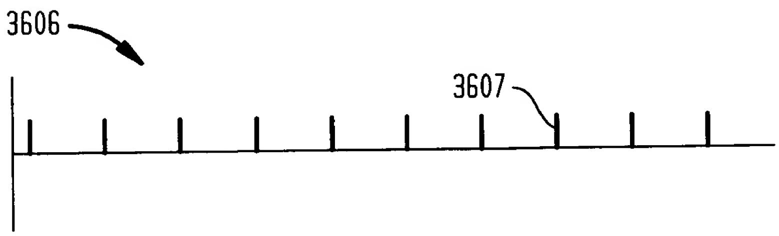

FIG. 36D

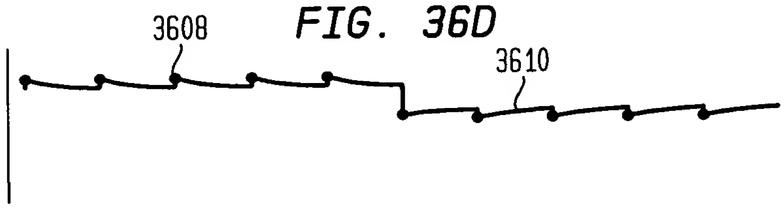

FIG. 36E

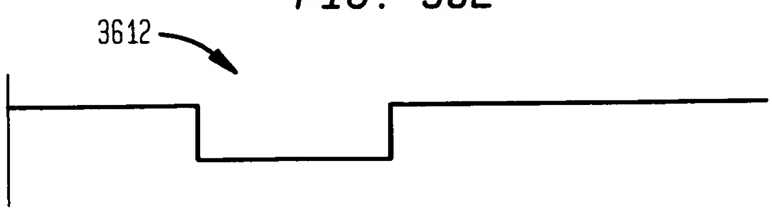

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FIG. 37A

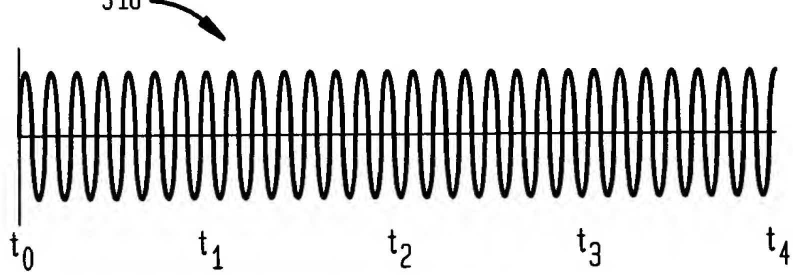

FIG. 37B

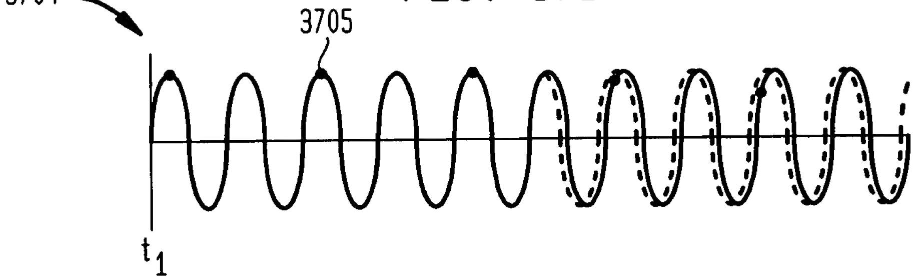

FIG. 37C

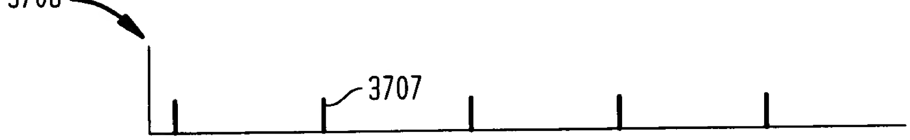

FIG. 37D

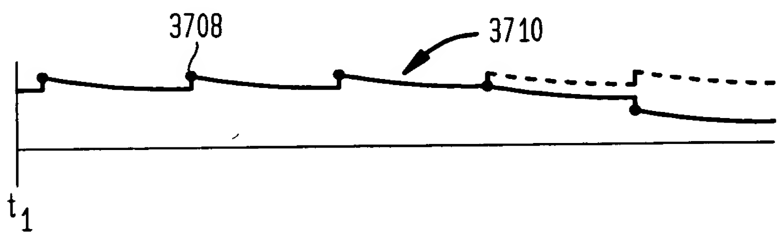

FIG. 37E

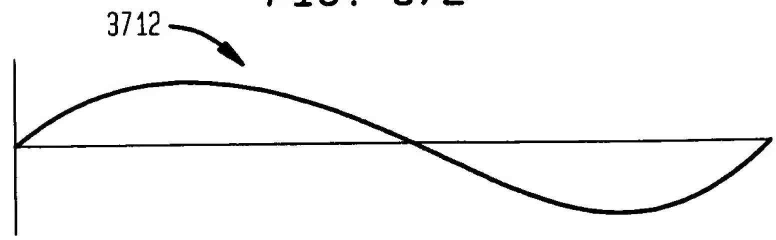

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FIG. 38A

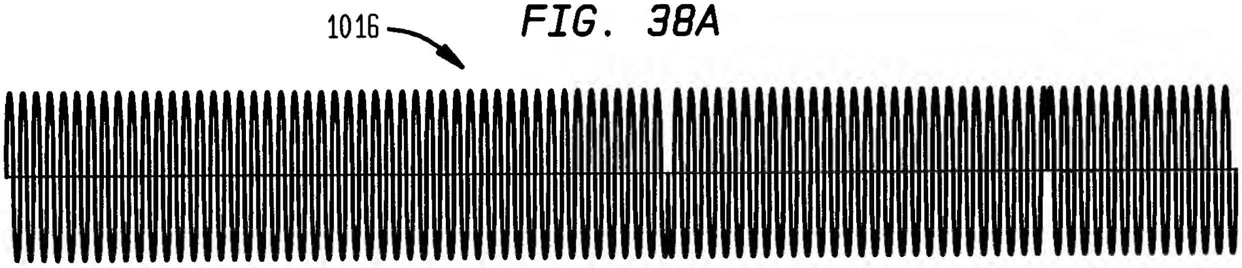

FIG. 38B

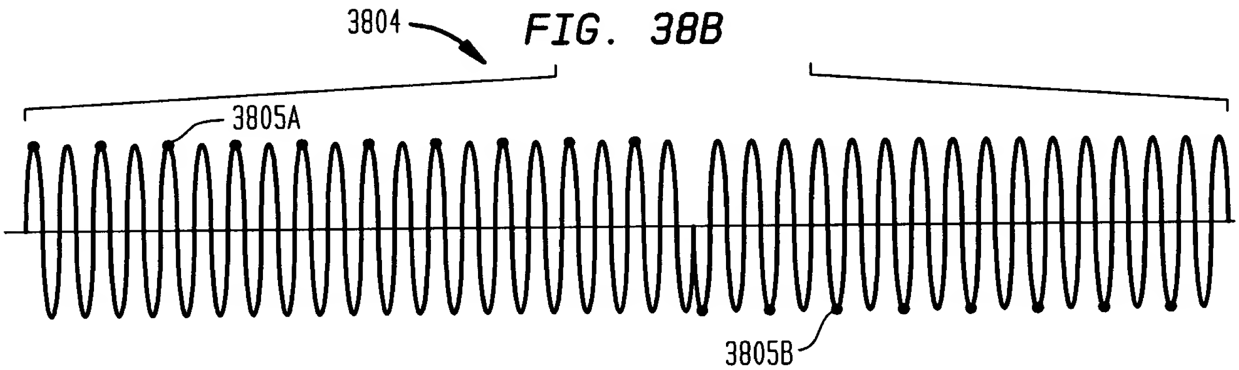

FIG. 38C

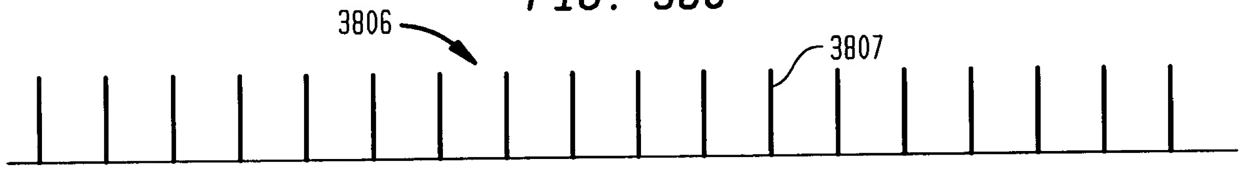

FIG. 38D

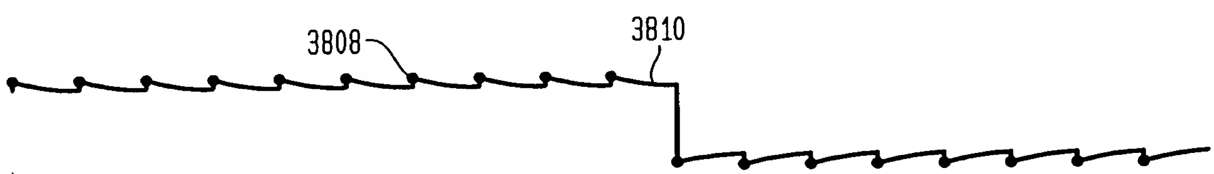

FIG. 38E

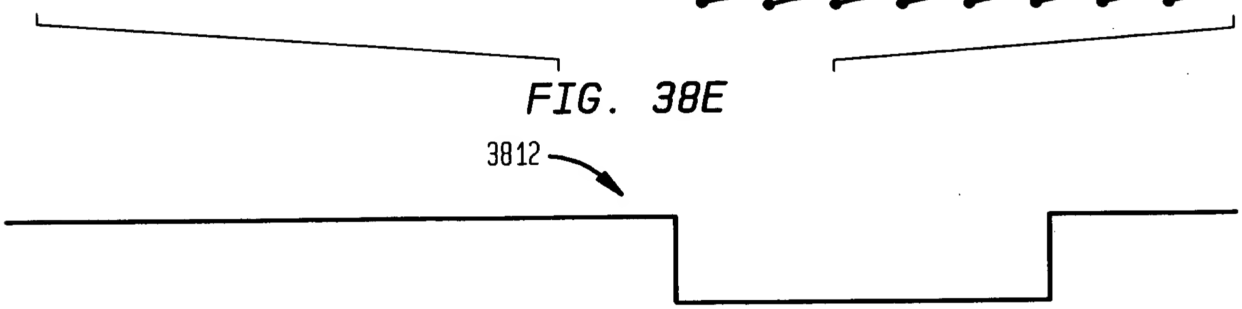

FIG. 39A

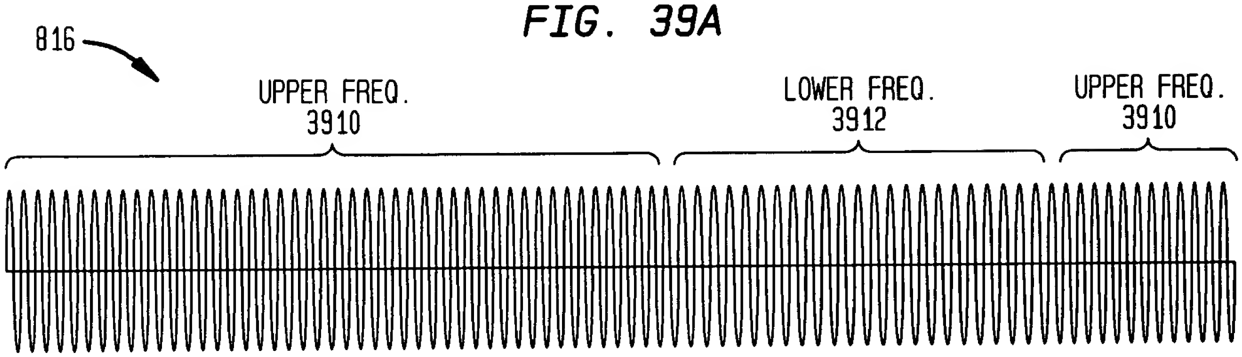

FIG. 39B

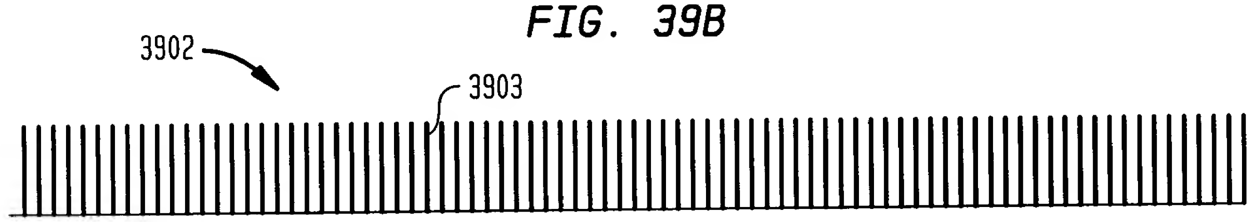

FIG. 39C

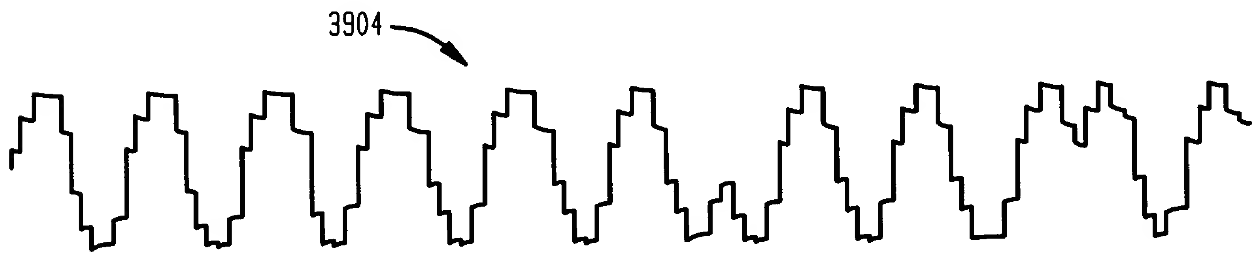

FIG. 39D

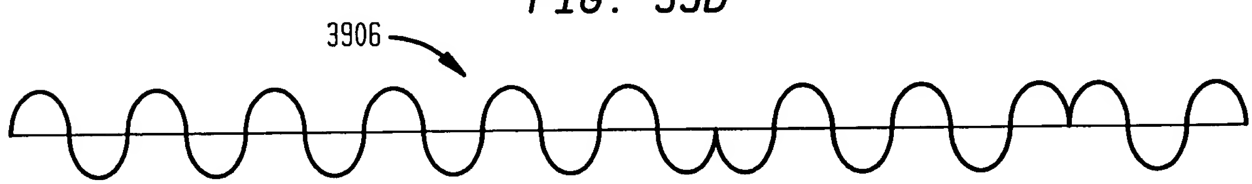

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FIG. 40A

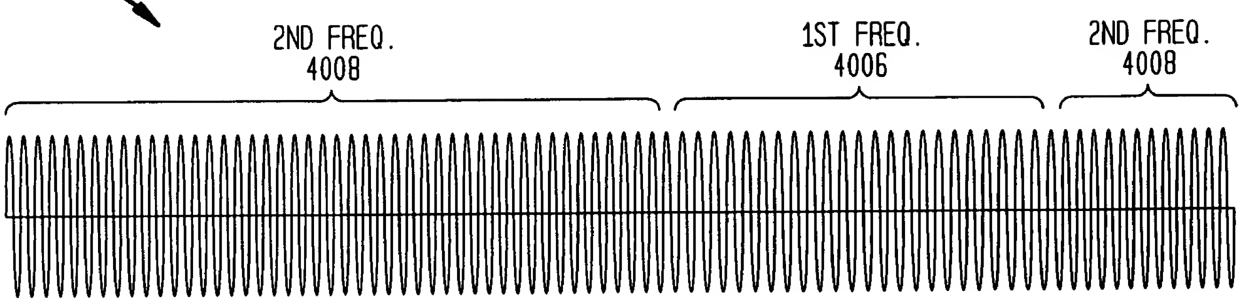

FIG. 40B

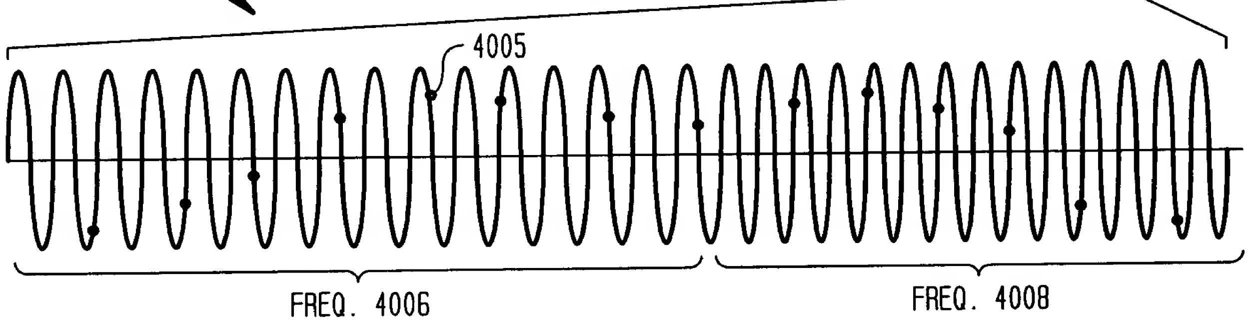

FIG. 40C

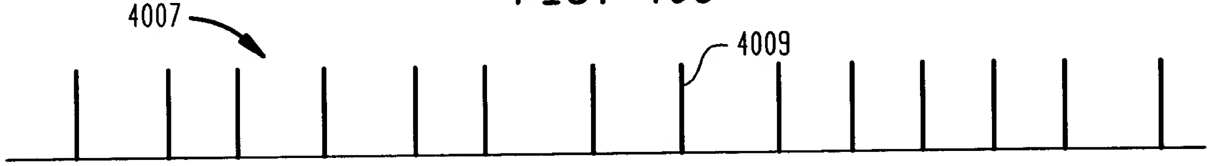

FIG. 40D

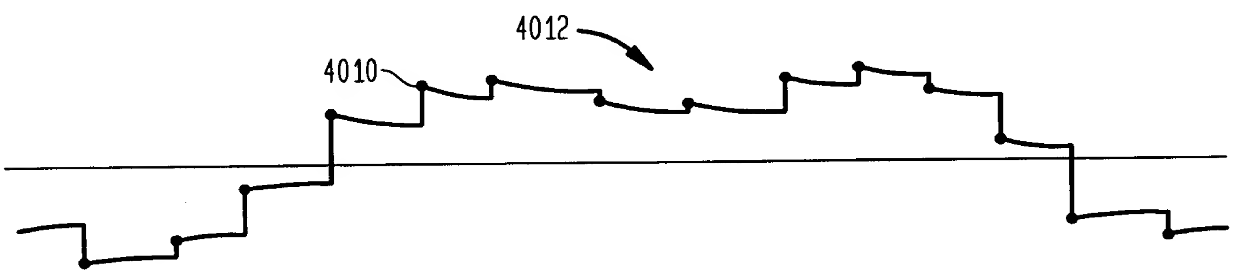

FIG. 40E

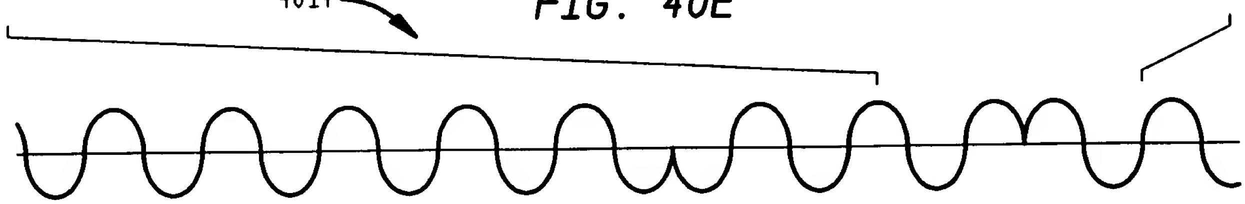

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FIG. 41A

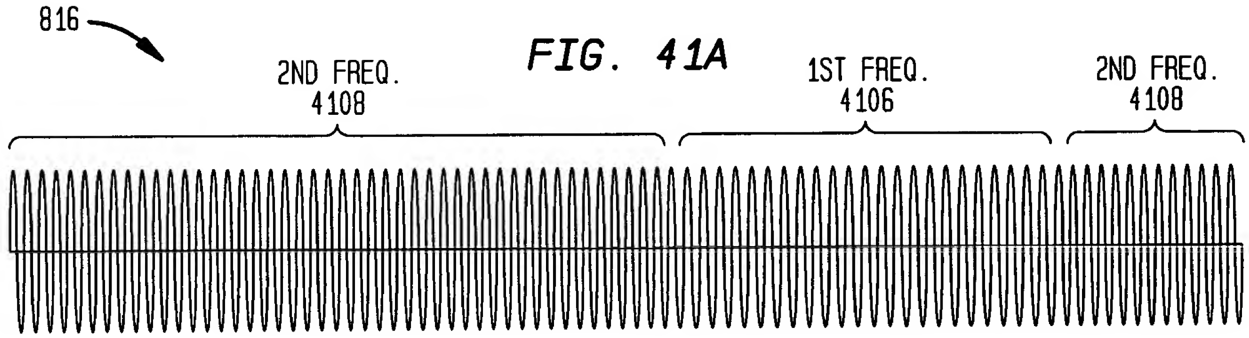

FIG. 41B

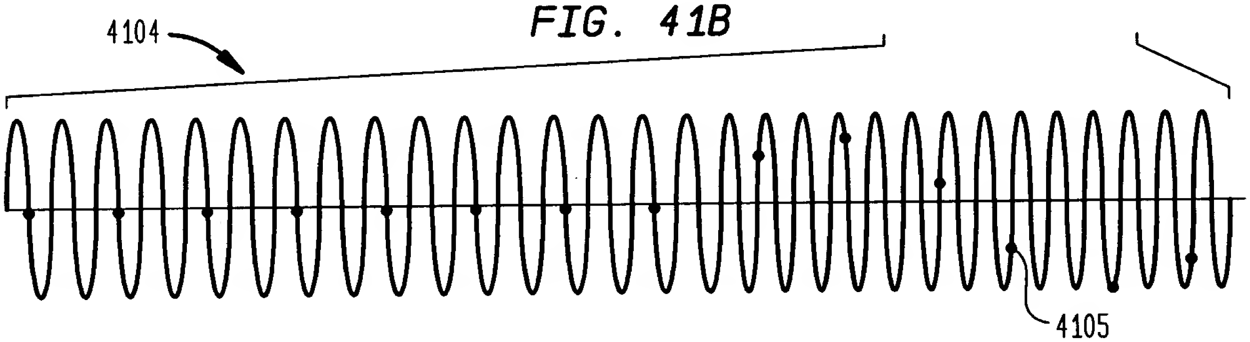

FIG. 41C

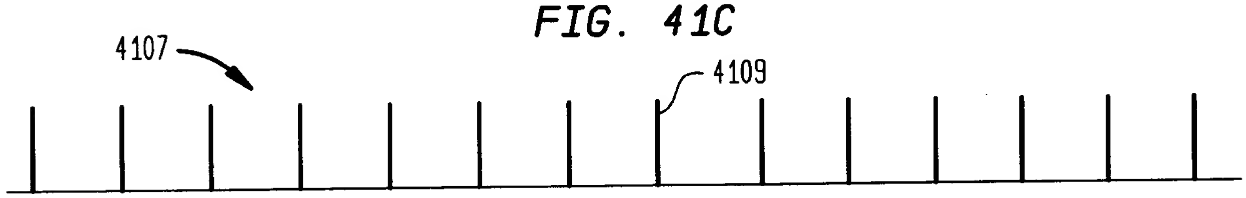

FIG. 41D

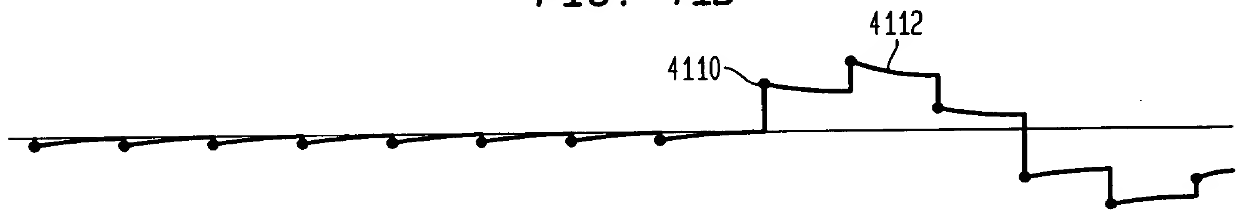

FIG. 41E

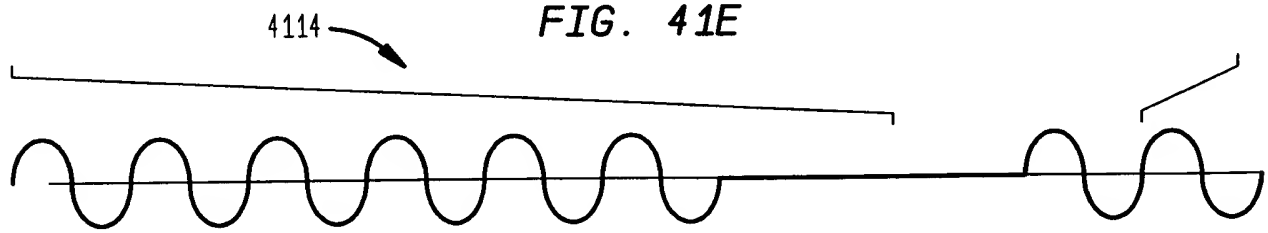

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FIG. 42

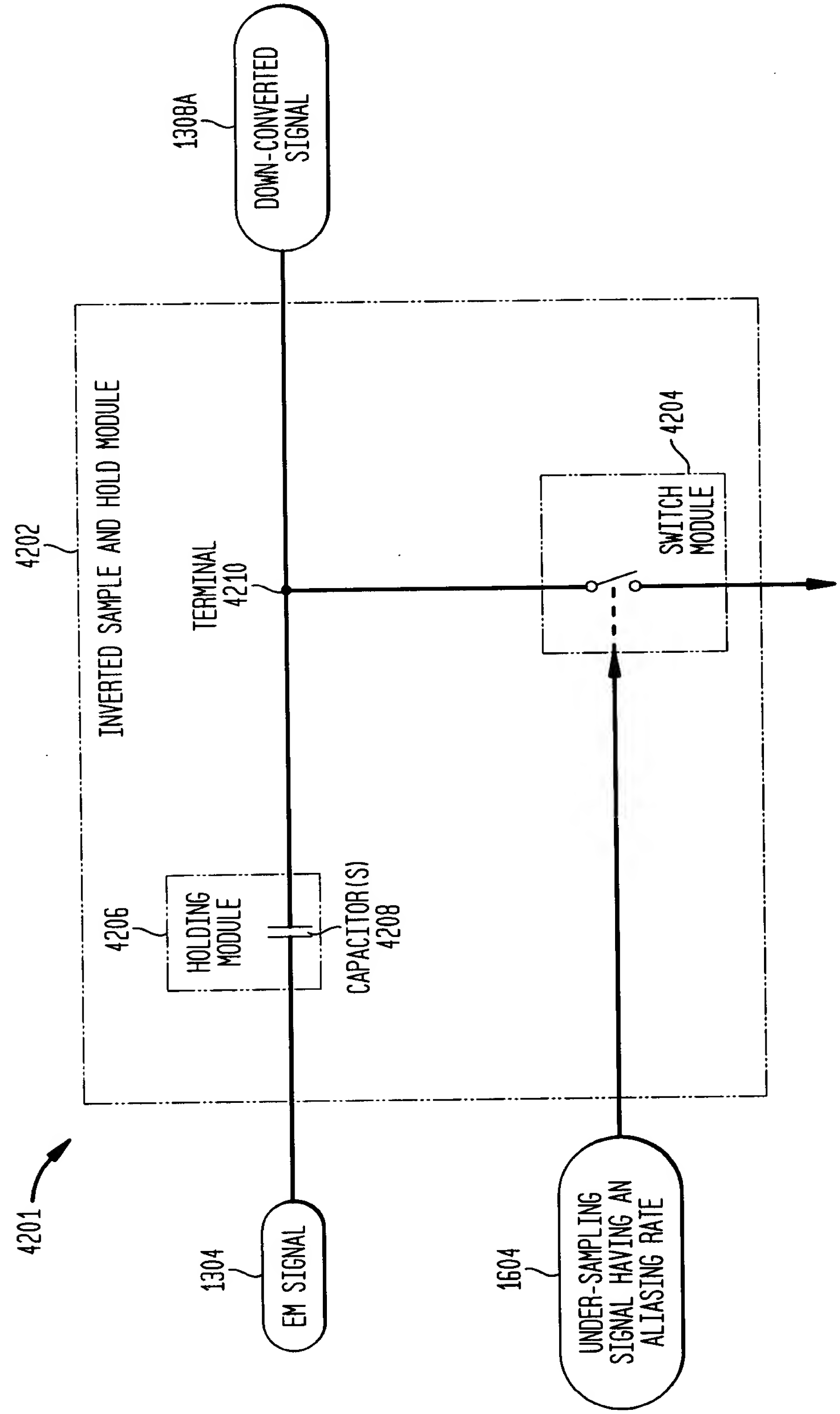

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FIG. 43

$$\Delta q(t) = 2 \cdot C \cdot A \cdot \sin\left(\frac{1}{2} \cdot T\right) \cdot \cos\left(t - \frac{1}{2} \cdot T\right)$$

FIG. 44A

DIFFERENTIAL CONFIGURATION

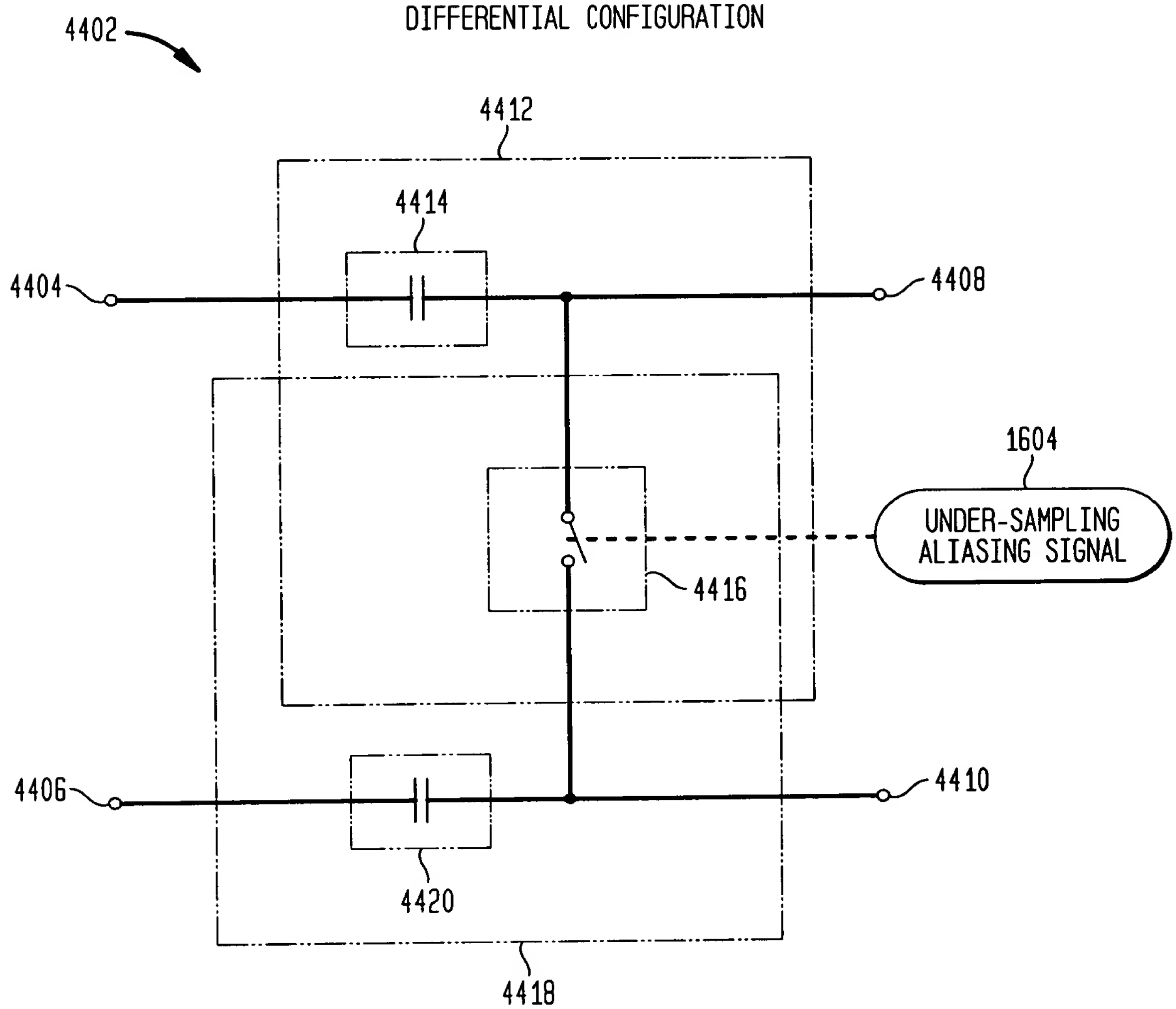

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FIG. 44B

DIFFERENTIAL INPUT TO DIFFERENTIAL OUTPUT

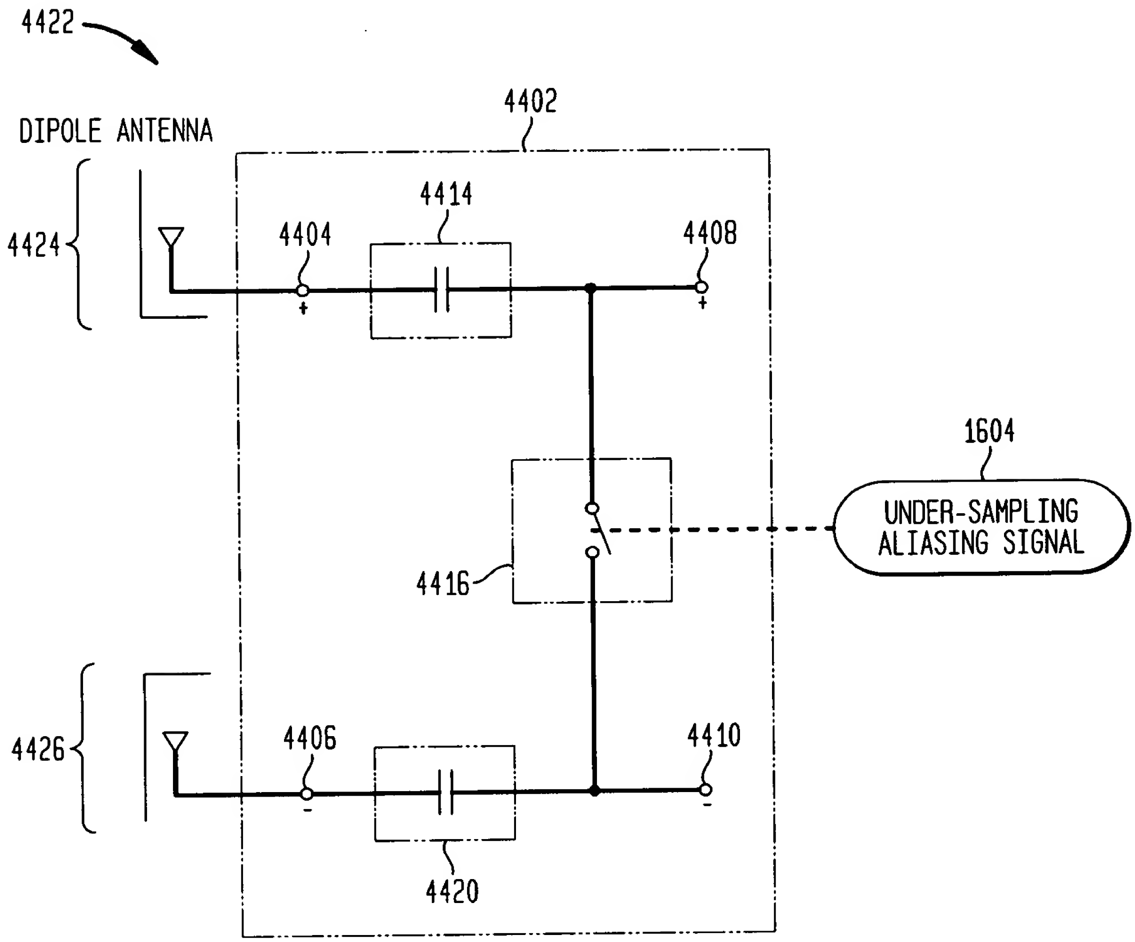

FIG. 44C

SINGLE INPUT TO DIFFERENTIAL OUTPUT

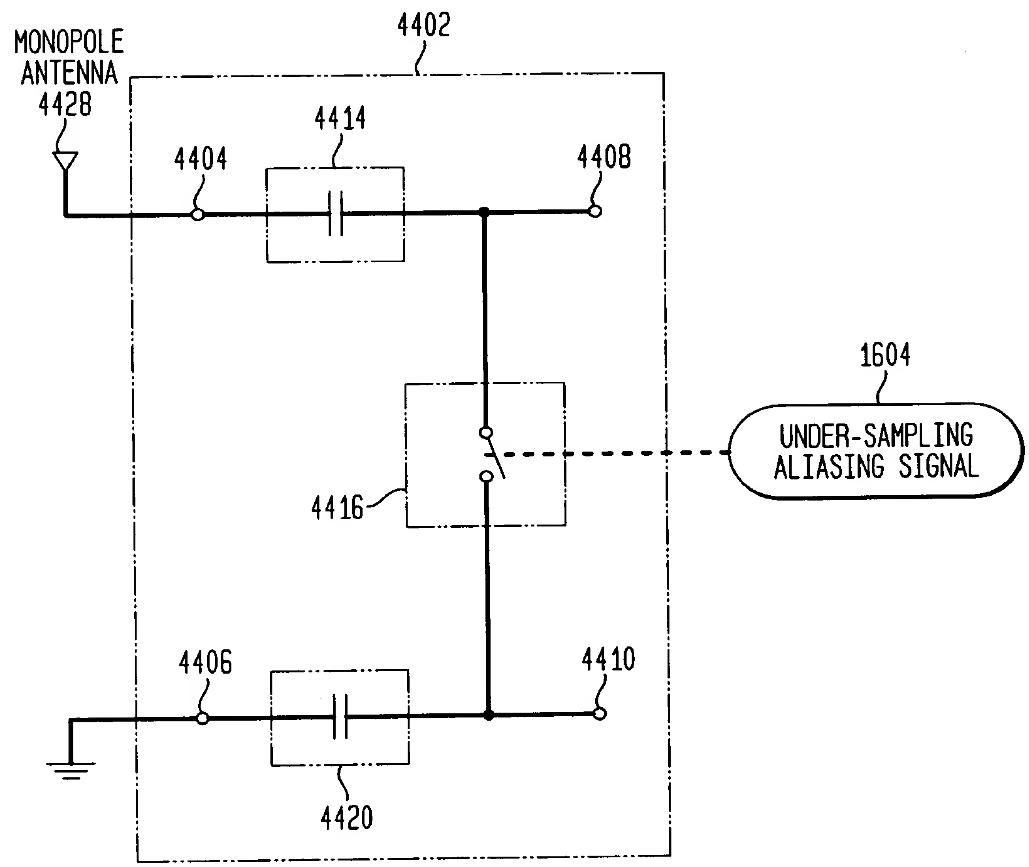

FIG. 44D

DIFFERENTIAL INPUT TO SINGLE OUTPUT

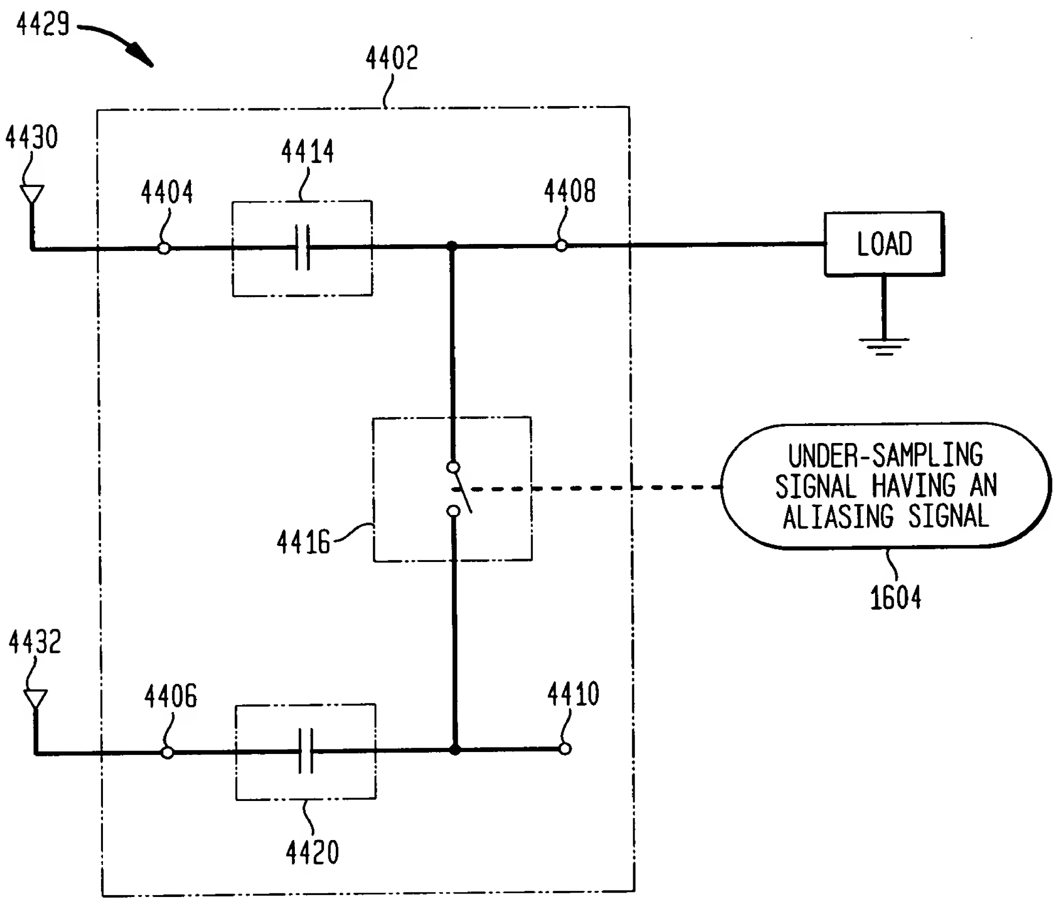

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FIG. 44E

EXAMPLE INPUT/OUTPUT CIRCUITRY

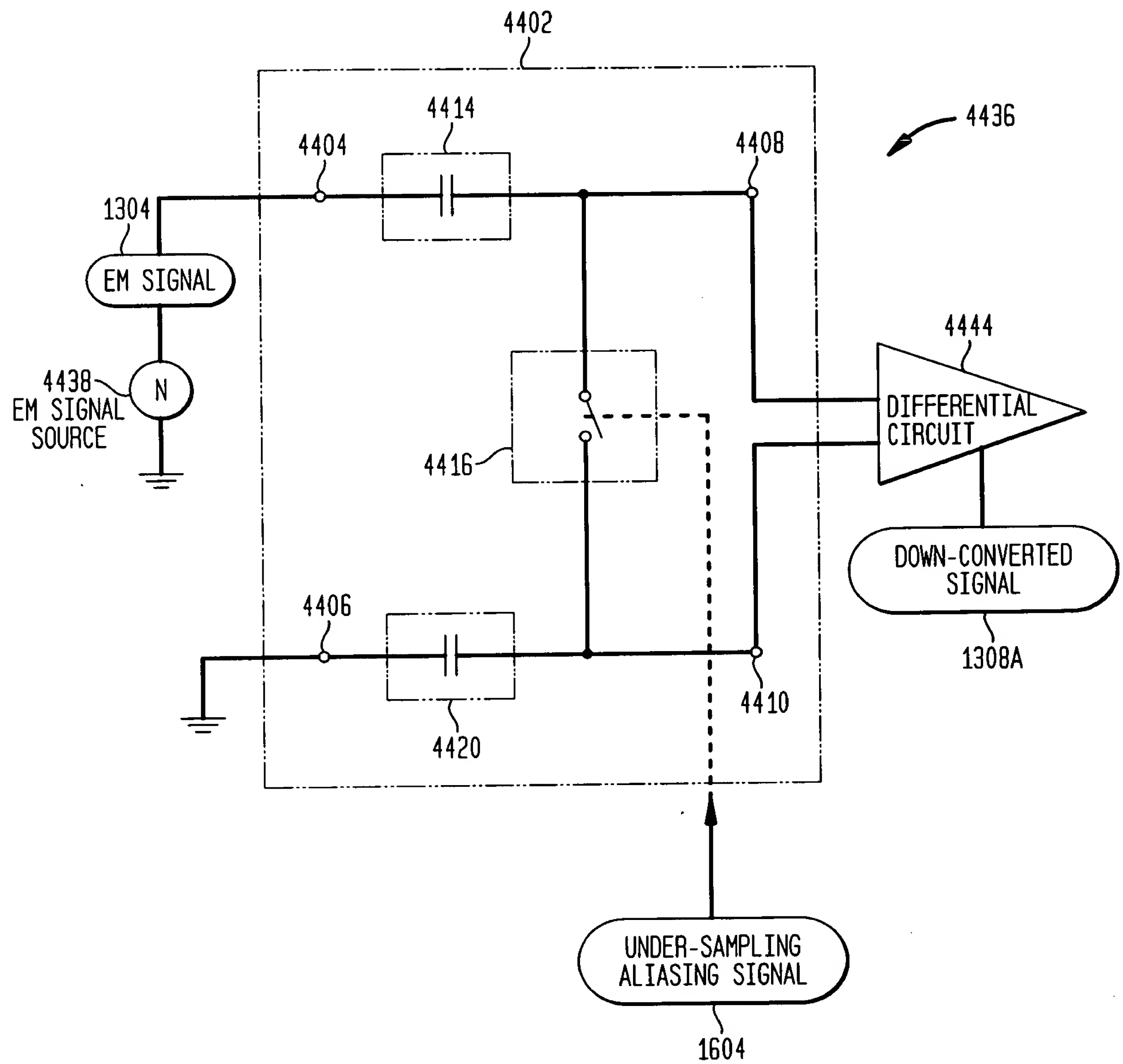

FIG. 45A

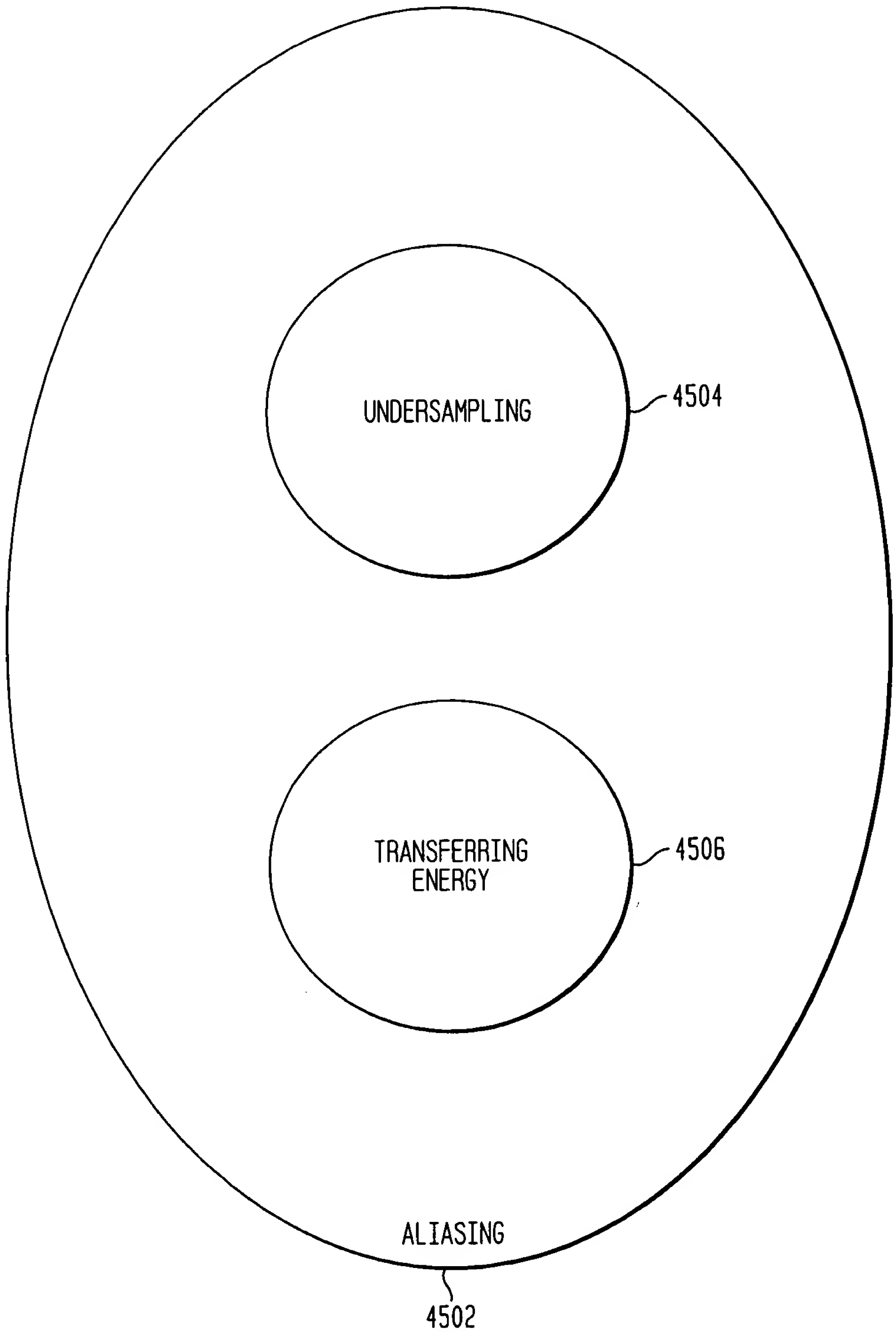
UNDERSAMPLING
4504
TRANSFERRING ENERGY
4506
ALIASING
4502

FIG. 45B

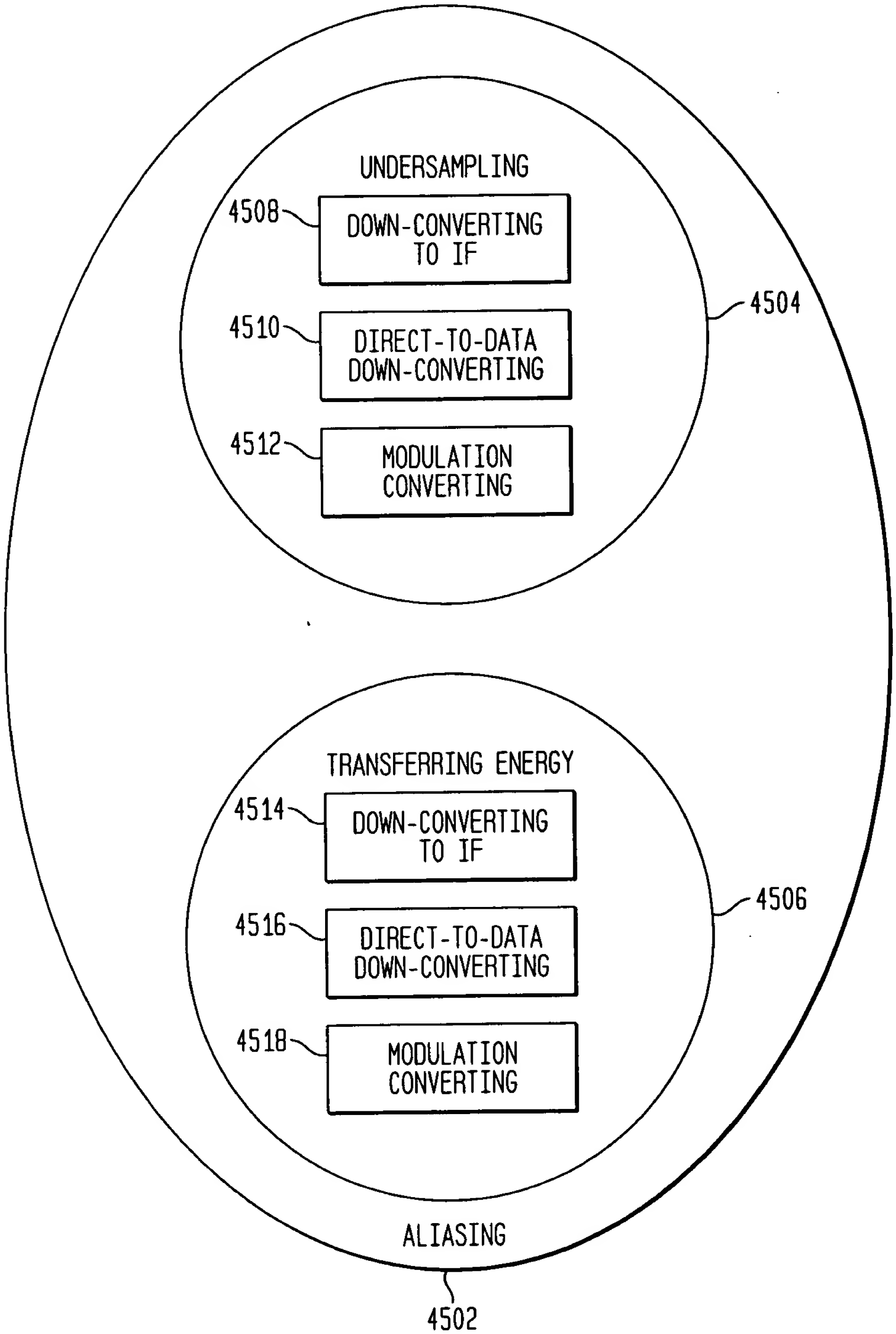
UNDERSAMPLING
4508
DOWN-CONVERTING TO IF
4510
DIRECT-TO-DATA DOWN-CONVERTING
4512
MODULATION CONVERTING
4504
TRANSFERRING ENERGY
4514
DOWN-CONVERTING TO IF
4516
DIRECT-TO-DATA DOWN-CONVERTING
4518
MODULATION CONVERTING
4506
ALIASING
4502

FIG. 46A

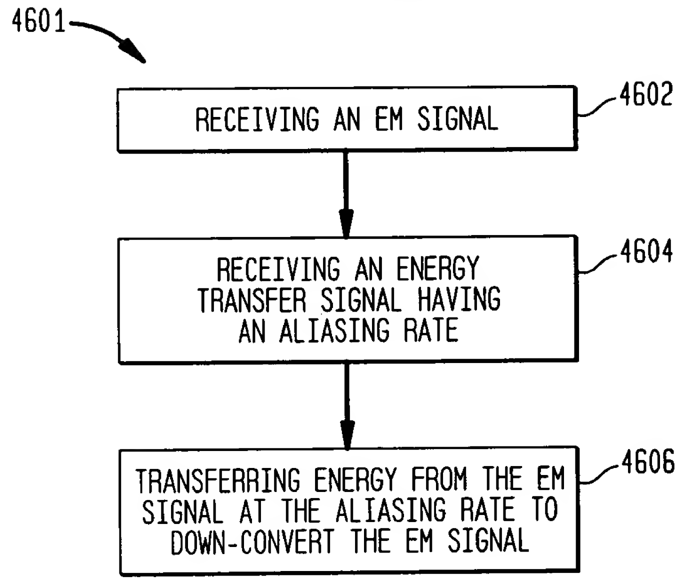

FIG. 46B

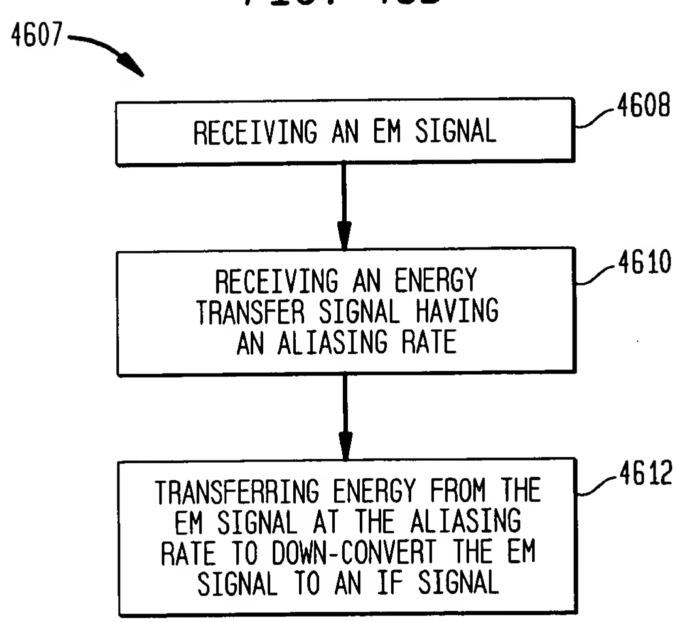

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FIG. 46C

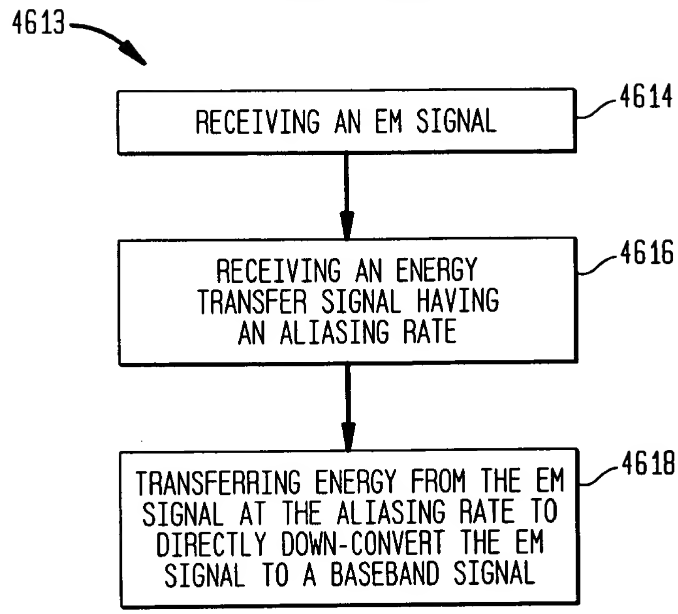

FIG. 46D

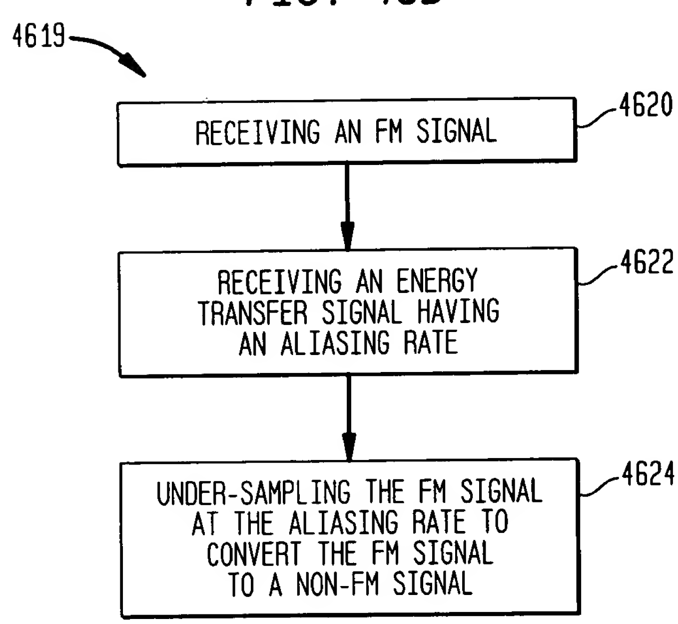

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FIG. 47E

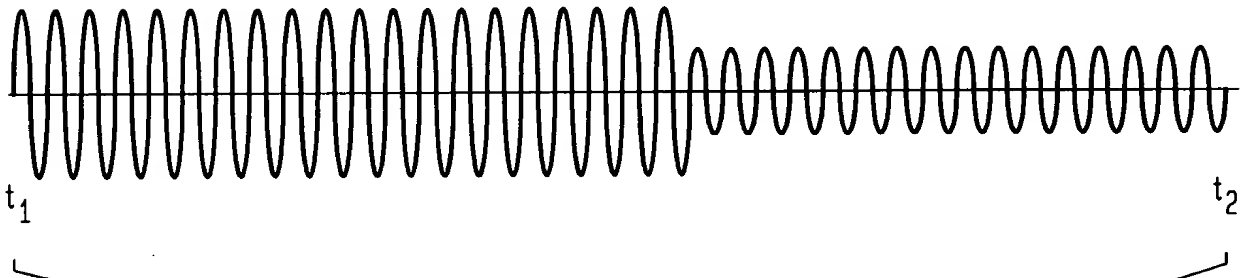

FIG. 47A

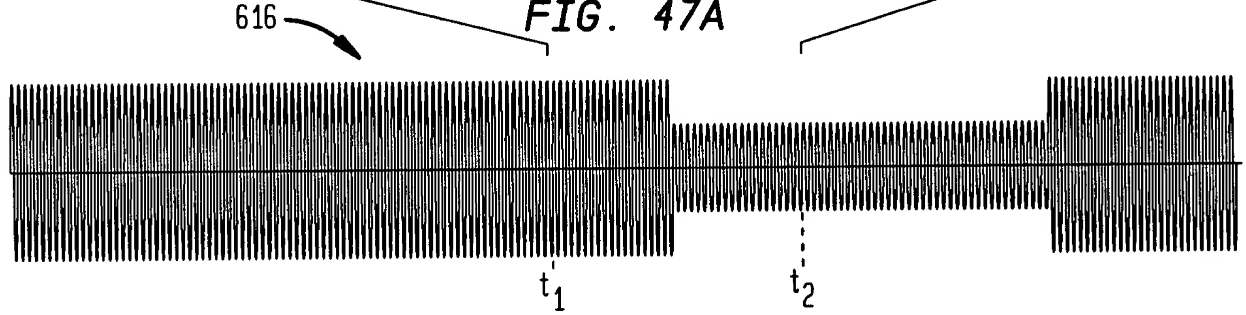

FIG. 47B

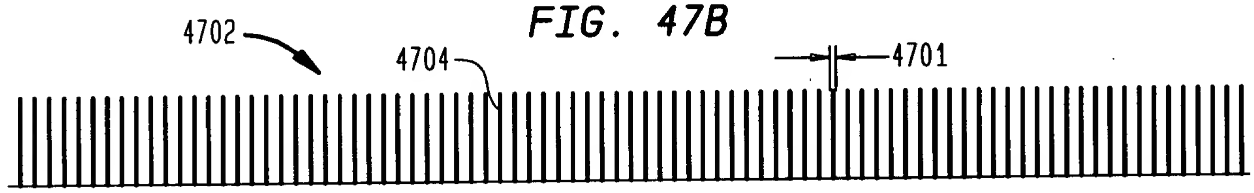

FIG. 47C

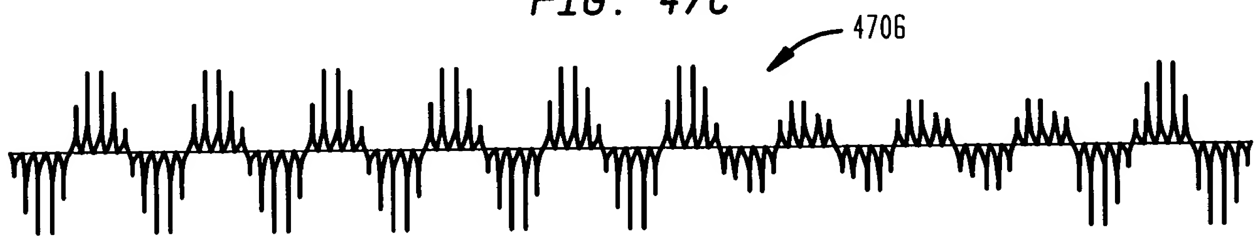

FIG. 47D

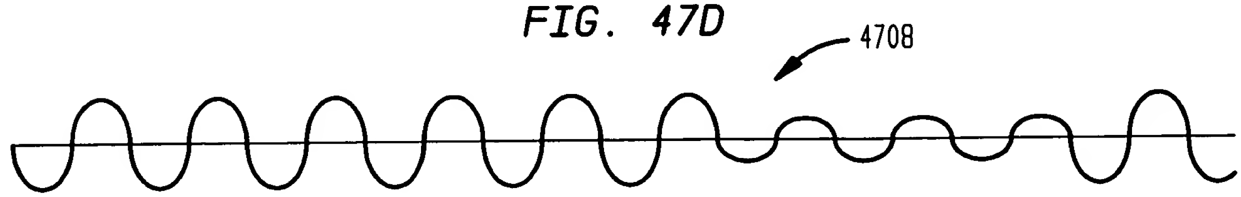

FIG. 48

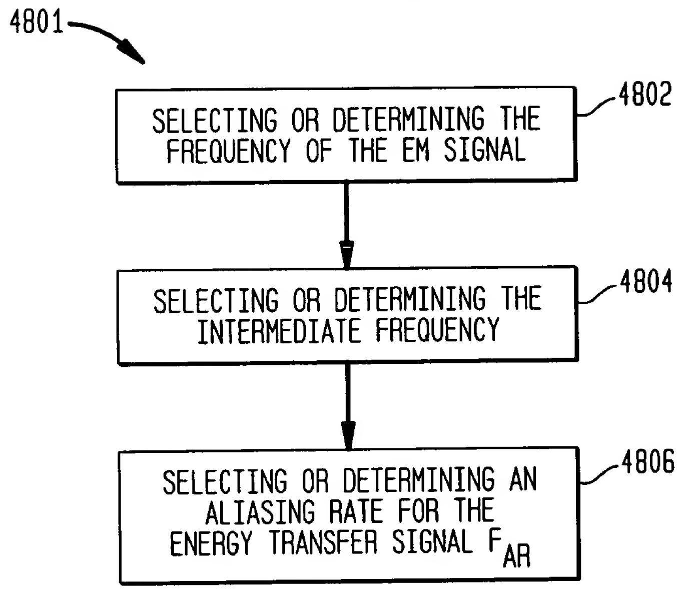
4801
SELECTING OR DETERMINING THE FREQUENCY OF THE EM SIGNAL
4802
SELECTING OR DETERMINING THE INTERMEDIATE FREQUENCY
4804
SELECTING OR DETERMINING AN ALIASING RATE FOR THE ENERGY TRANSFER SIGNAL F_{AR}
4806

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FIG. 49A

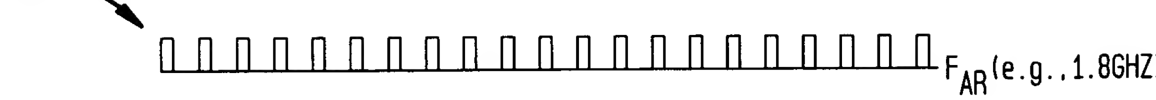

FIG. 49B

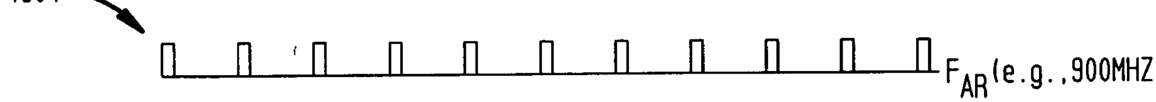

FIG. 49C

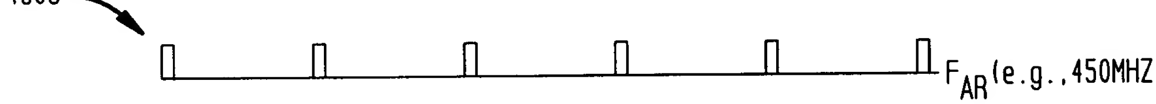

FIG. 49D

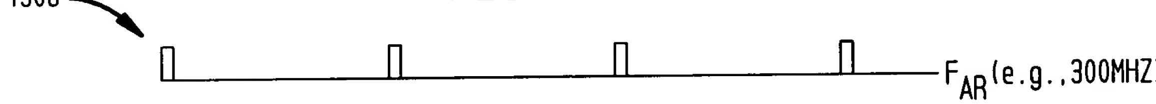

FIG. 49E

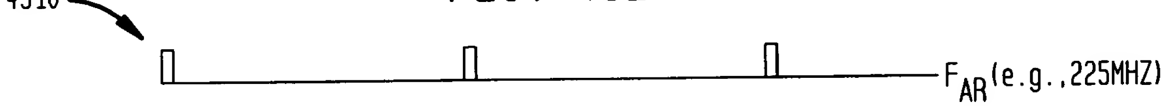

FIG. 49F

FIG. 49G

FIG. 49H

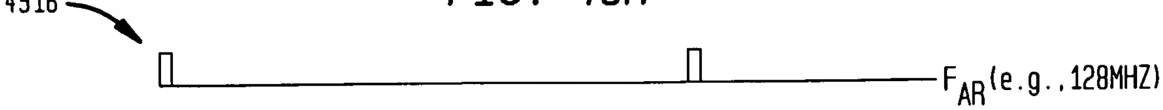

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FIG. 50A

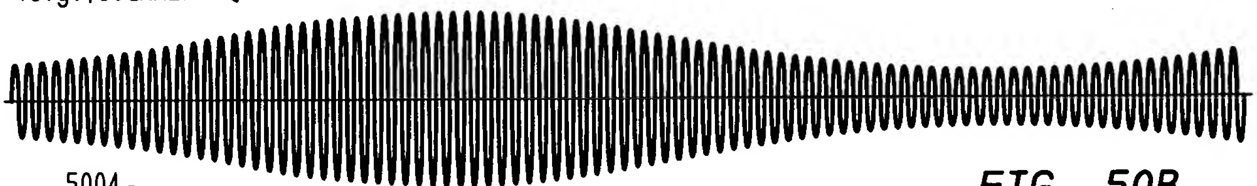

FIG. 50B

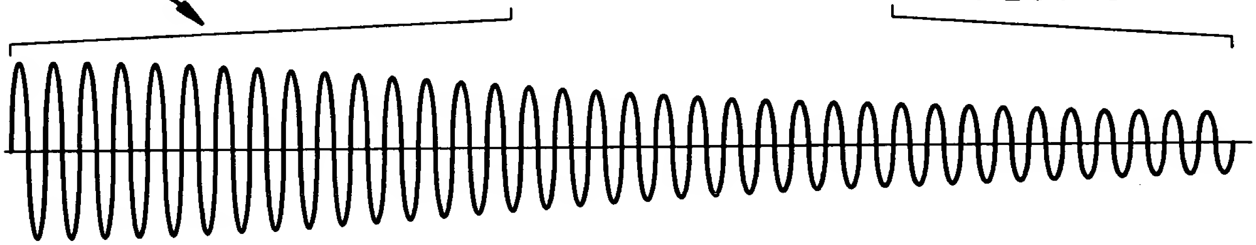

FIG. 50D

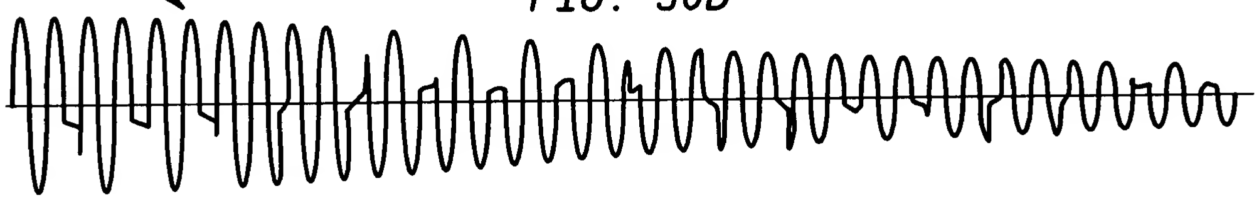

FIG. 50C

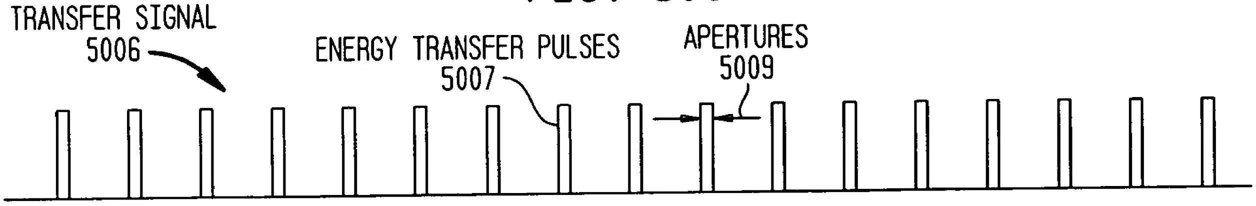

FIG. 50E

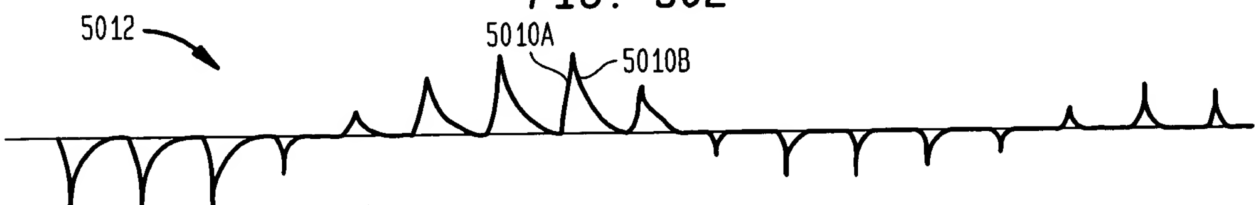

FIG. 50F

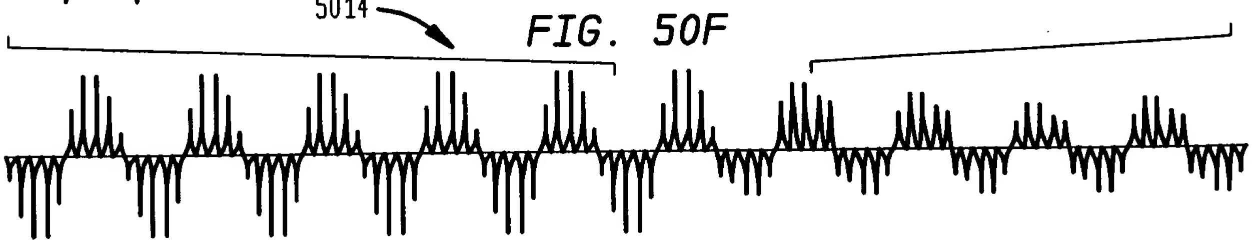

FIG. 50G

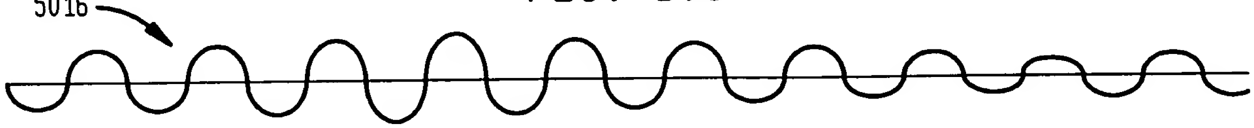

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FIG. 51A

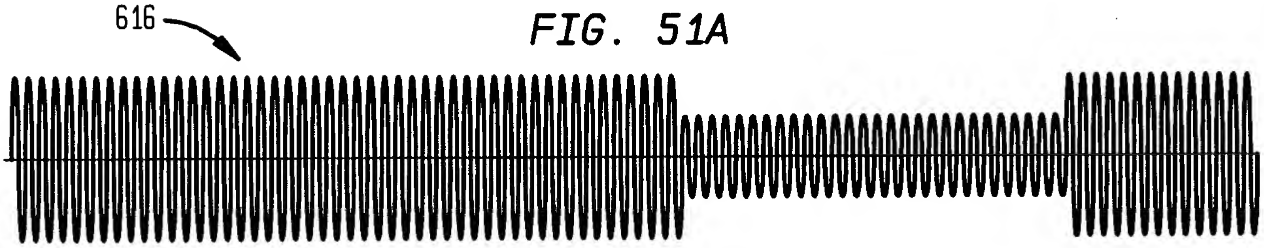

FIG. 51B

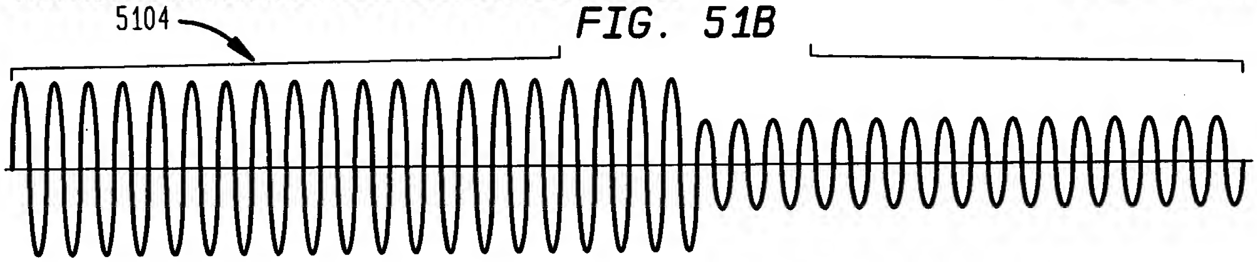

FIG. 51D

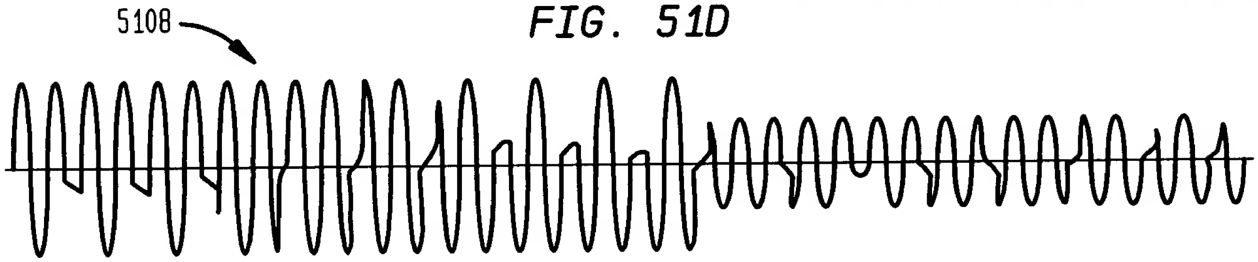

FIG. 51C

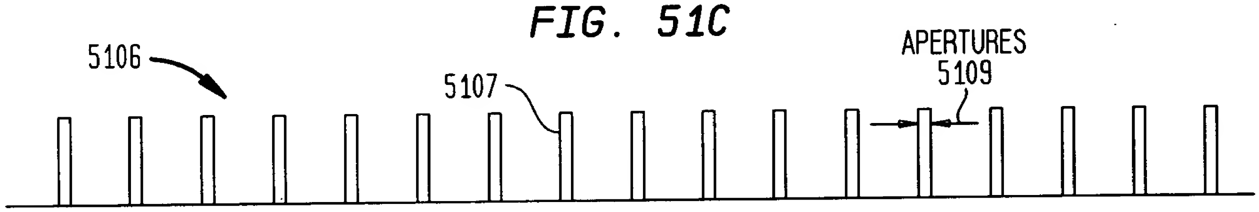

FIG. 51E

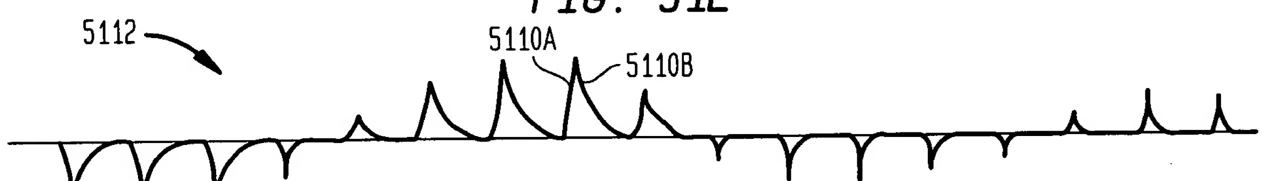

FIG. 51F

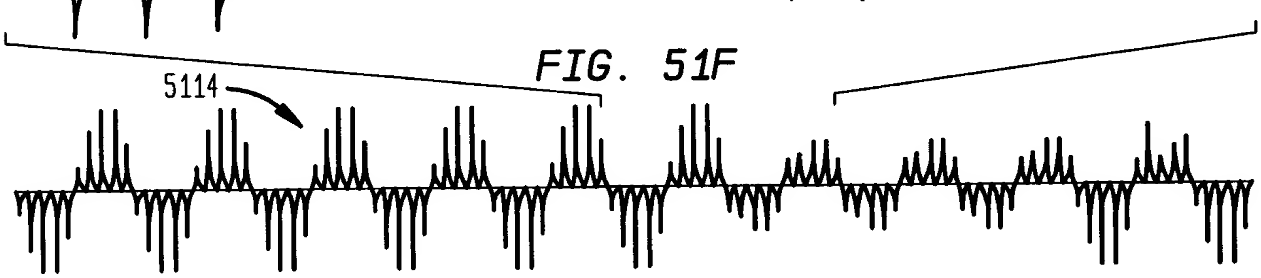

FIG. 51G

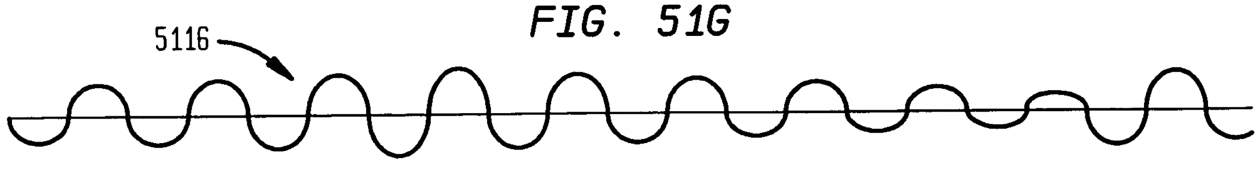

FIG. 52A

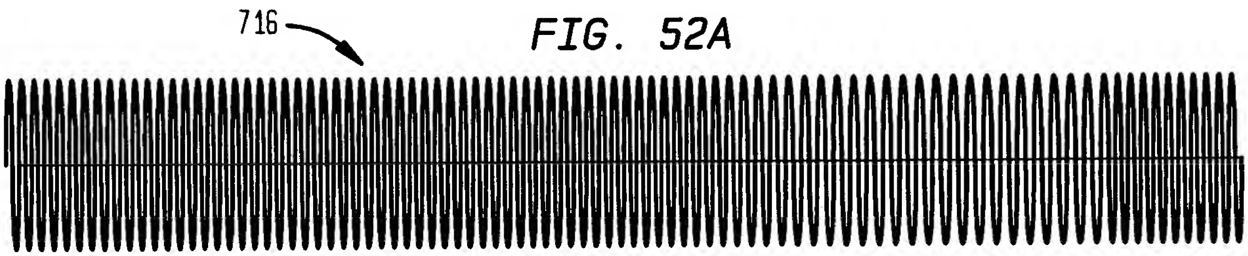

FIG. 52B

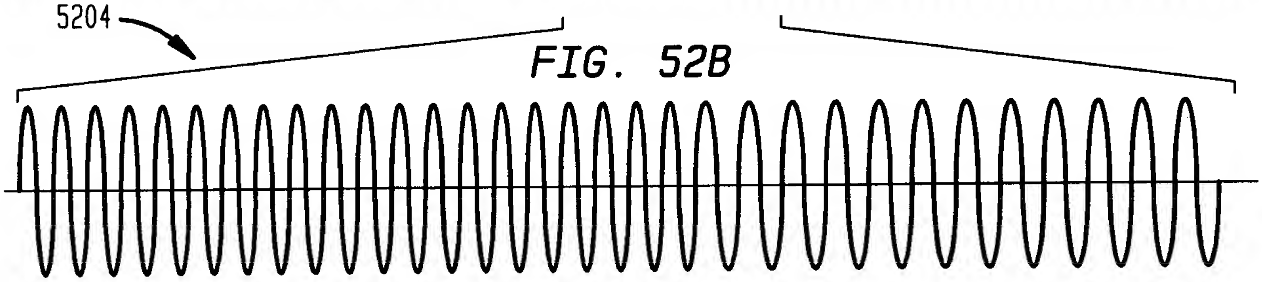

FIG. 52D

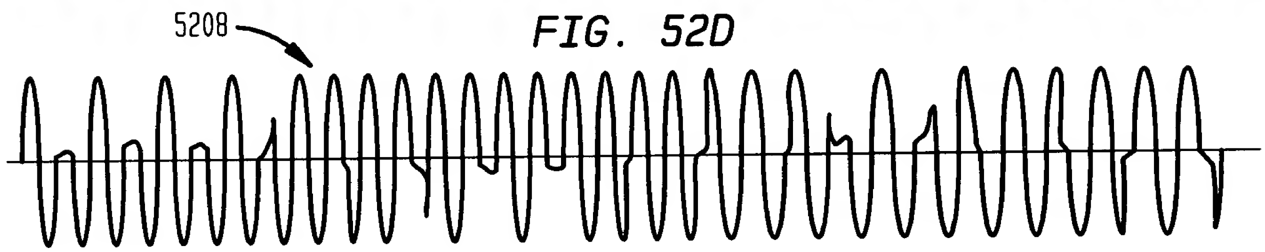

FIG. 52C

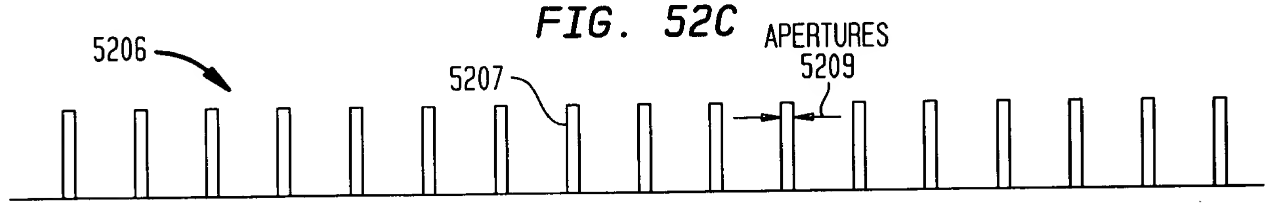

FIG. 52E

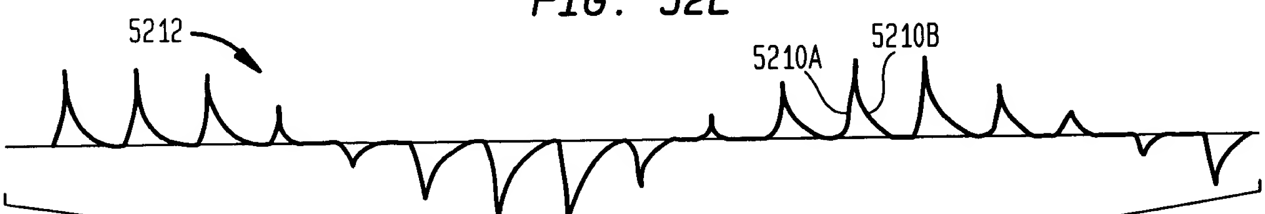

FIG. 52F

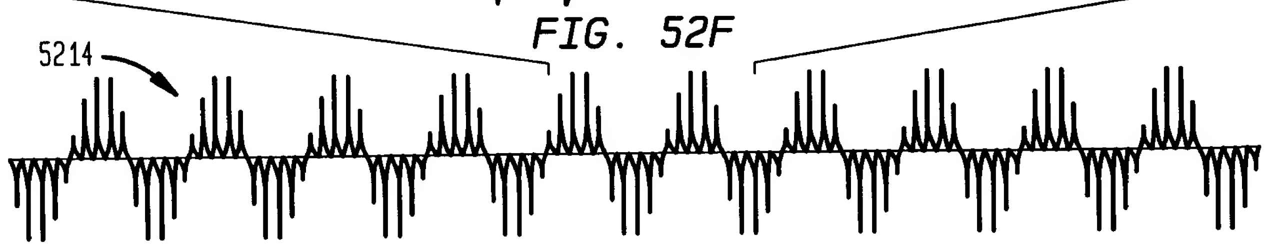

FIG. 52G

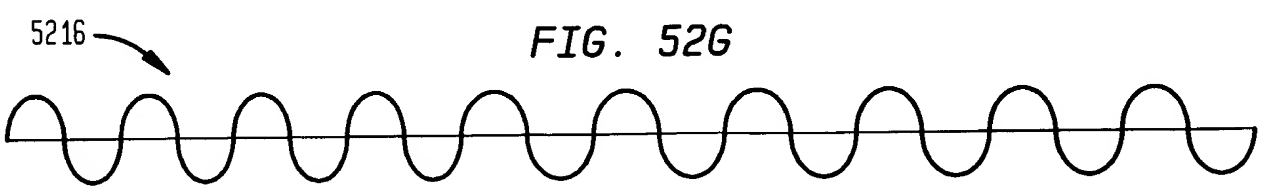

FIG. 53A

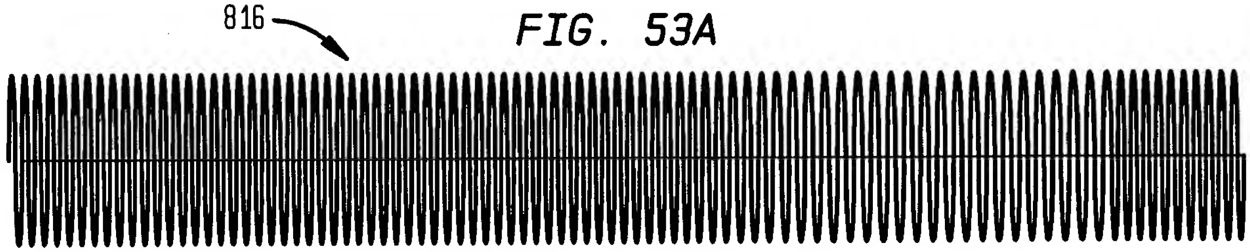

FIG. 53B

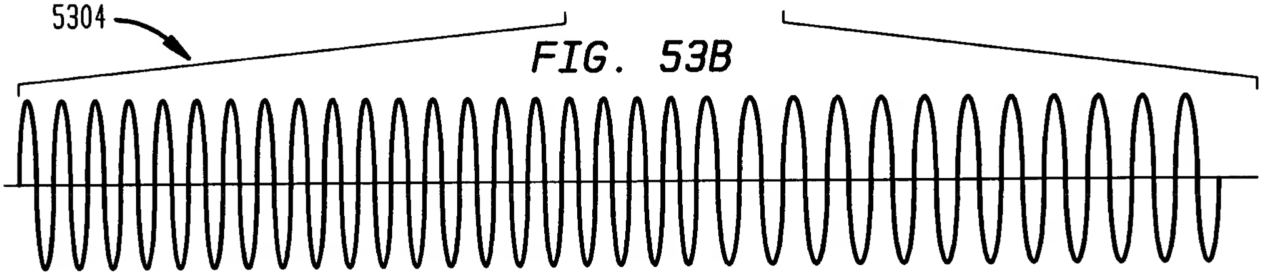

FIG. 53D

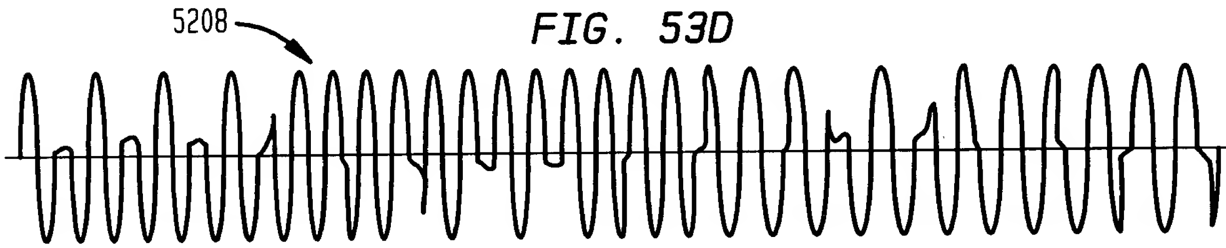

FIG. 53C

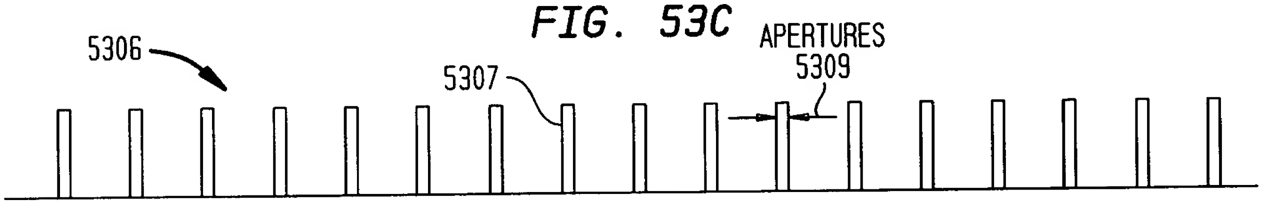

FIG. 53E

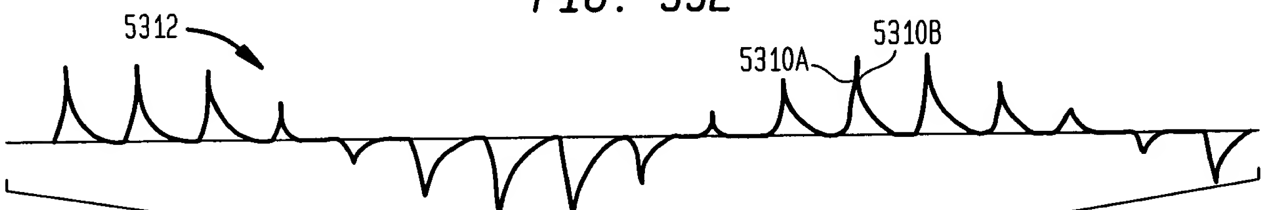

FIG. 53F

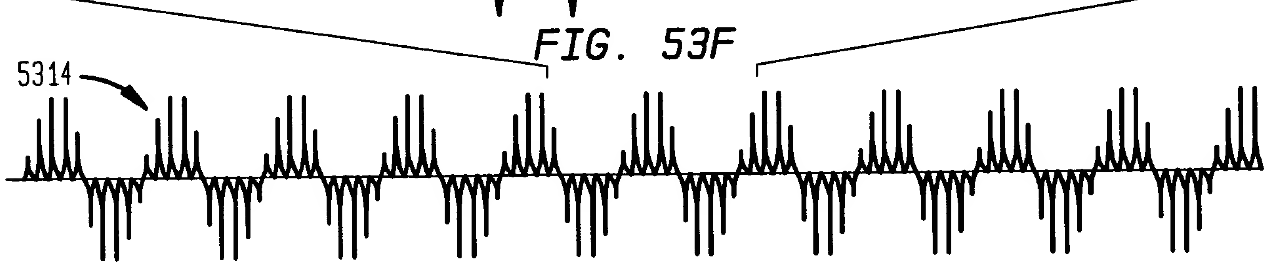

FIG. 53G

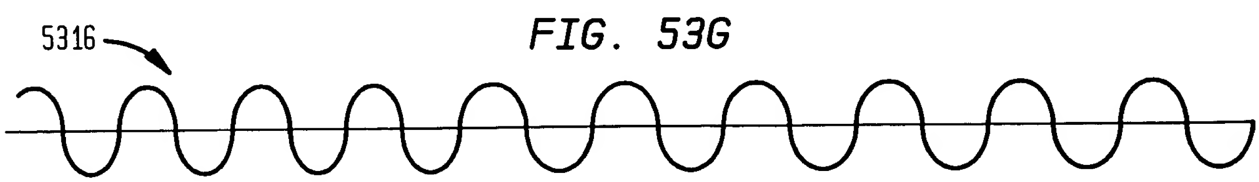

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FIG. 54A

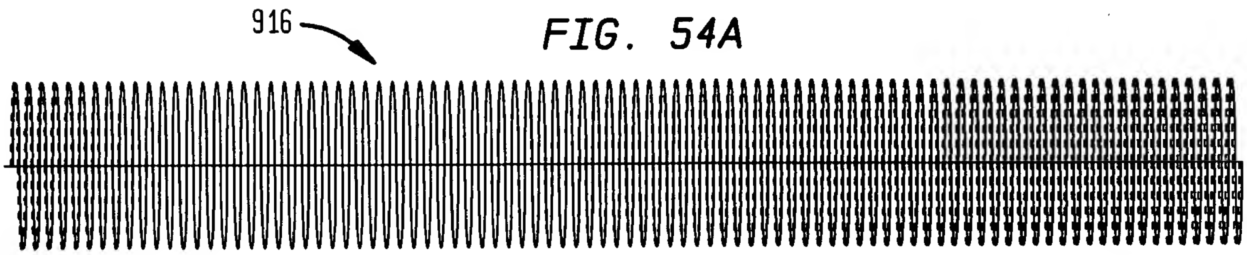

FIG. 54B

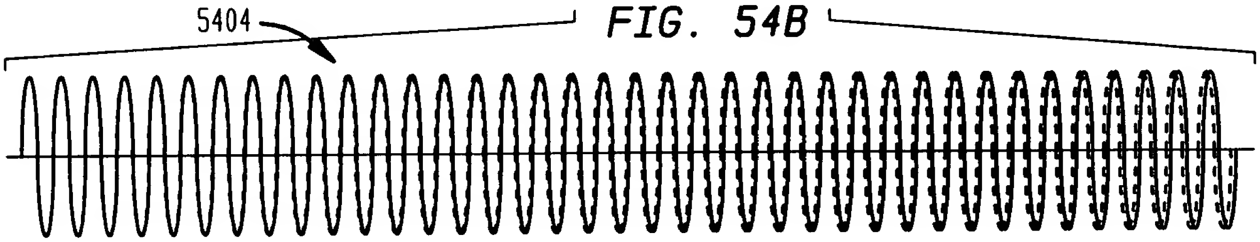

FIG. 54D

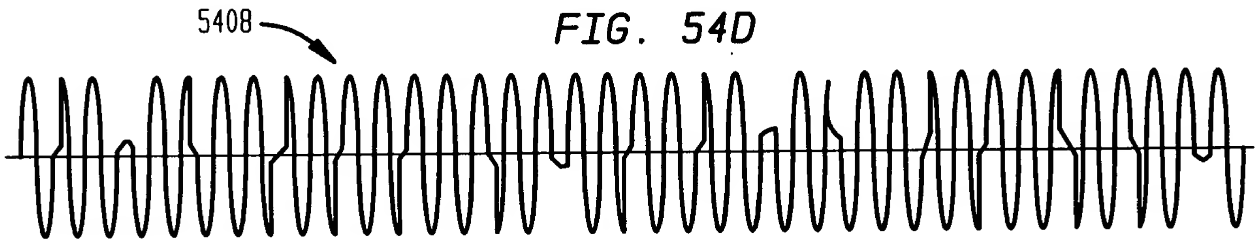

FIG. 54C

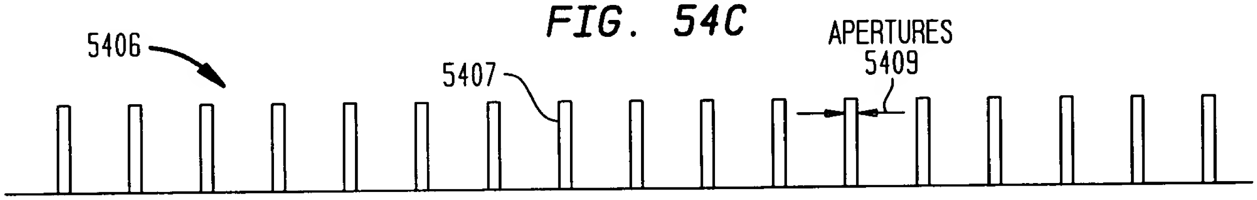

FIG. 54E

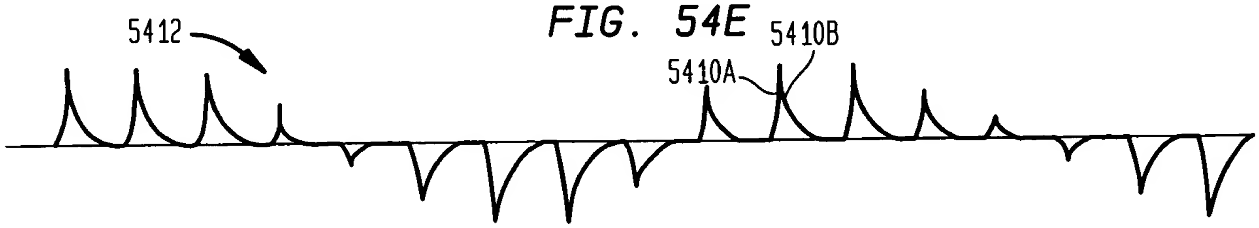

FIG. 54F

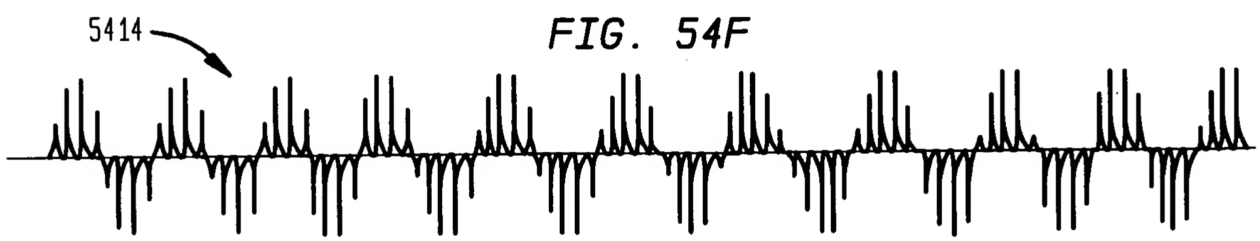

FIG. 54G

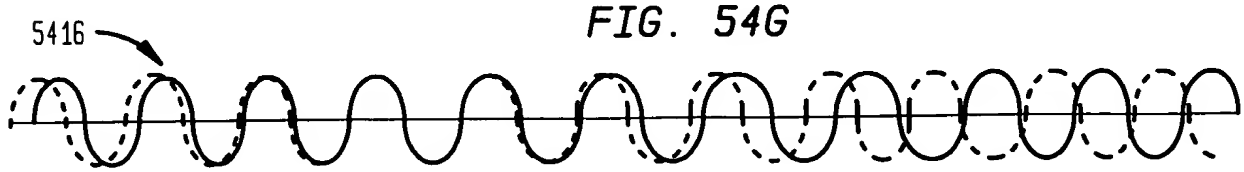

FIG. 55A

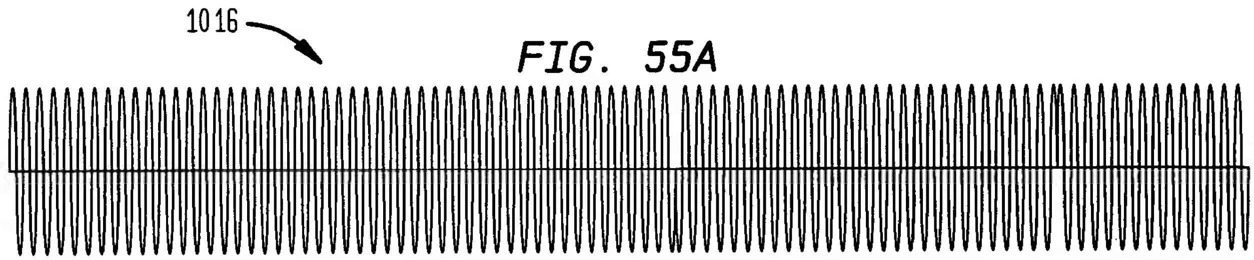

FIG. 55B

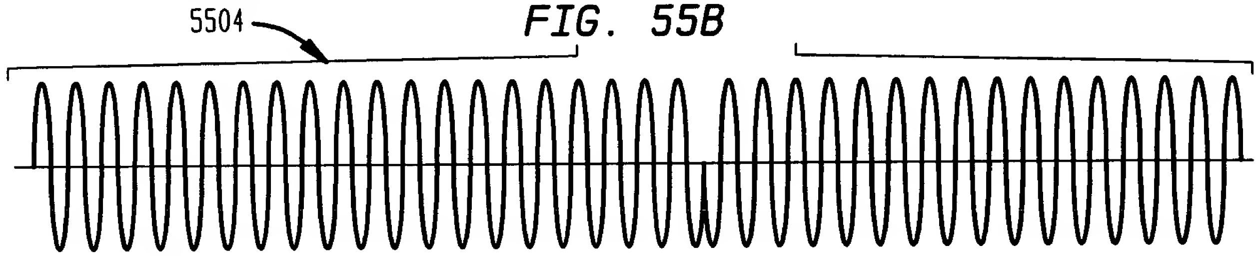

FIG. 55D

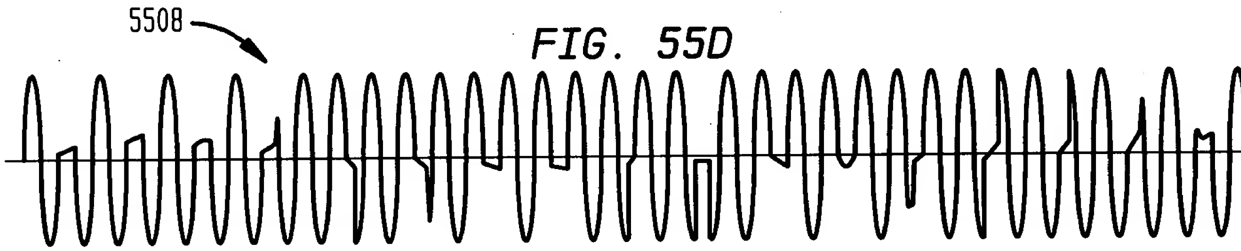

FIG. 55C

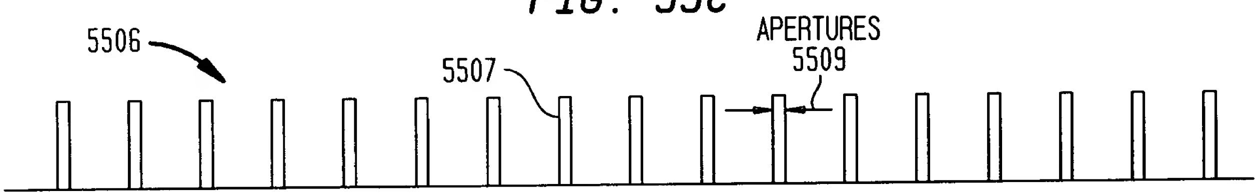

FIG. 55E

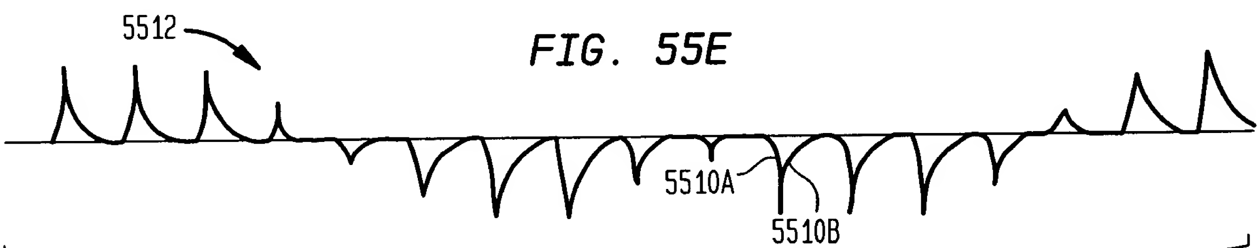

FIG. 55F

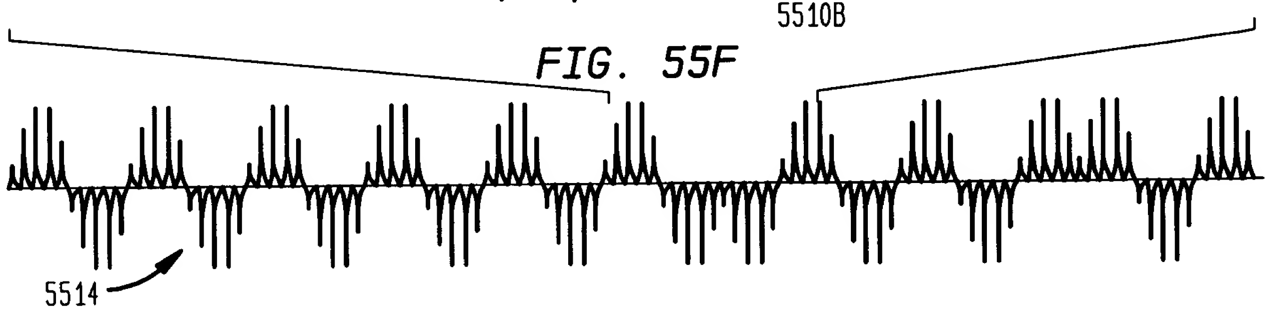

FIG. 55G

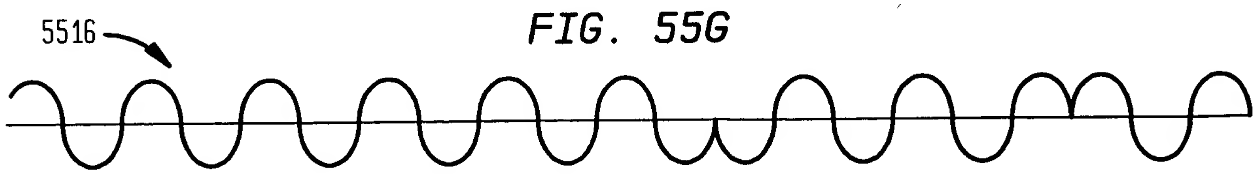

FIG. 56A

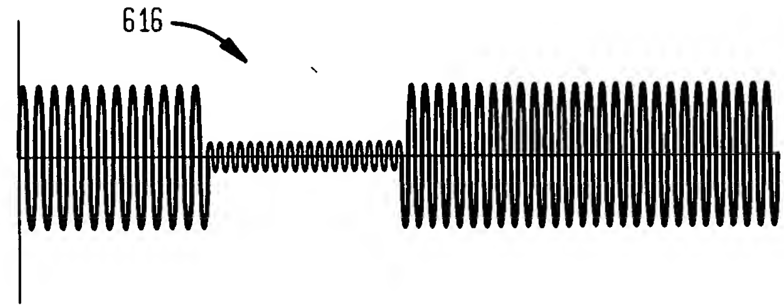

FIG. 56B

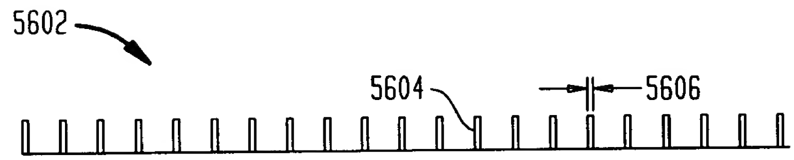

FIG. 56C

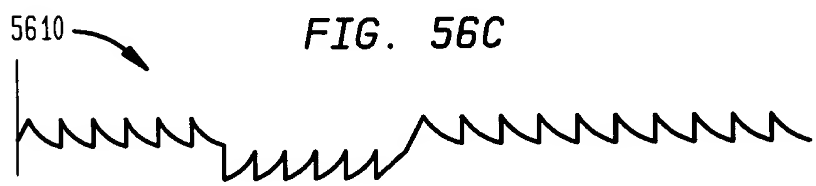

FIG. 56D

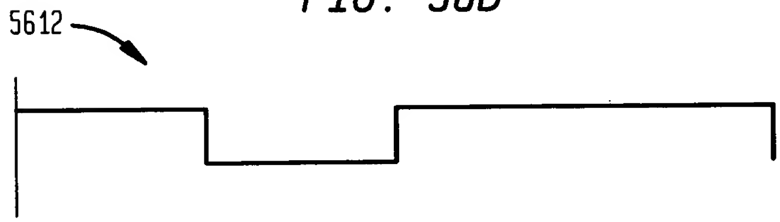

FIG. 57A

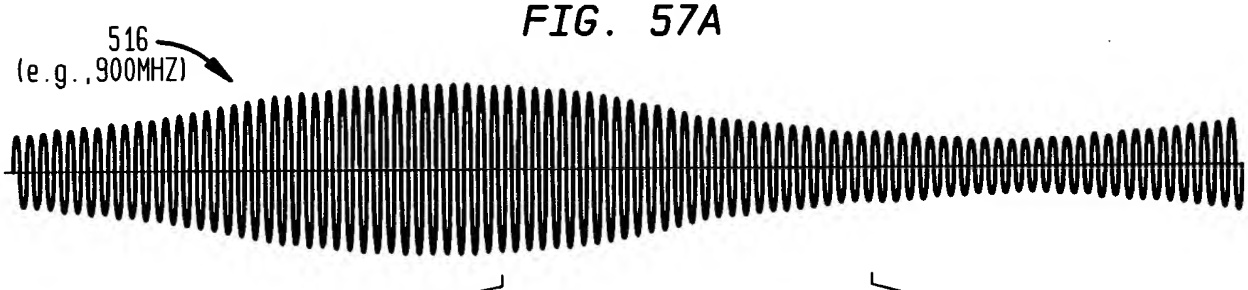

FIG. 57B

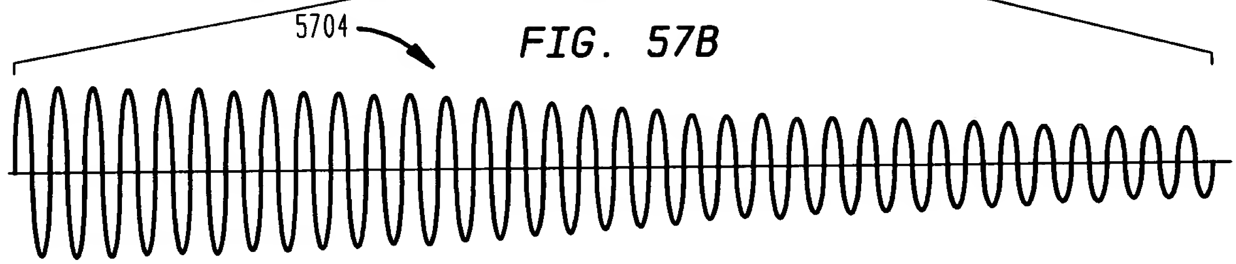

FIG. 57D

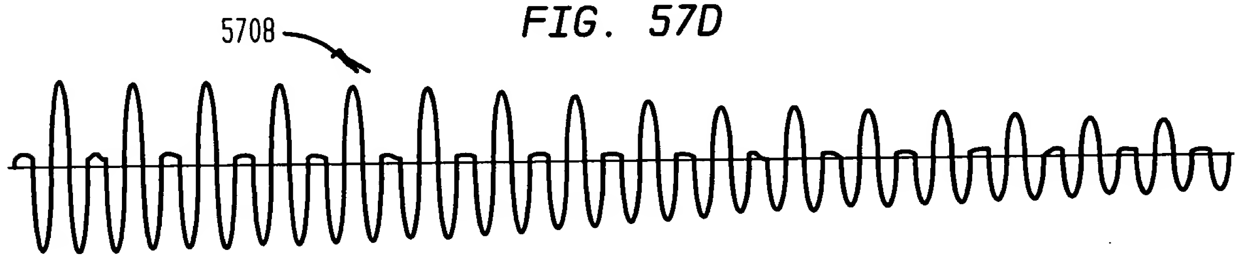

FIG. 57C

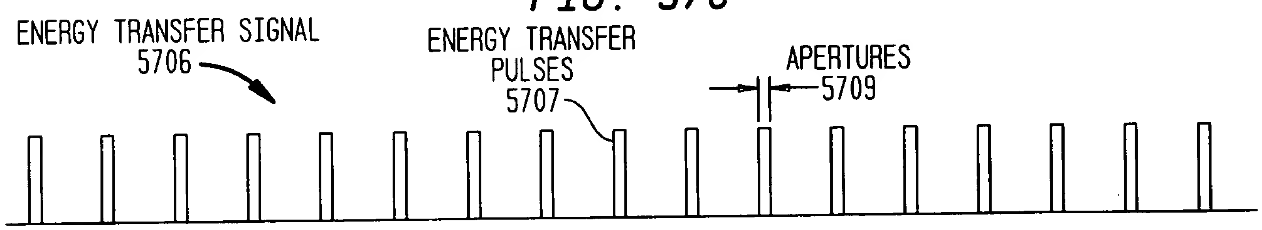

FIG. 57E

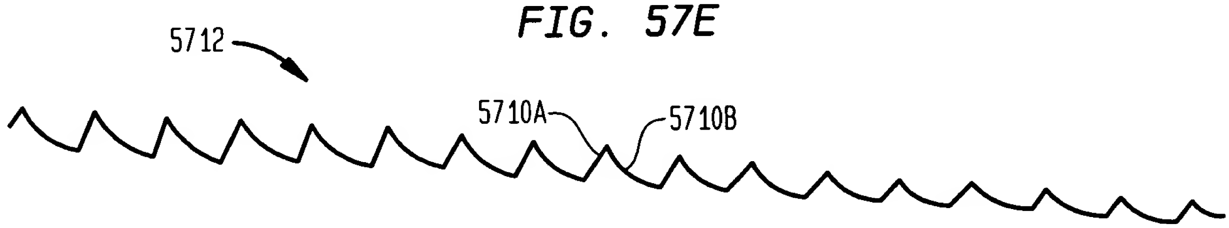

FIG. 57F

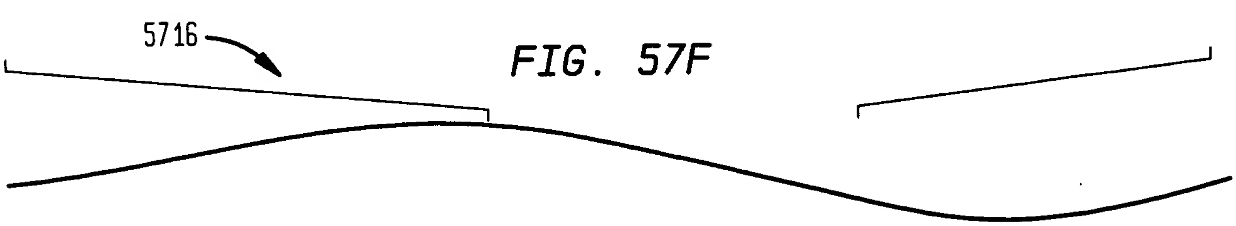

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FIG. 58A

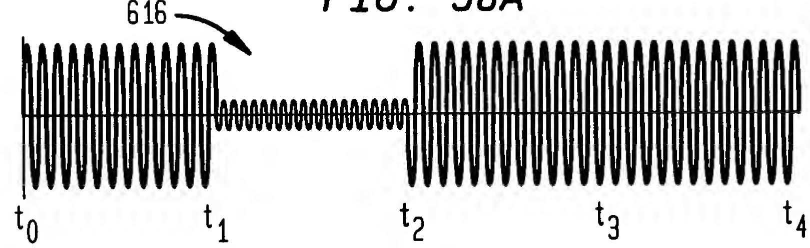

FIG. 58B

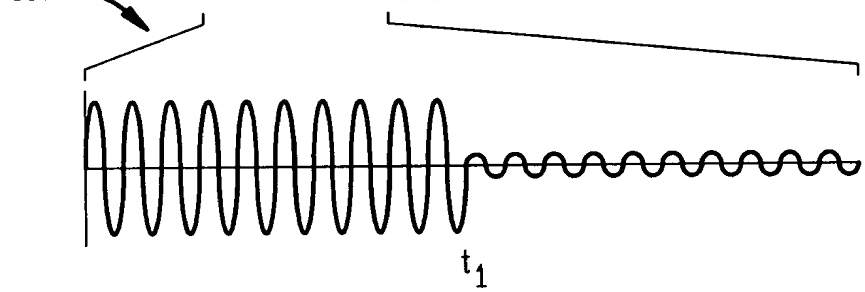

FIG. 58D

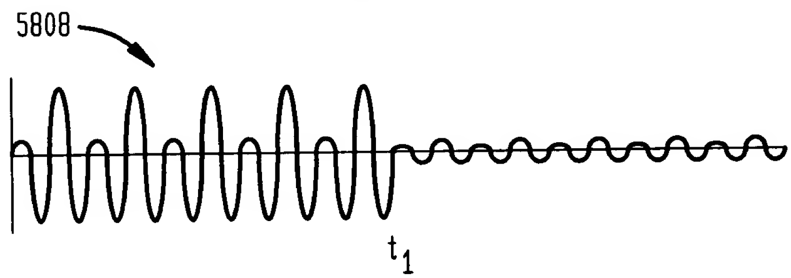

FIG. 58C

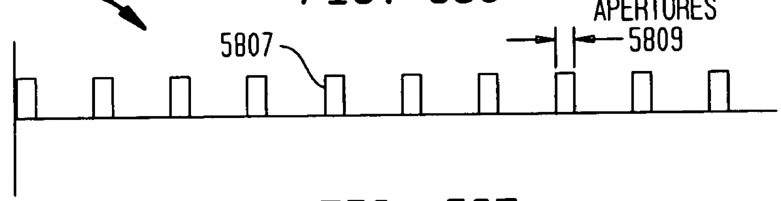

FIG. 58E

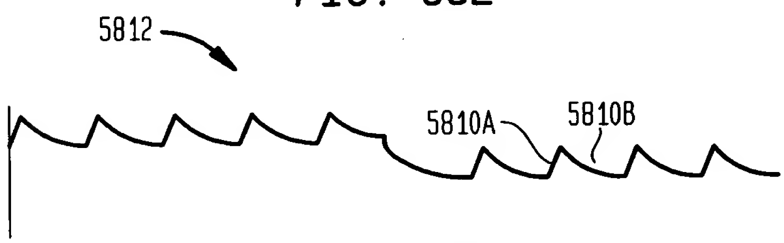

FIG. 58F

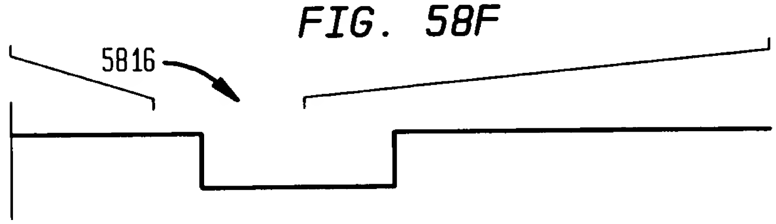

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FIG. 59A

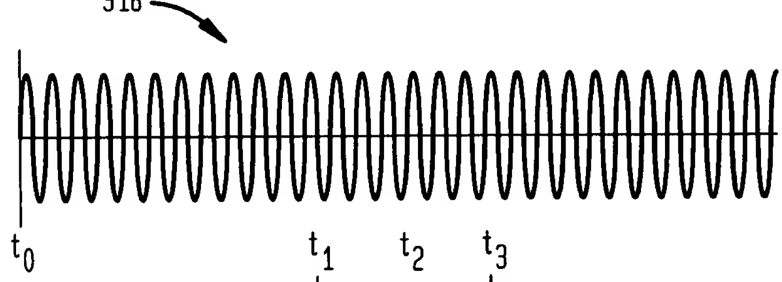

FIG. 59B

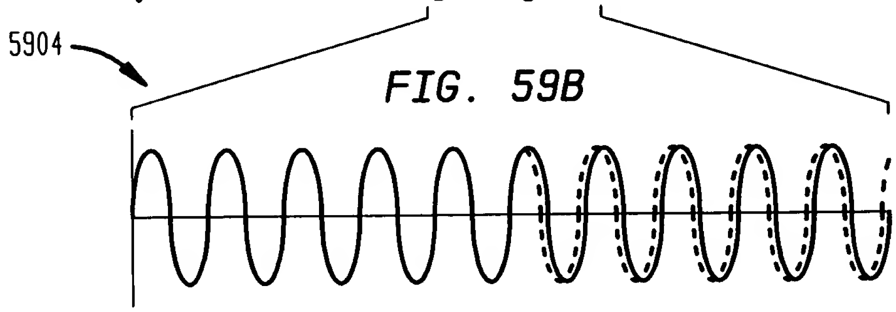

FIG. 59D

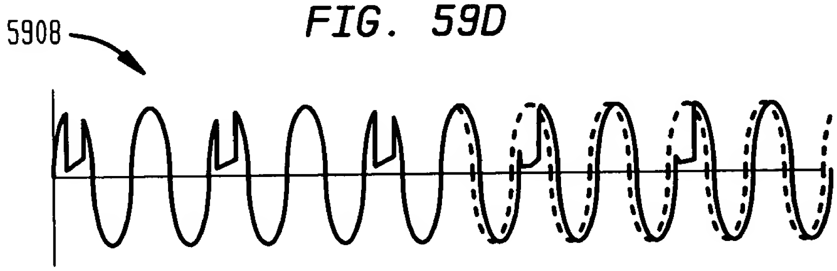

FIG. 59C

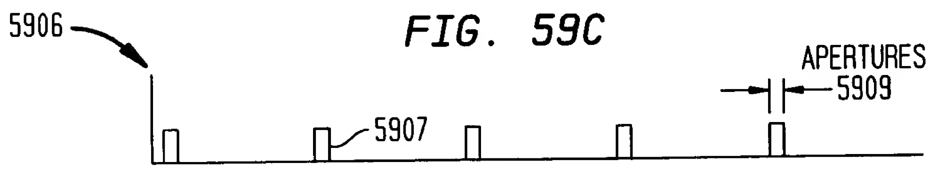

FIG. 59E

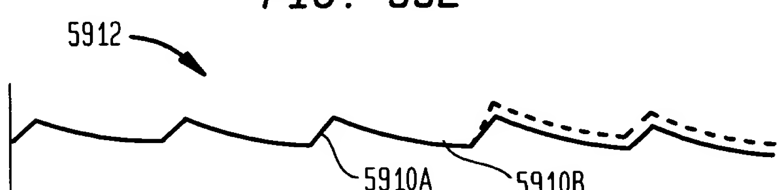

FIG. 59F

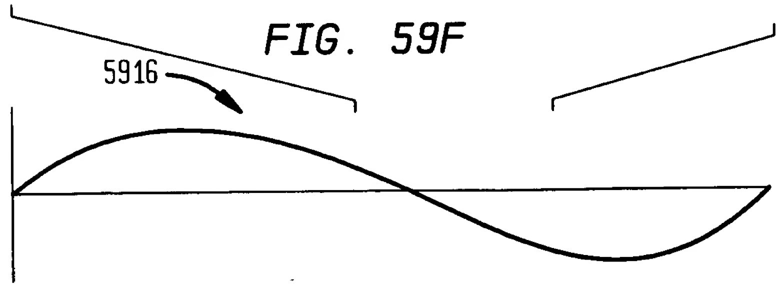

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FIG. 60A

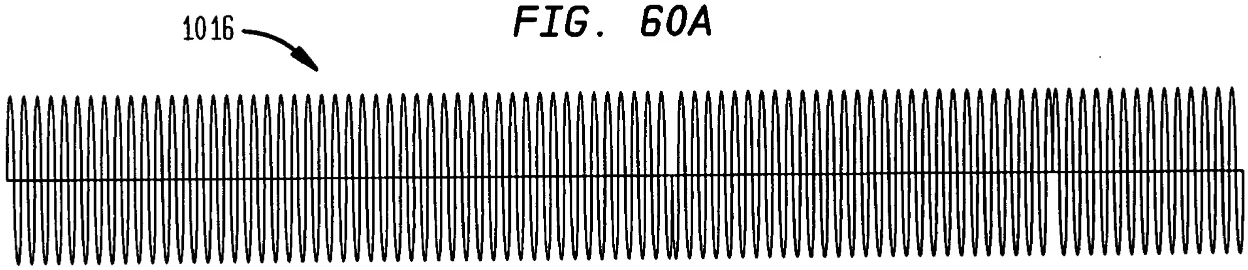

FIG. 60B

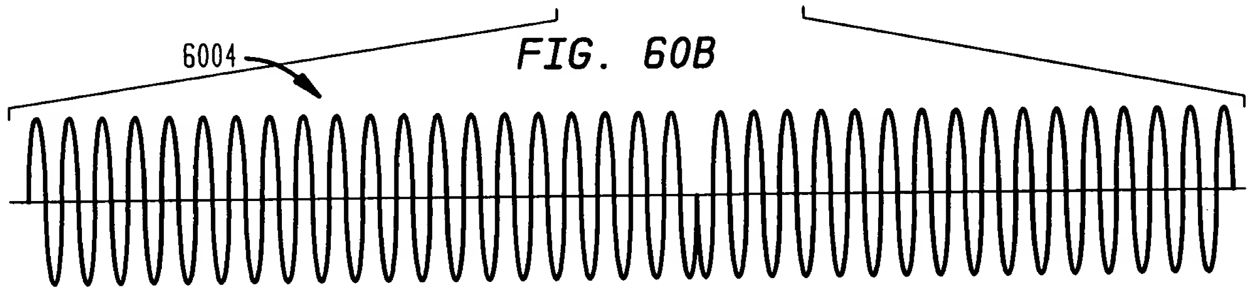

FIG. 60D

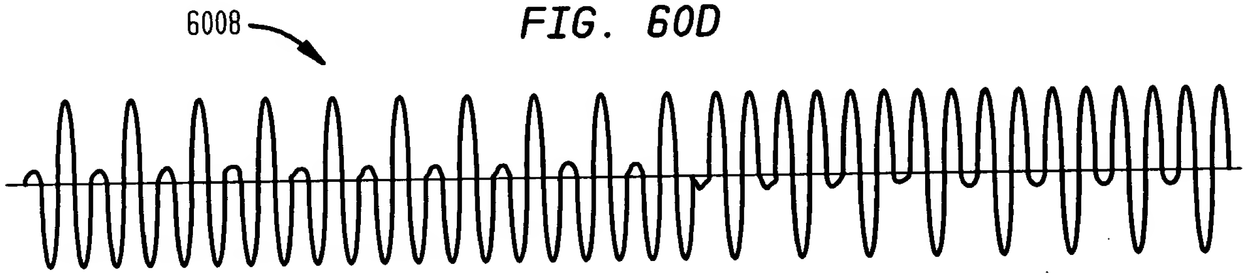

FIG. 60C

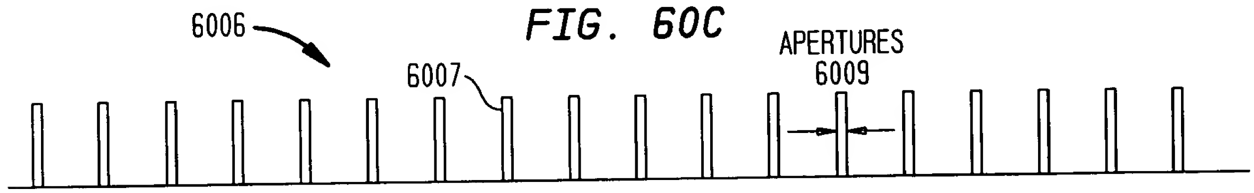

FIG. 60E

FIG. 60F

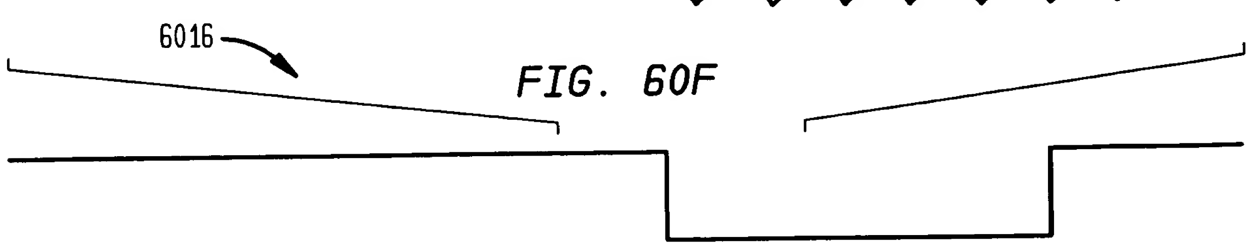

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FIG. 61A

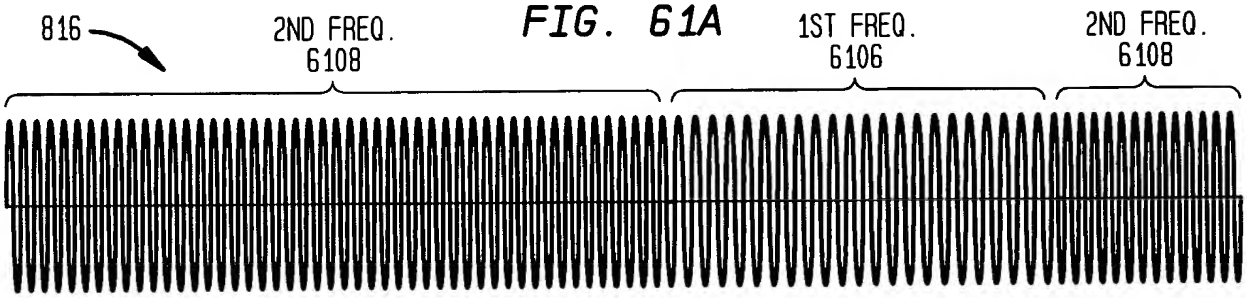


FIG. 61B

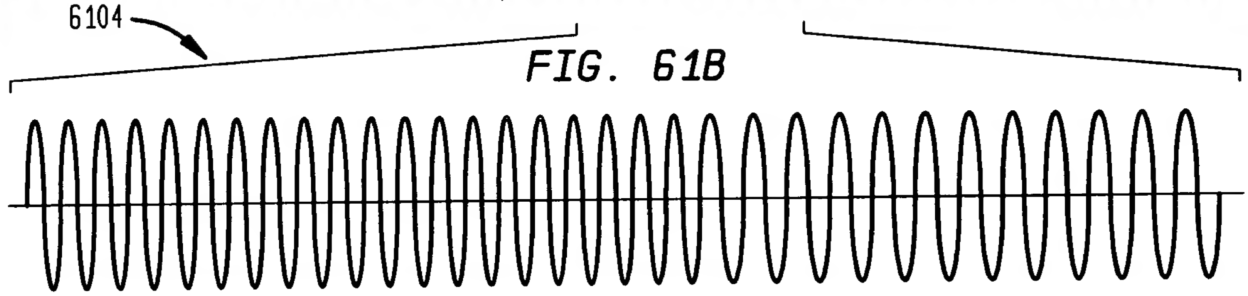


FIG. 61D

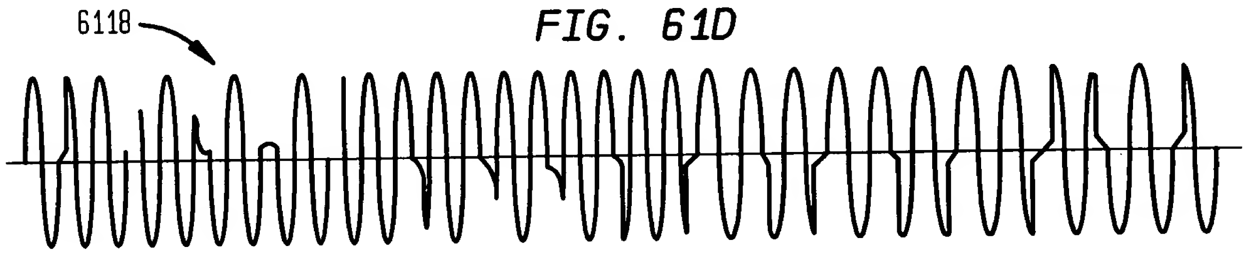


FIG. 61C

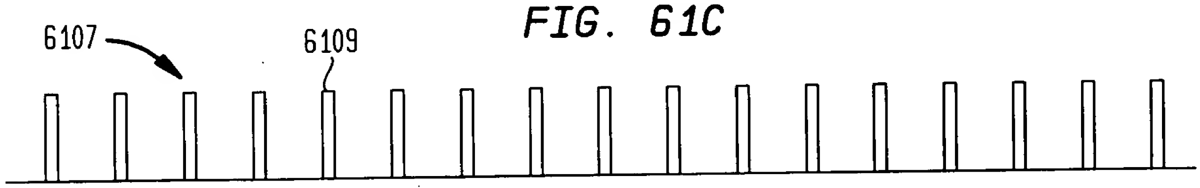


FIG. 61E

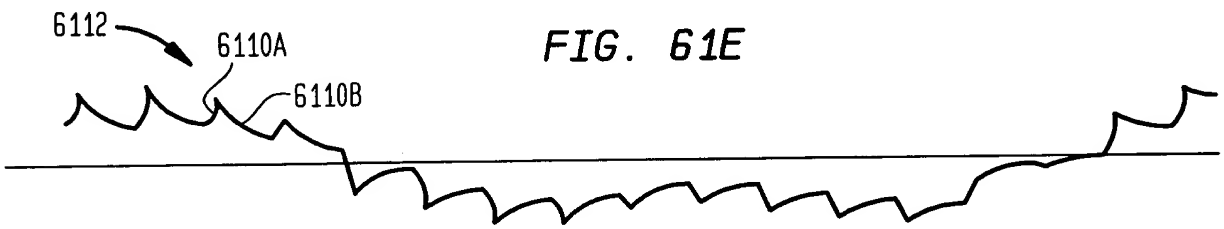
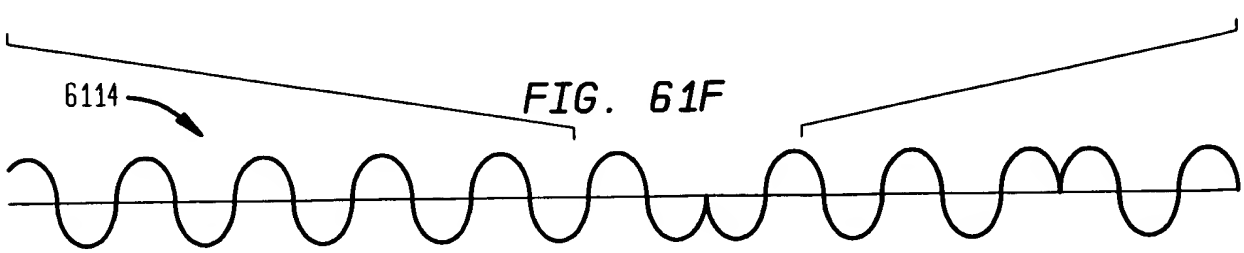


FIG. 61F



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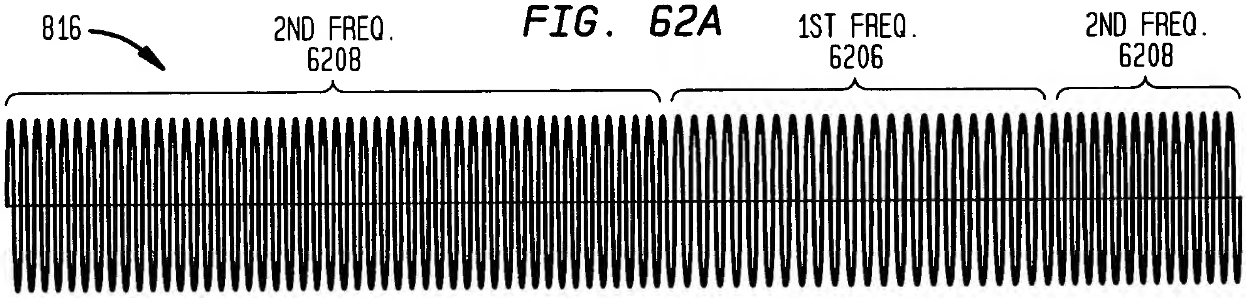


FIG. 62A

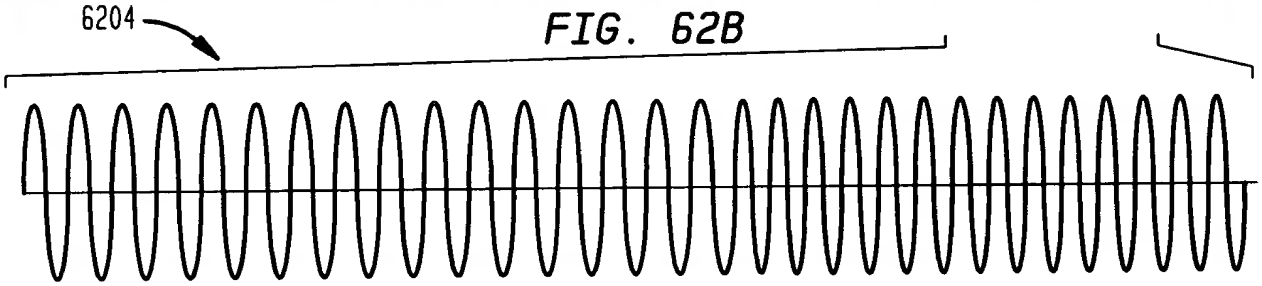


FIG. 62B

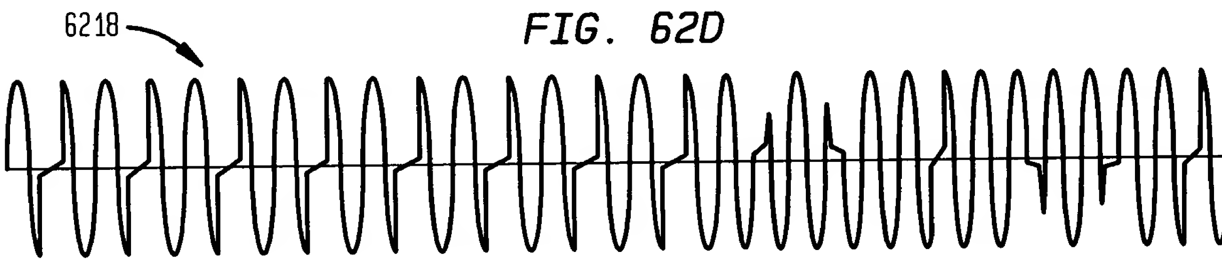


FIG. 62D

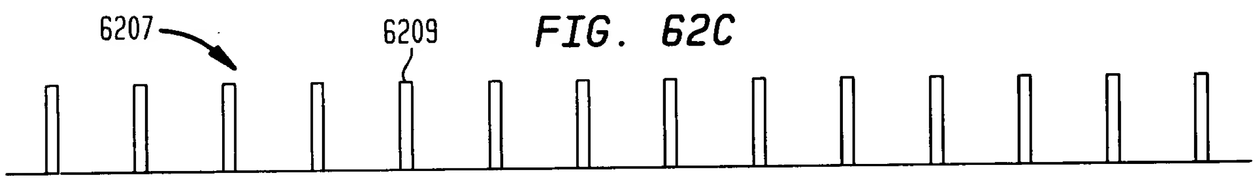


FIG. 62C

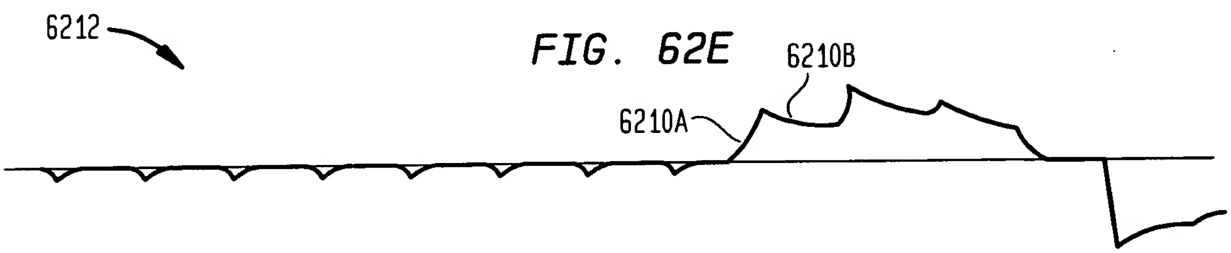


FIG. 62E

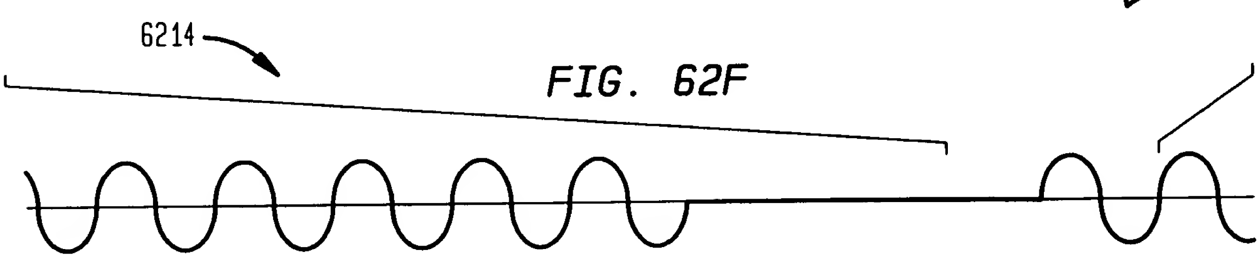


FIG. 62F

FIG. 63

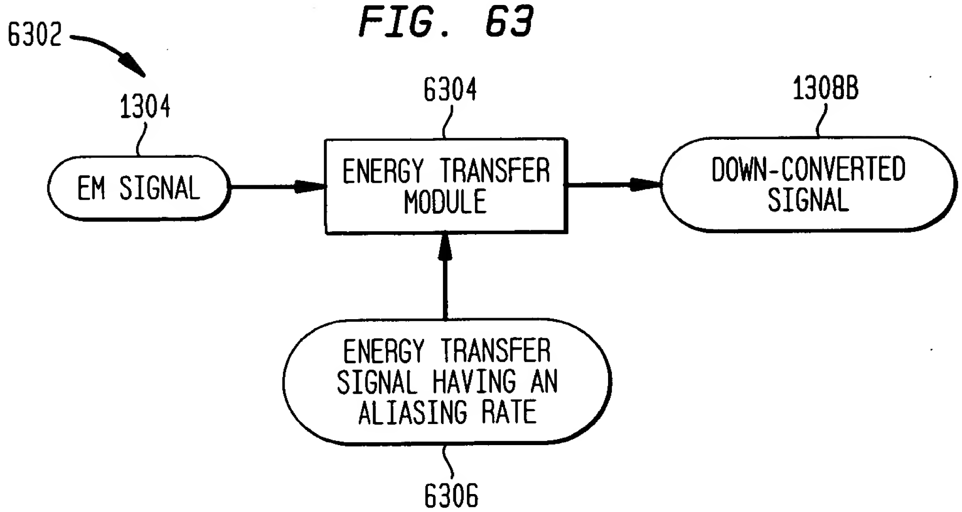


FIG. 64A

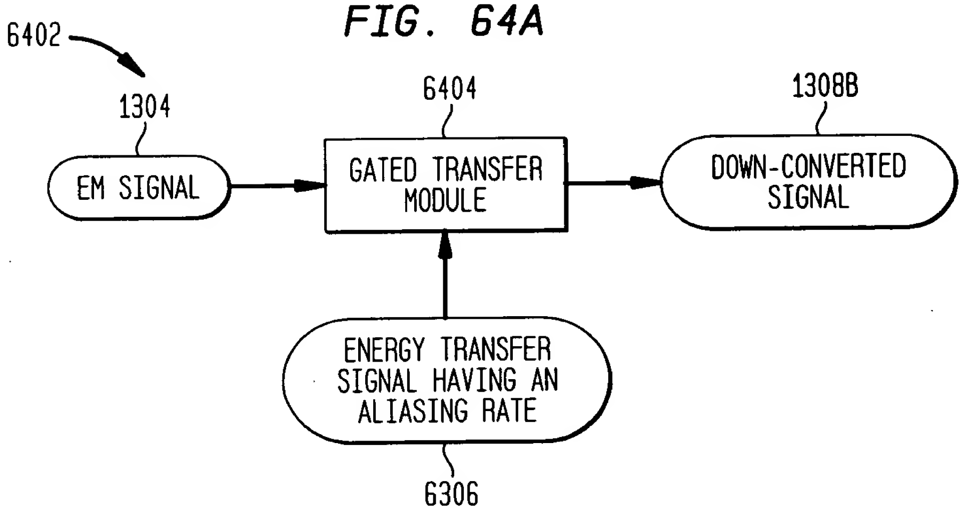


FIG. 64B

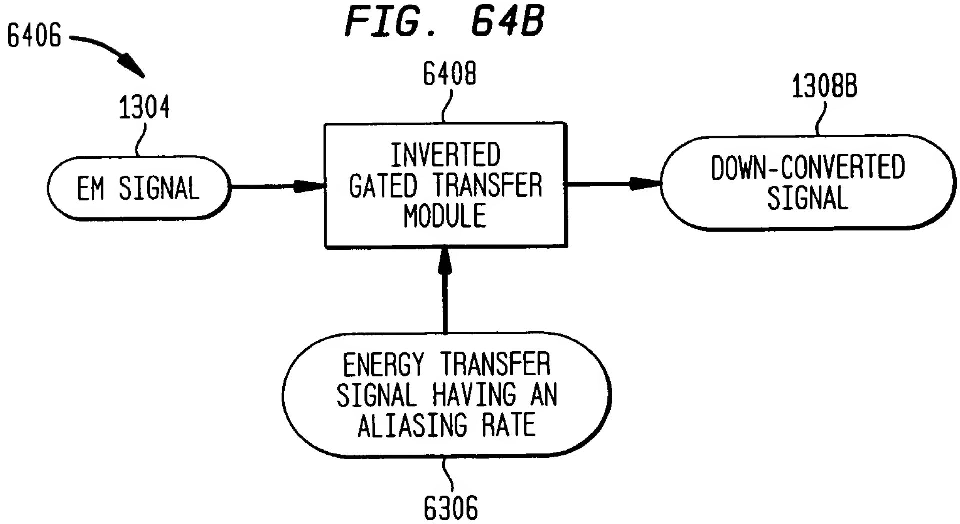


FIG. 65

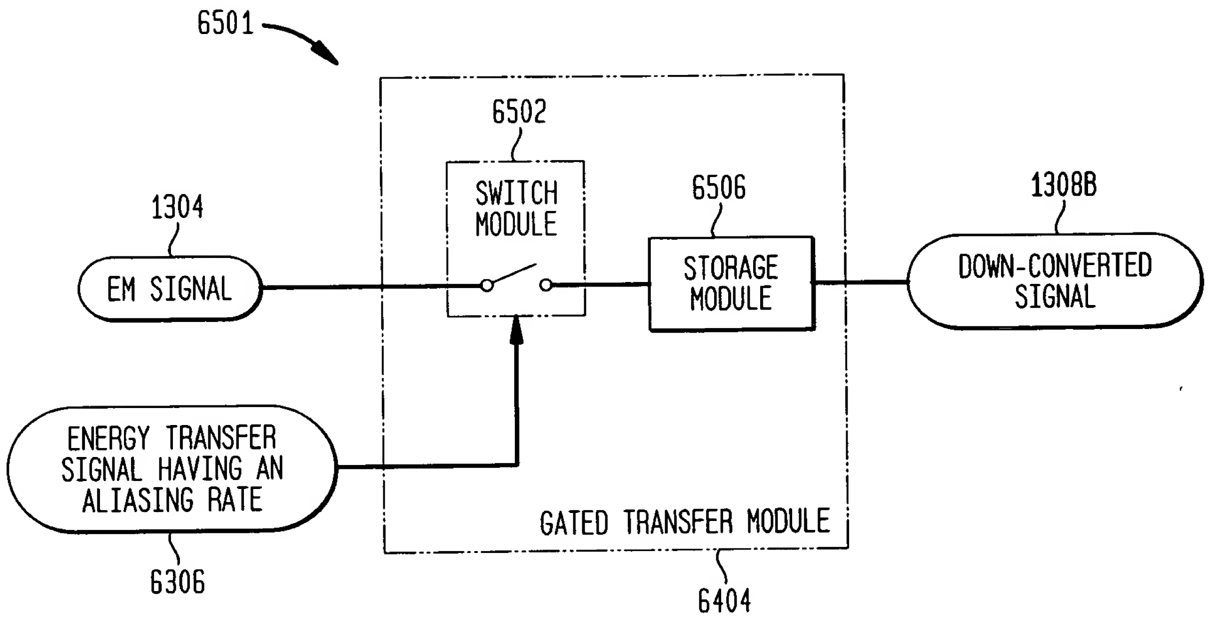


FIG. 66A

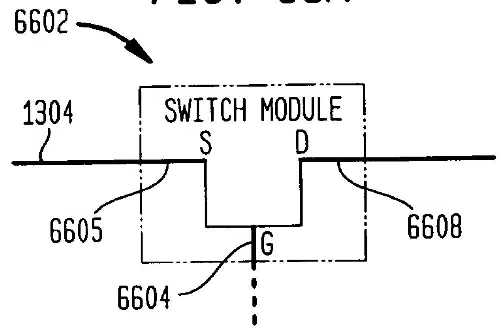


FIG. 66B

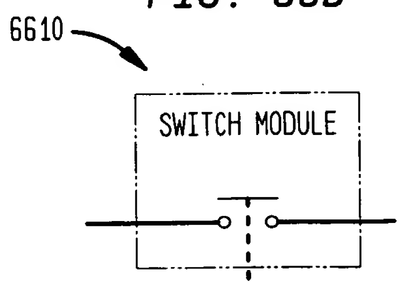


FIG. 66C

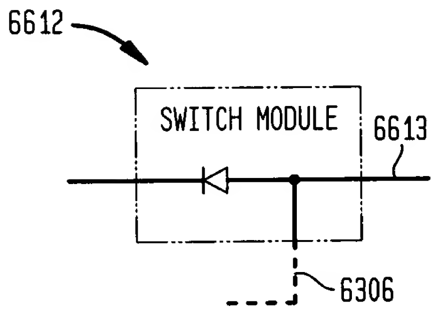


FIG. 66D

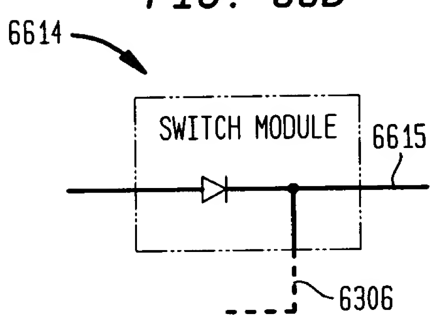


FIG. 67A

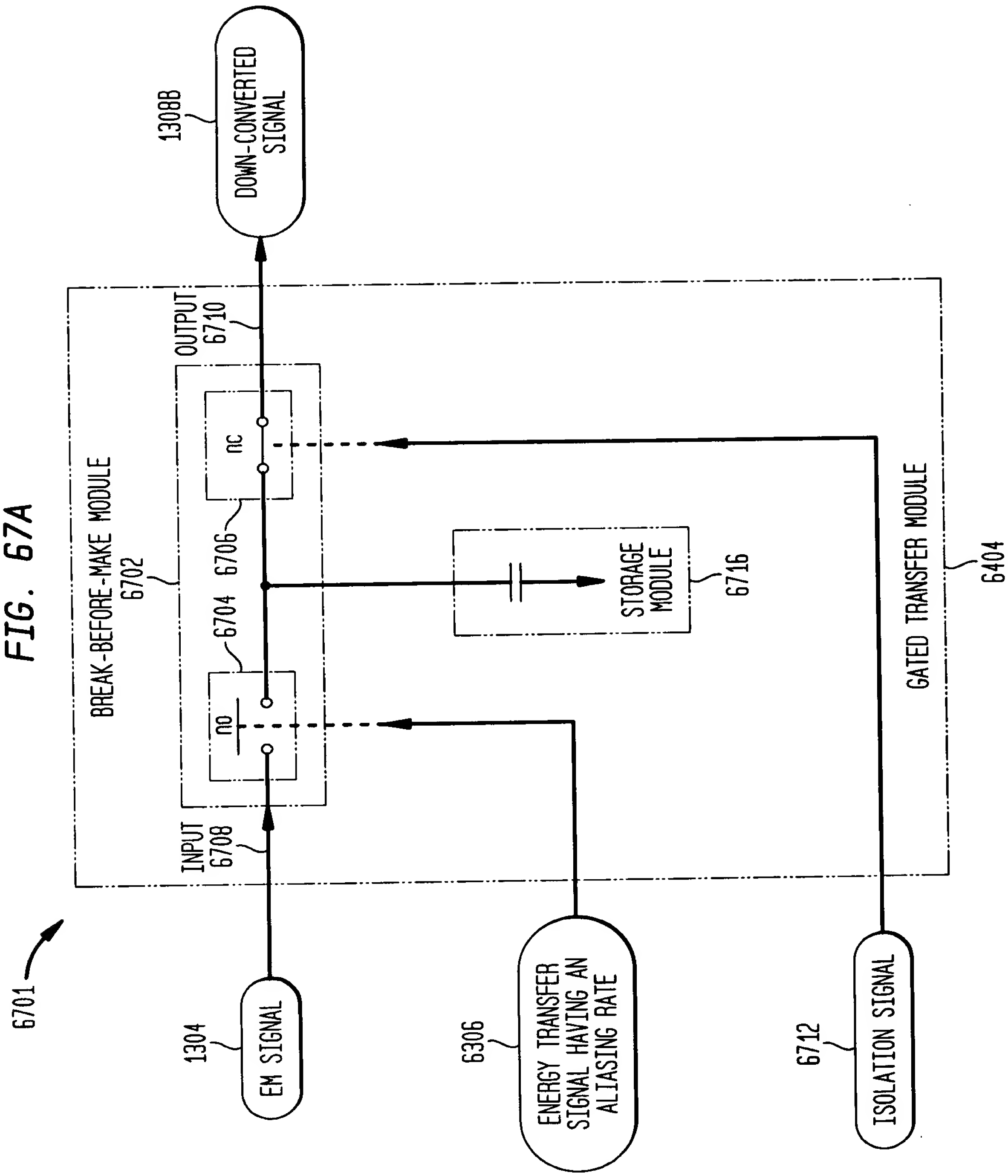

6701
1304
EM SIGNAL
6306
ENERGY TRANSFER SIGNAL HAVING AN ALIASING RATE
6712
ISOLATION SIGNAL
INPUT 6708
BREAK-BEFORE-MAKE MODULE 6702
no
6704
6706
nc
OUTPUT 6710
STORAGE MODULE
6716
GATED TRANSFER MODULE
6404
1308B
DOWN-CONVERTED SIGNAL

FIG. 67B

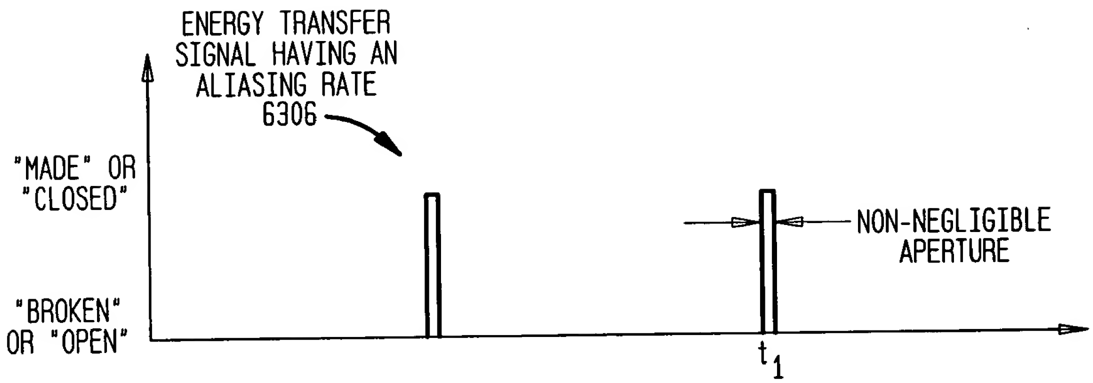


FIG. 67C

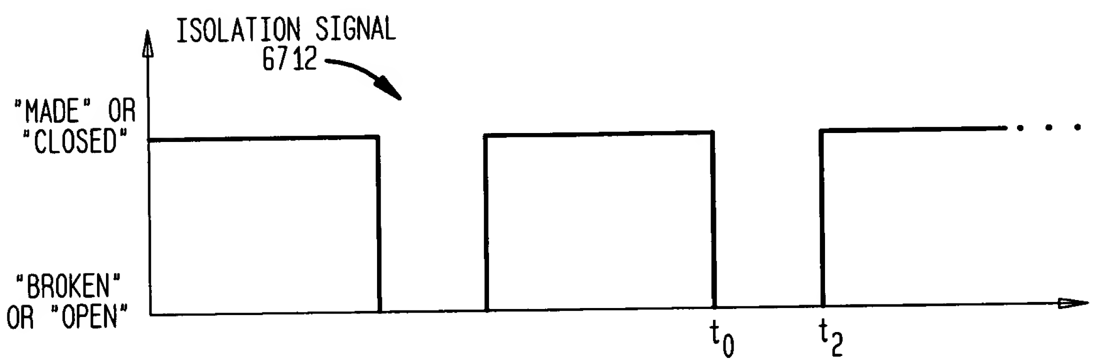


FIG. 68A

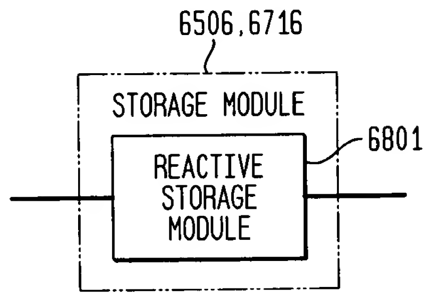


FIG. 68B

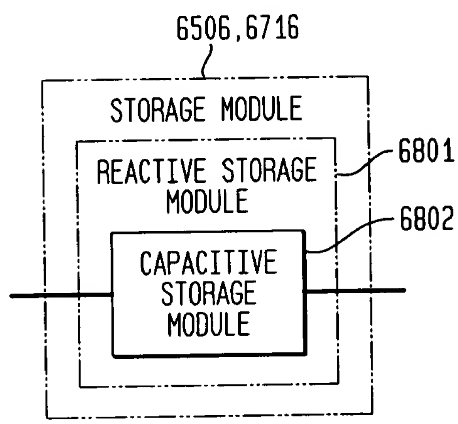


FIG. 68C

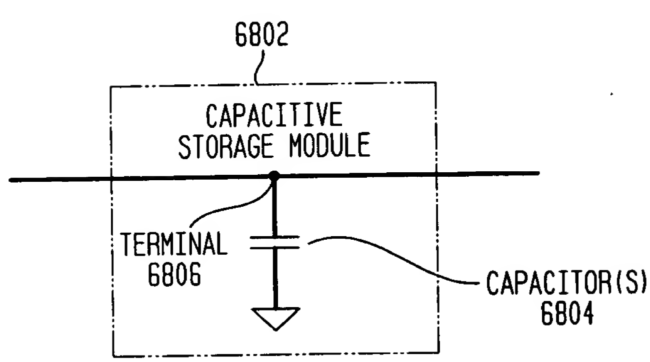


FIG. 68D

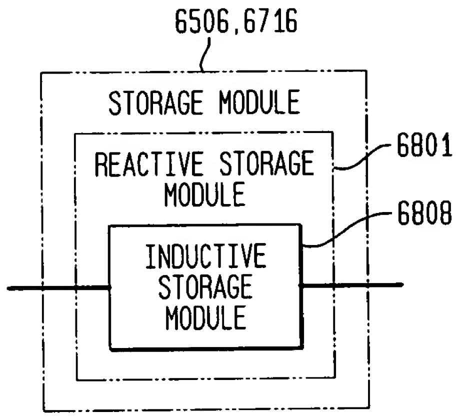


FIG. 68E

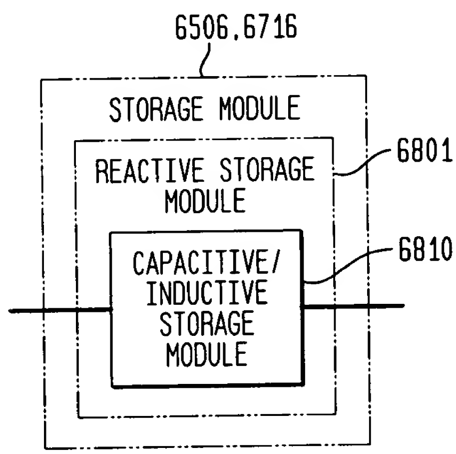
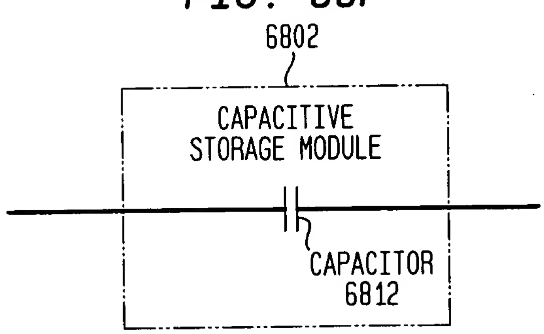


FIG. 68F



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Dkt No. 1744.0920001; Group Unit: 2634
Inventors: SORRELLS et al.
Tel. No.: 202-371-2600
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FIG. 68G

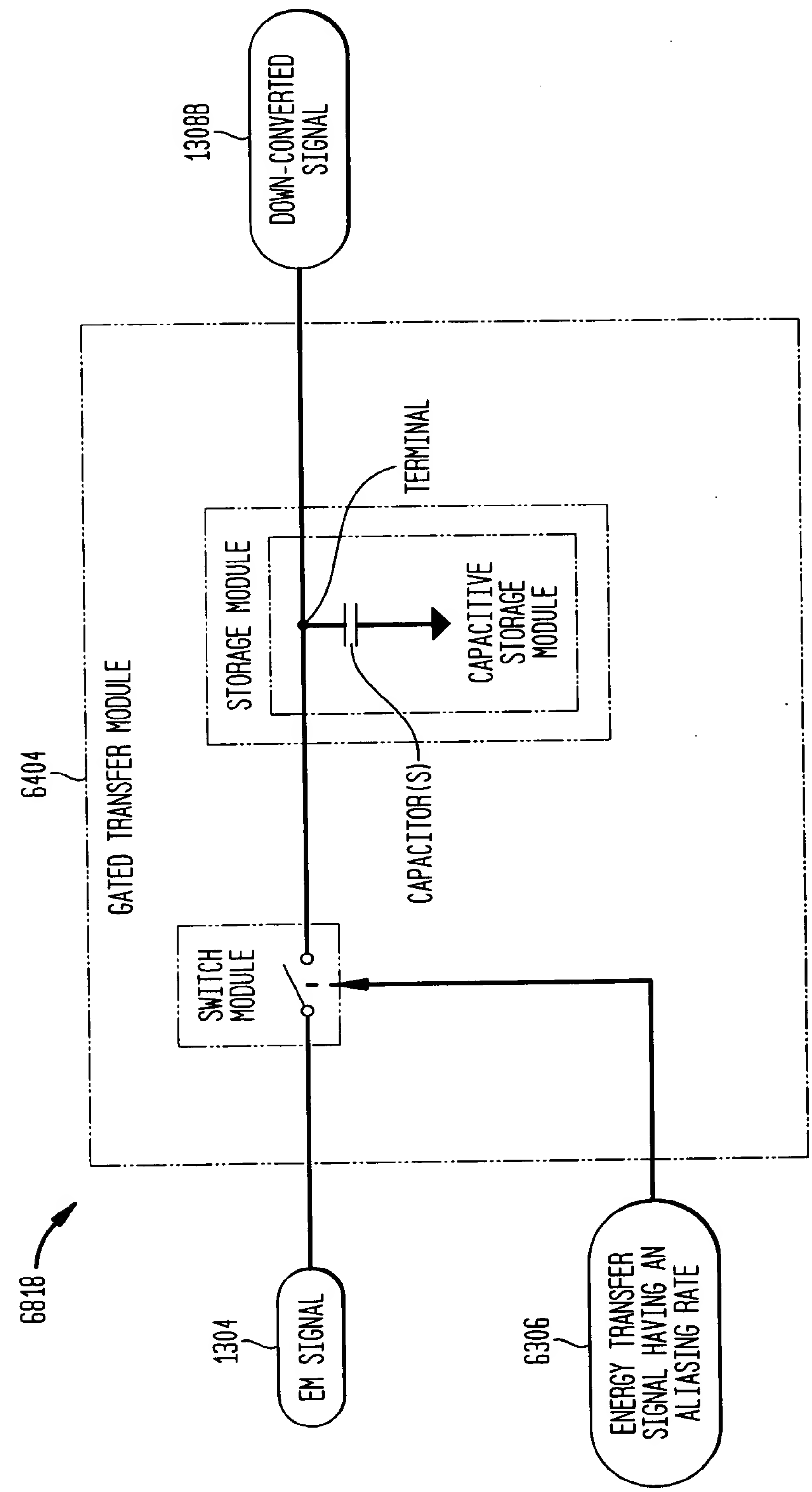
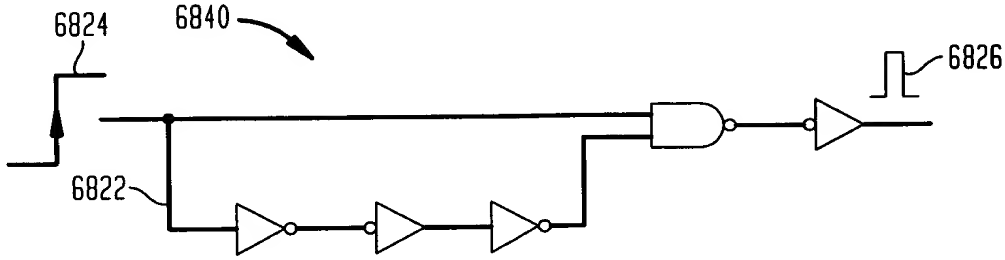
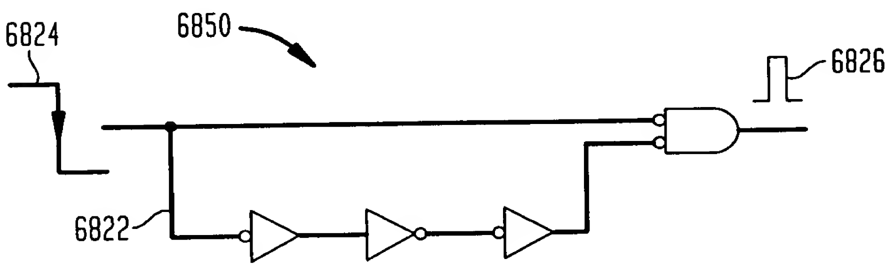


FIG. 68H



A. RISING EDGE PULSE GENERATOR

FIG. 68I



B. FALLING-EDGE PULSE GENERATOR

FIG. 68J

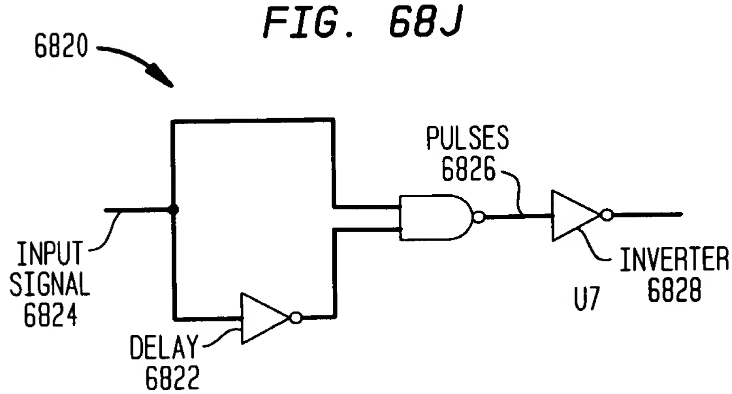


FIG. 68K

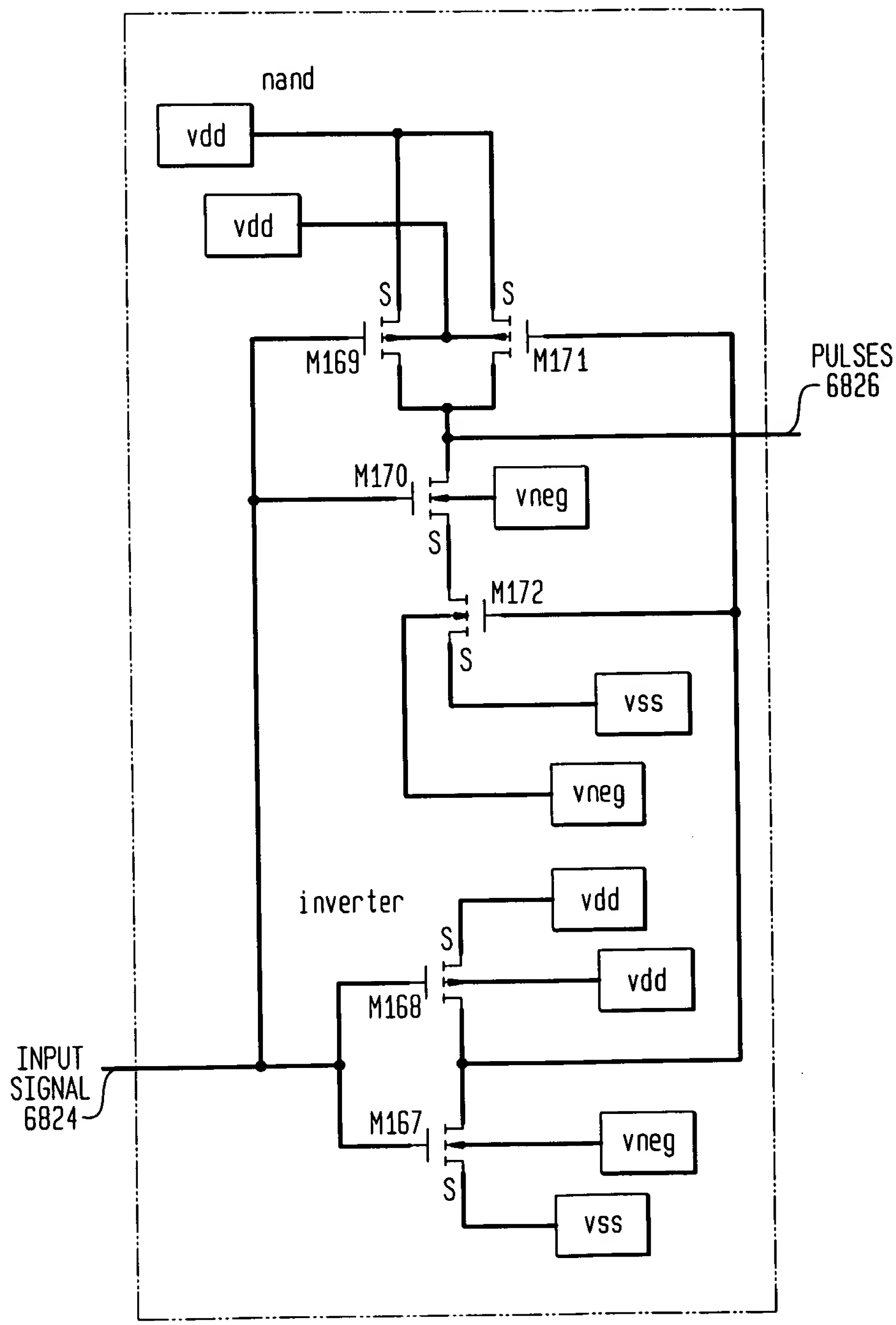


FIG. 68L

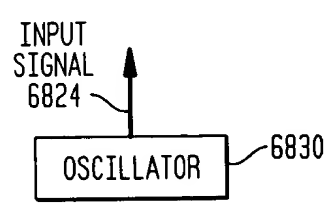


FIG. 69

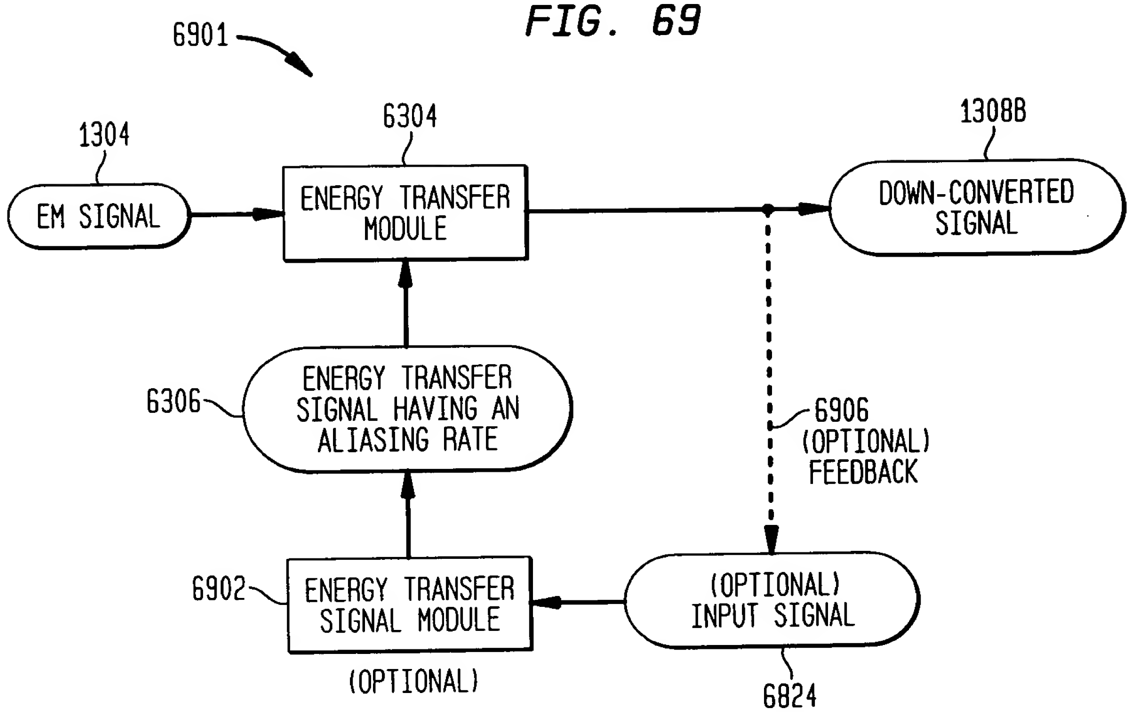

6901
1304
EM SIGNAL
6304
ENERGY TRANSFER MODULE
1308B
DOWN-CONVERTED SIGNAL
6306
ENERGY TRANSFER SIGNAL HAVING AN ALIASING RATE
6906
(OPTIONAL) FEEDBACK
6902
ENERGY TRANSFER SIGNAL MODULE
(OPTIONAL)
(OPTIONAL) INPUT SIGNAL
6824

FIG. 70

IMPEDANCE MATCHED ALIASING MODULE

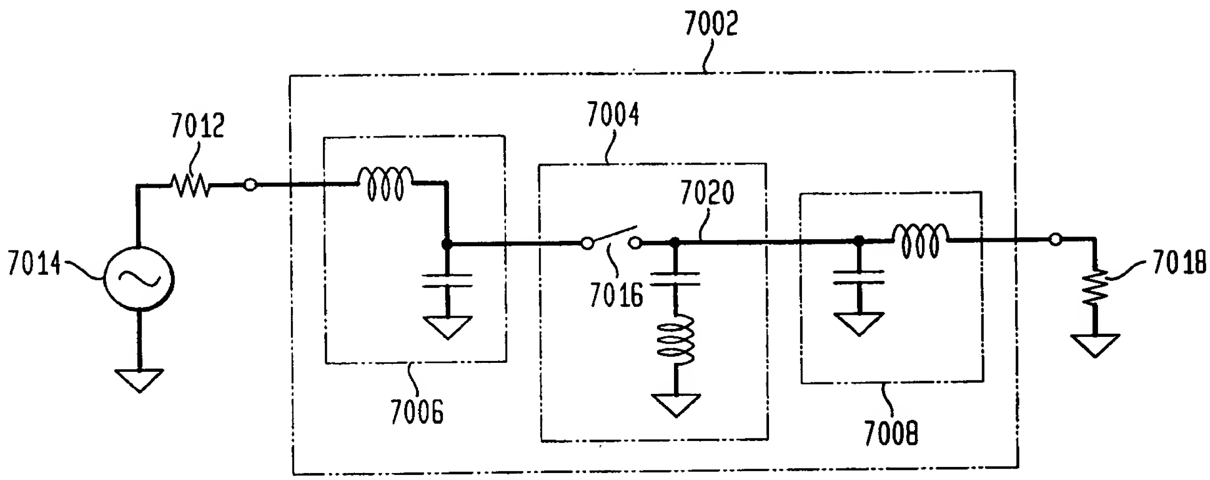
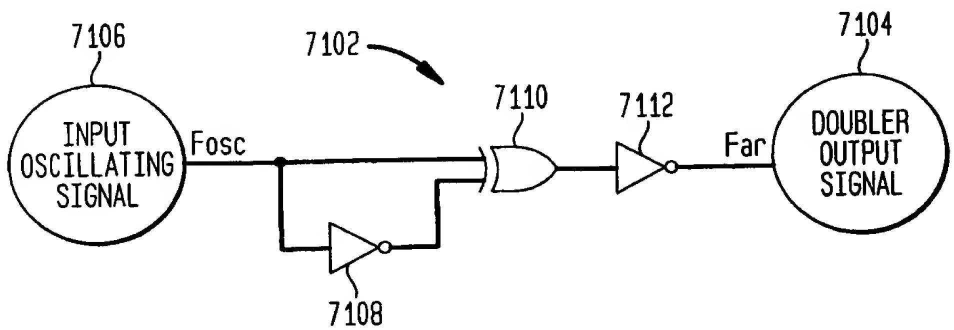


FIG. 71A



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Inventors: SORRELLS et al.
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Electromagnetic Signal, and Transforms for Same

FIG. 71B

7106

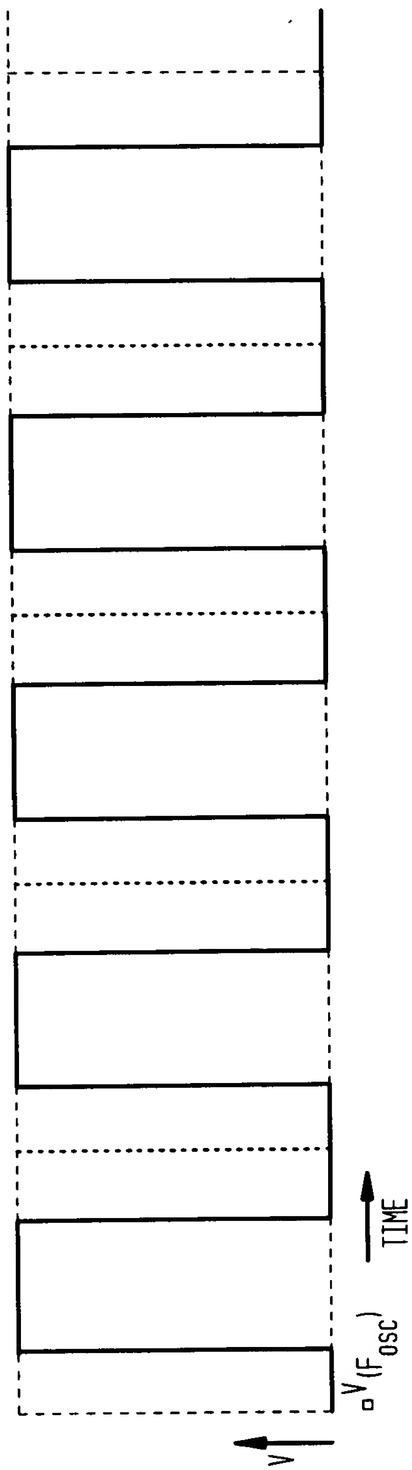


FIG. 71C

7104

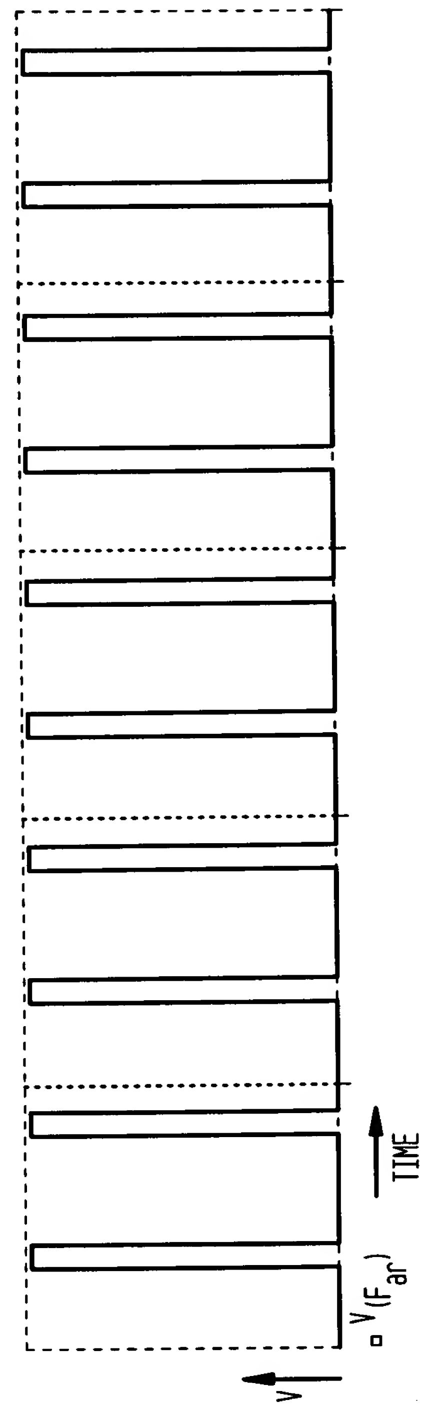


FIG. 72

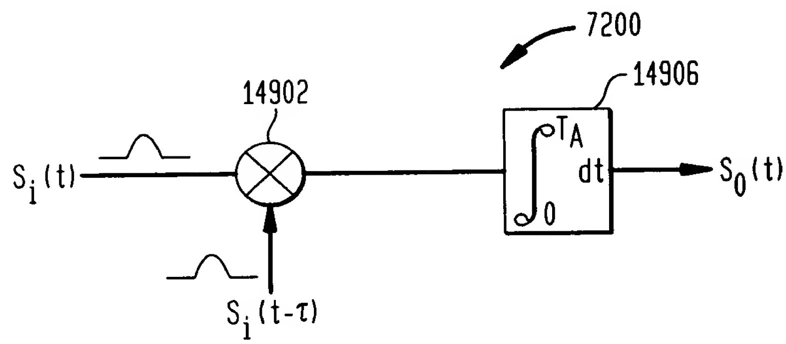


FIG. 73

ALIASING MODULE

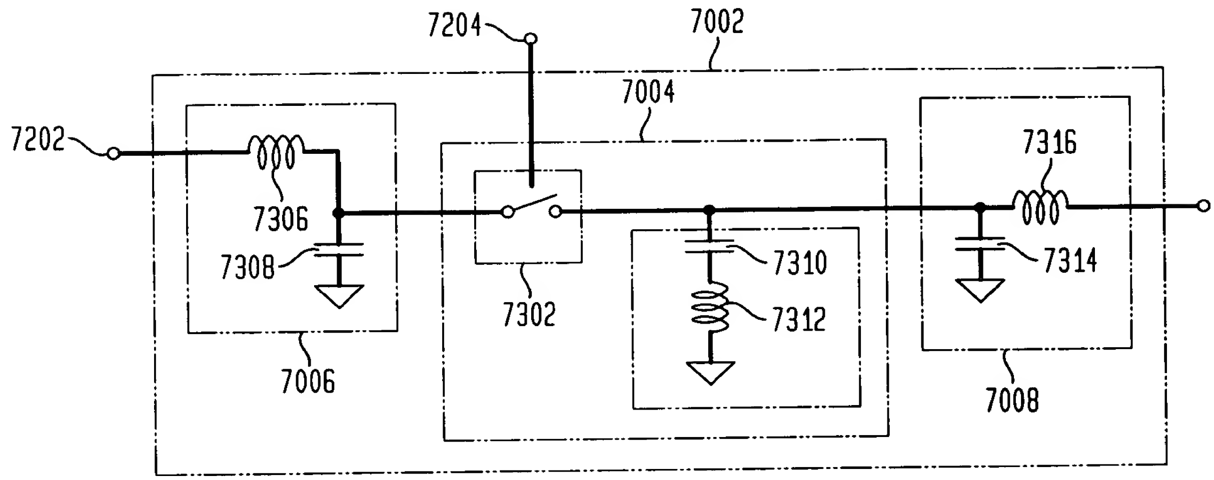
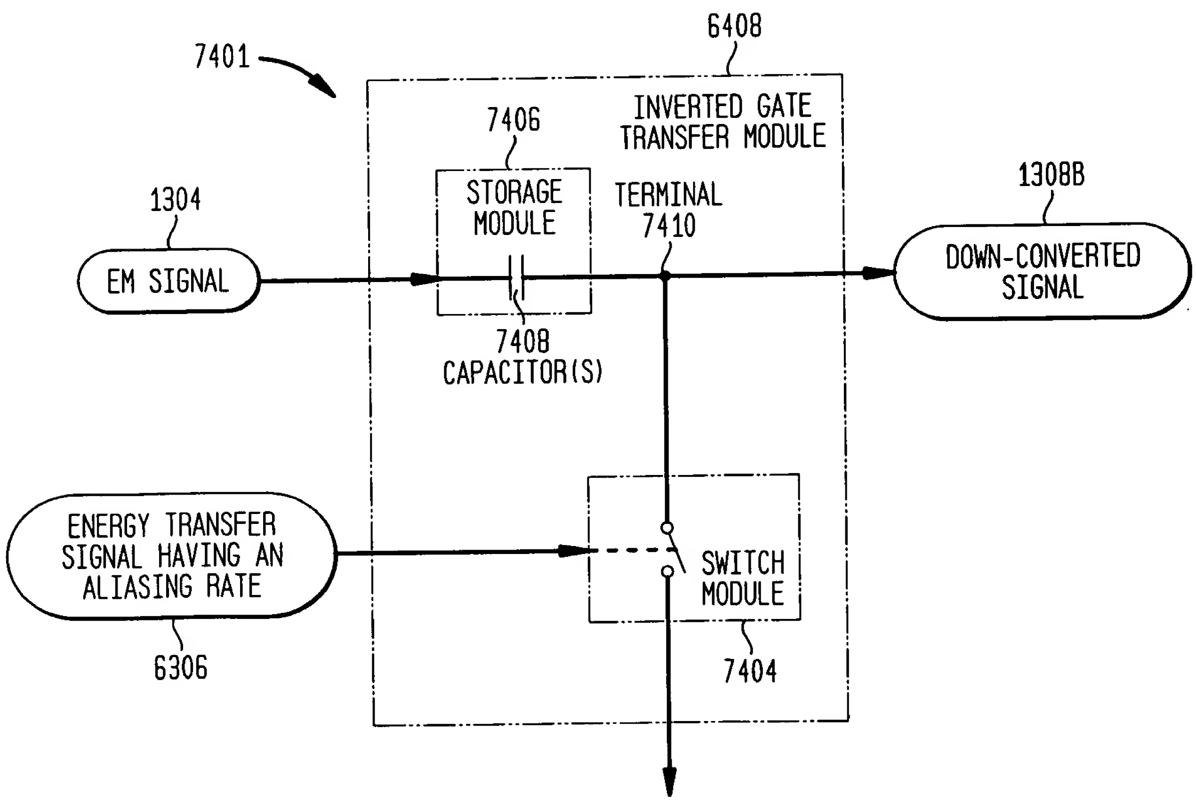


FIG. 74



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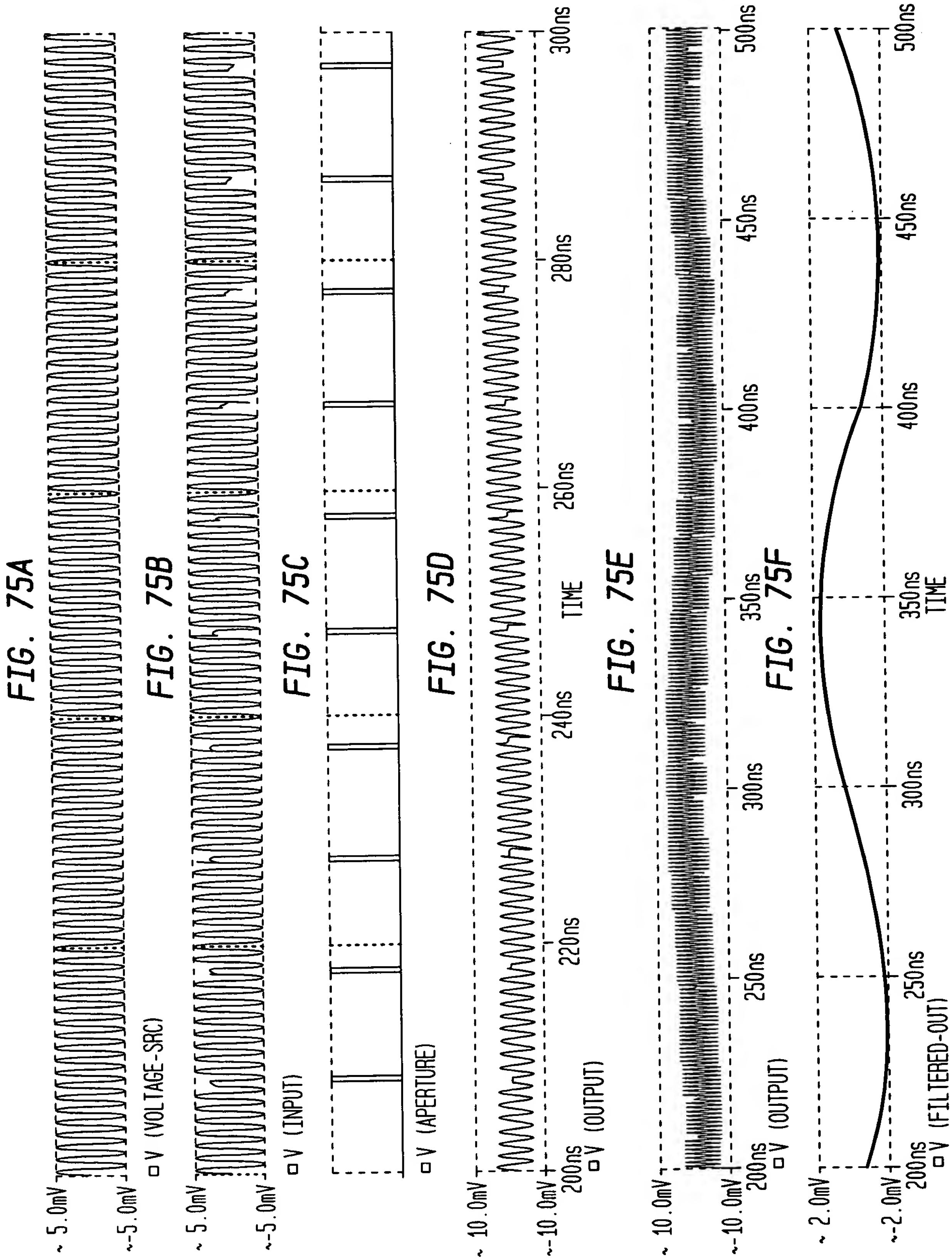


FIG. 75A

FIG. 75B

FIG. 75C

FIG. 75D

FIG. 75E

FIG. 75F

FIG. 76A

DIFFERENTIAL ENERGY TRANSFER CONFIGURATION

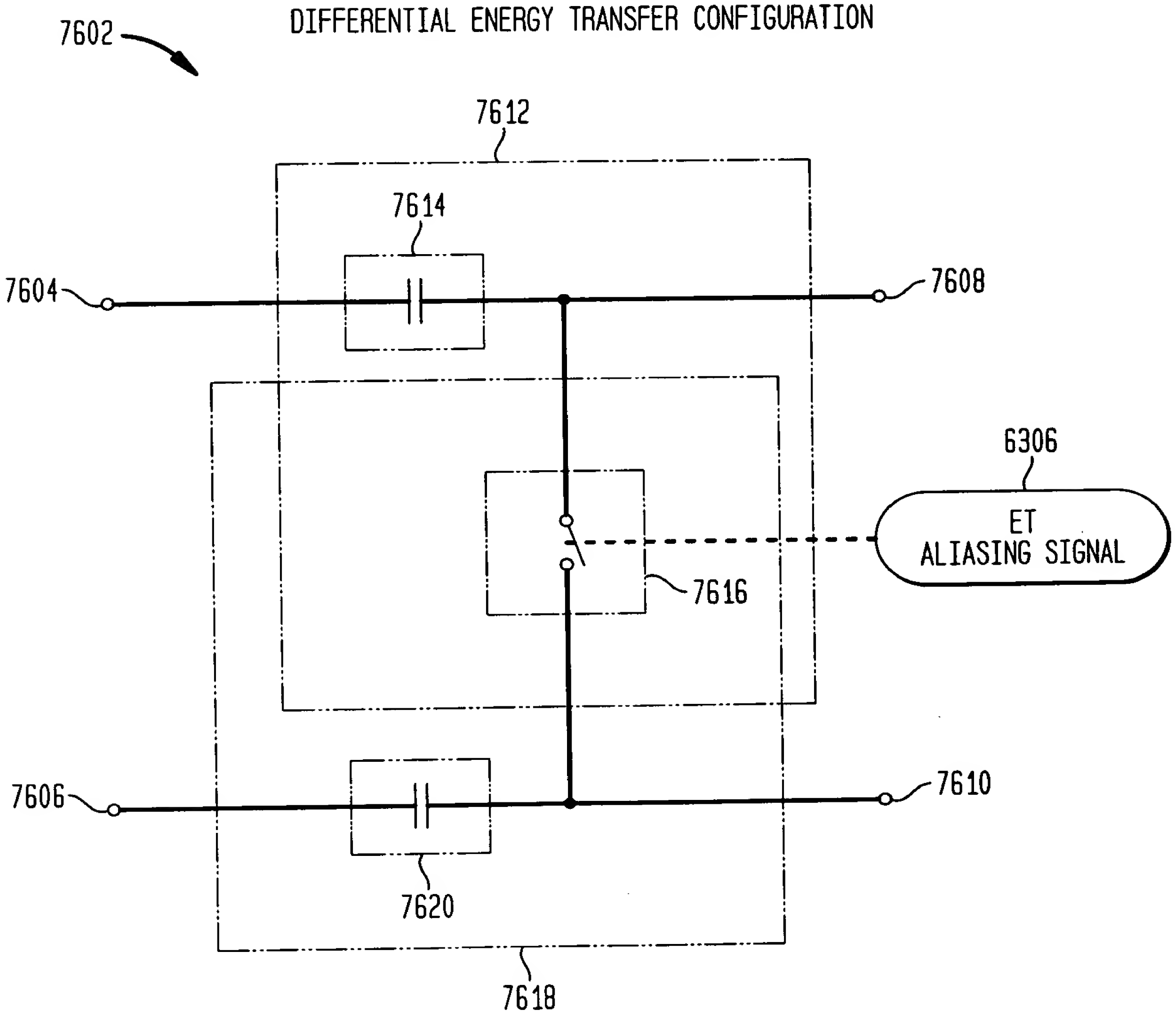


FIG. 76B

DIFFERENTIAL INPUT TO DIFFERENTIAL OUTPUT

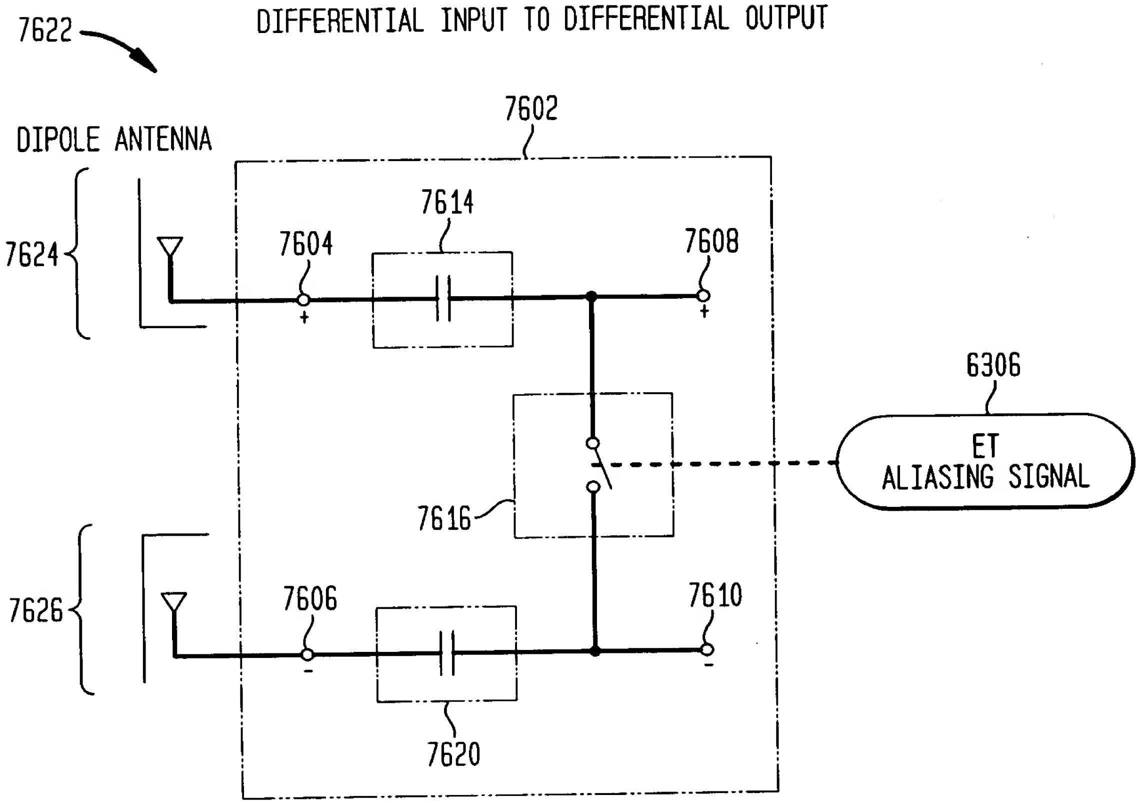


FIG. 76C

SINGLE INPUT TO DIFFERENTIAL OUTPUT

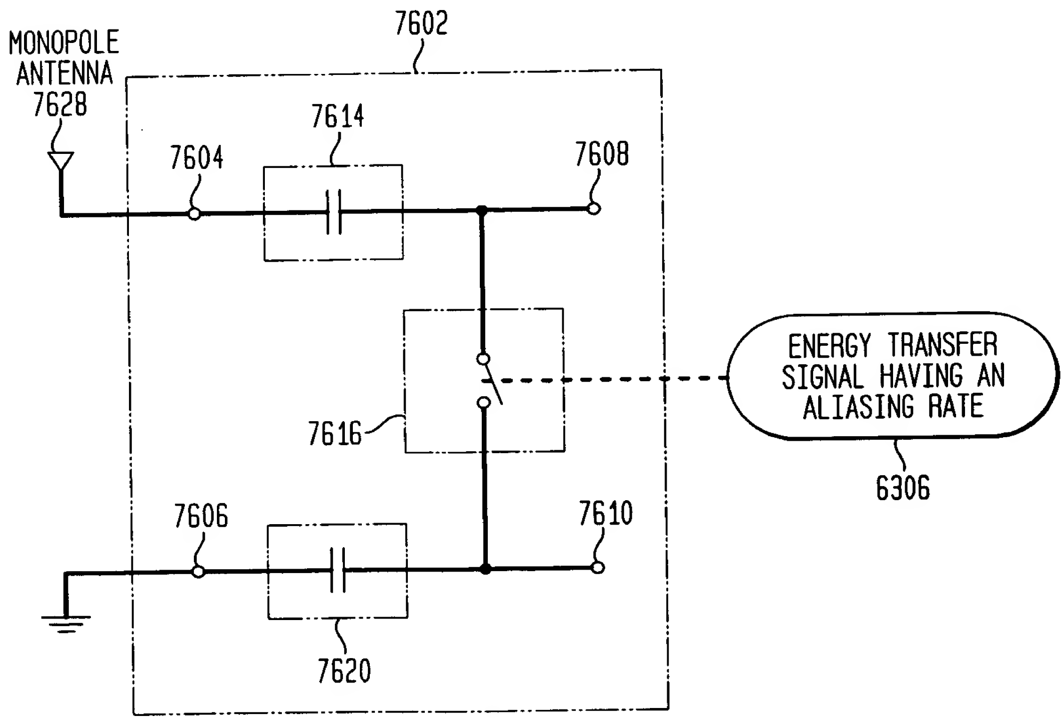


FIG. 76D

DIFFERENTIAL INPUT TO SINGLE OUTPUT

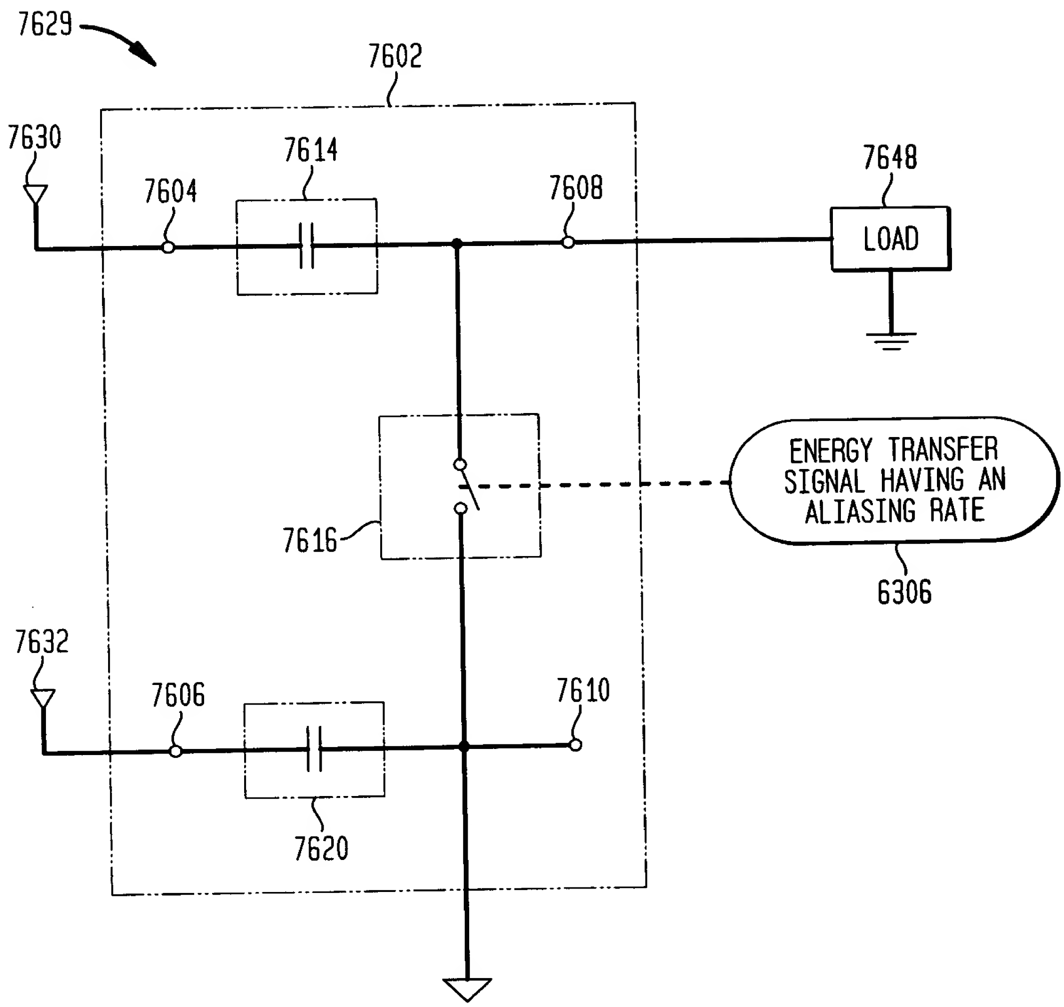


FIG. 76E

EXAMPLE INPUT/OUTPUT CIRCUITRY

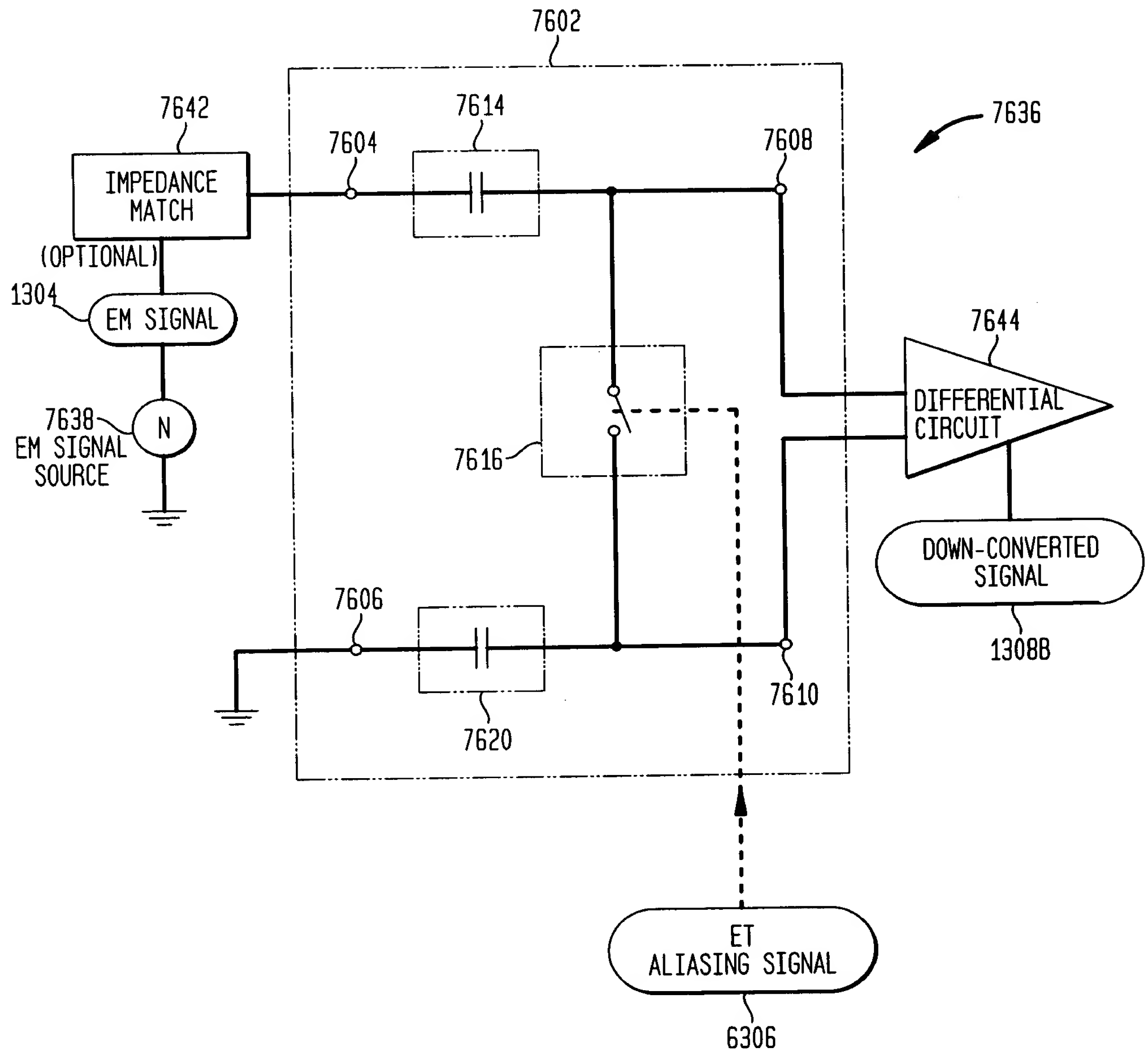


FIG. 77A

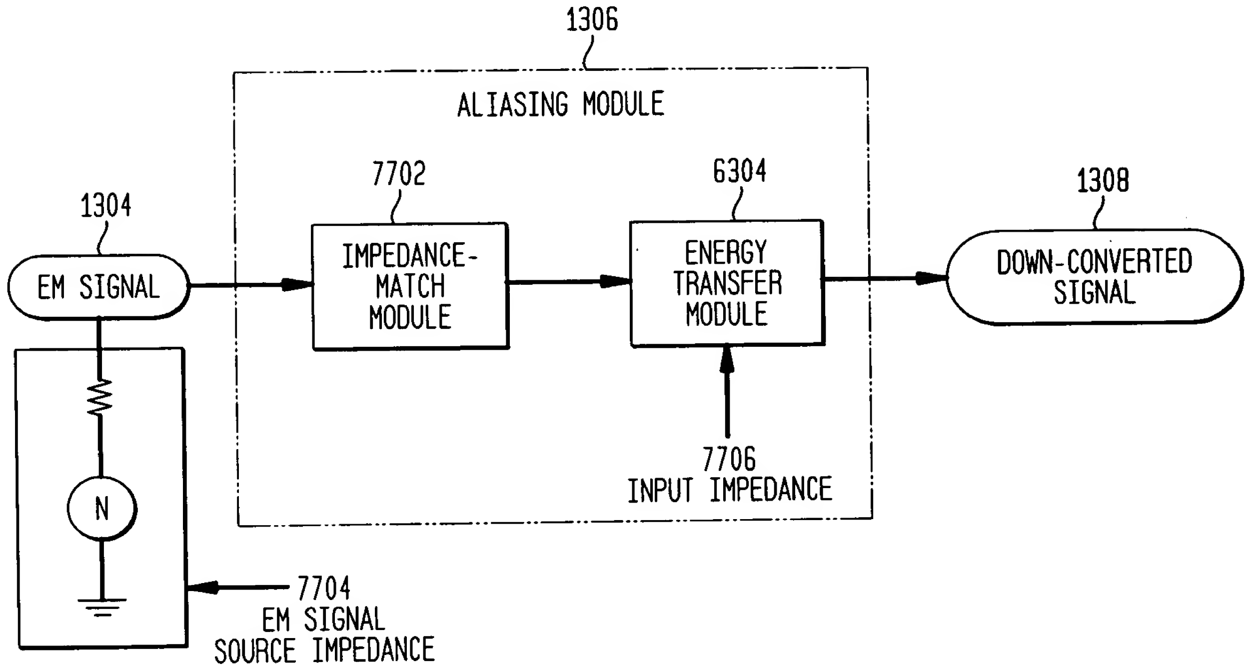


FIG. 77B

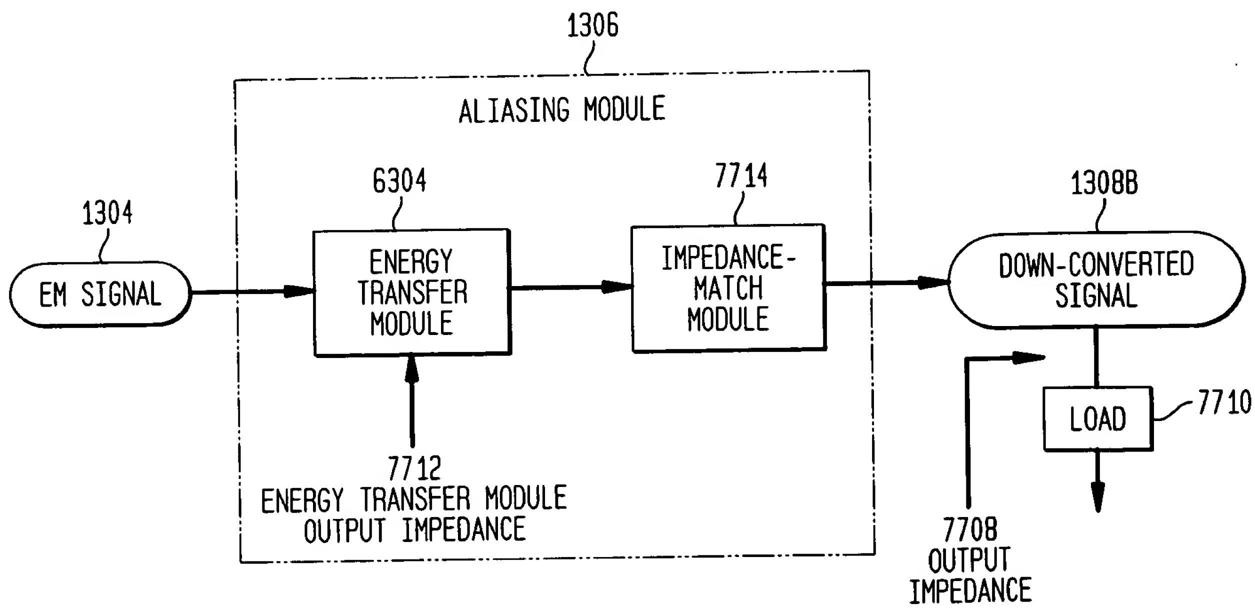


FIG. 77C

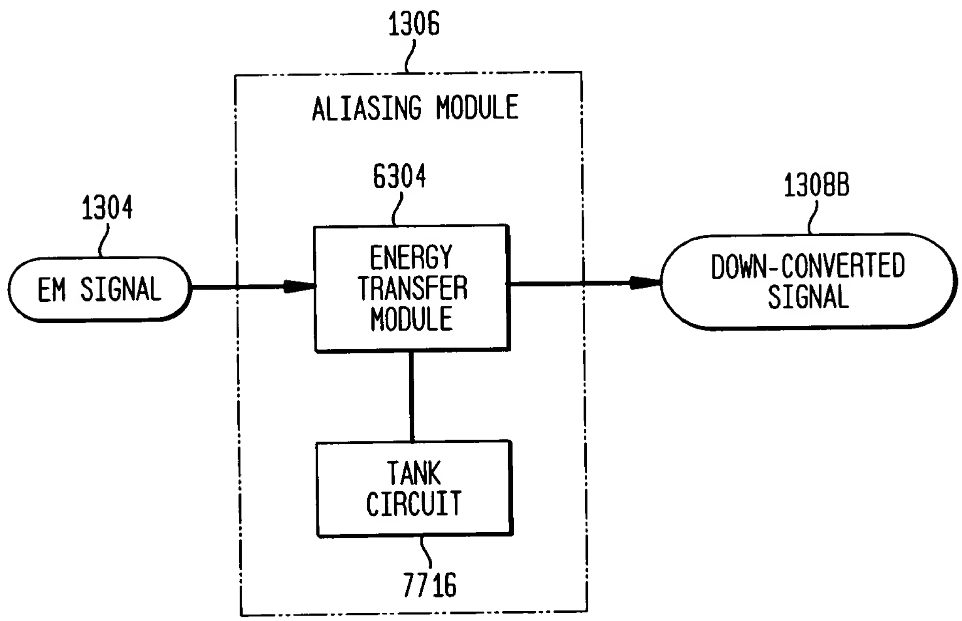

1306
ALIASING MODULE
6304
1304
EM SIGNAL
ENERGY TRANSFER MODULE
1308B
DOWN-CONVERTED SIGNAL
TANK CIRCUIT
7716

FIG. 78A

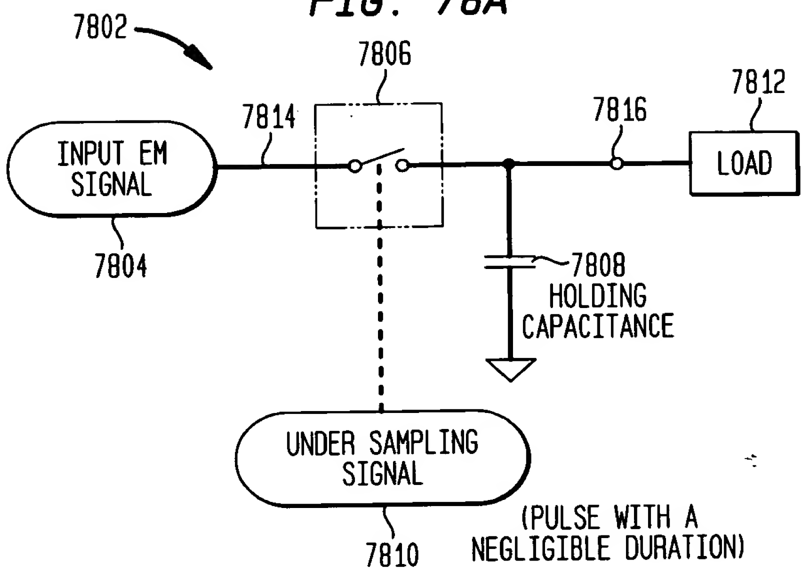
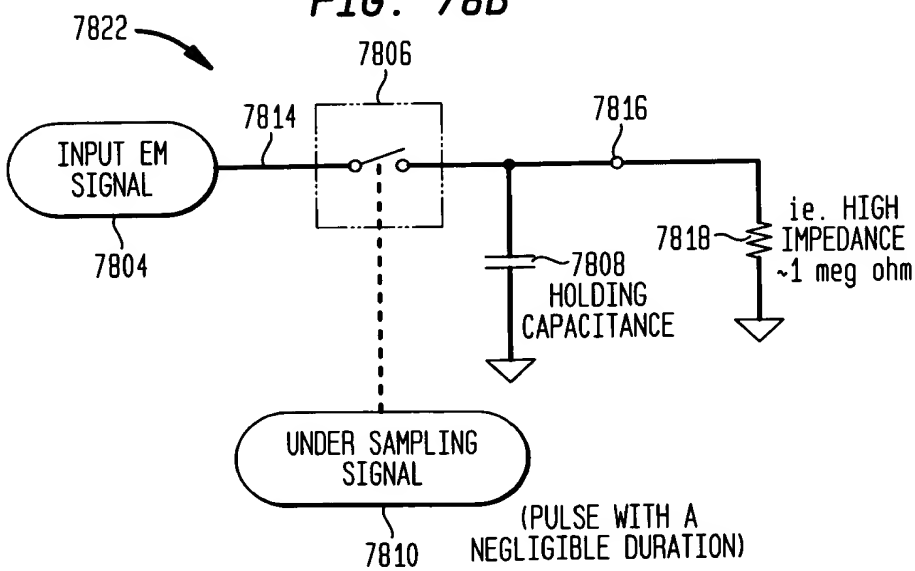


FIG. 78B



Appl. No. 09/550,642; Filed: Apr 14, 2000
Dkt No. 1744.0920001; Group Unit: 2634

Inventors: SORRELLS et al.
Tel. No.: 202-371-2600

For: Method and System for Down-Converting an Electromagnetic Signal, and Transforms for Same

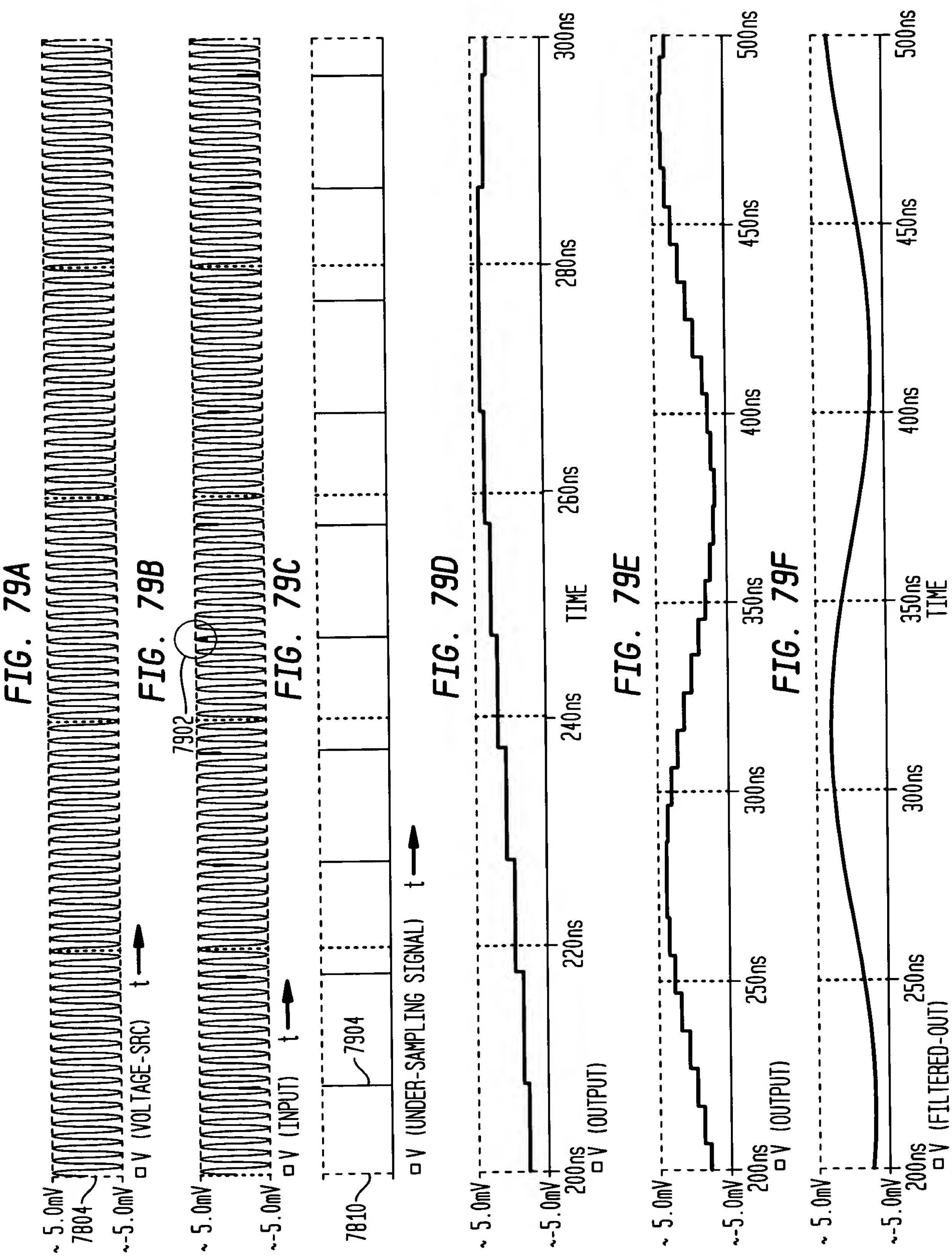


FIG. 79A

FIG. 79B

FIG. 79C

FIG. 79D

FIG. 79E

FIG. 79F

Appl. No. 09/550,642; Filed: Apr 14, 2000
Dkt No. 1744.0920001; Group Unit: 2634
Inventors: SORRELLS et al.
Tel. No.: 202-371-2600
For: Method and System for Down-Converting an Electromagnetic Signal, and Transforms for Same

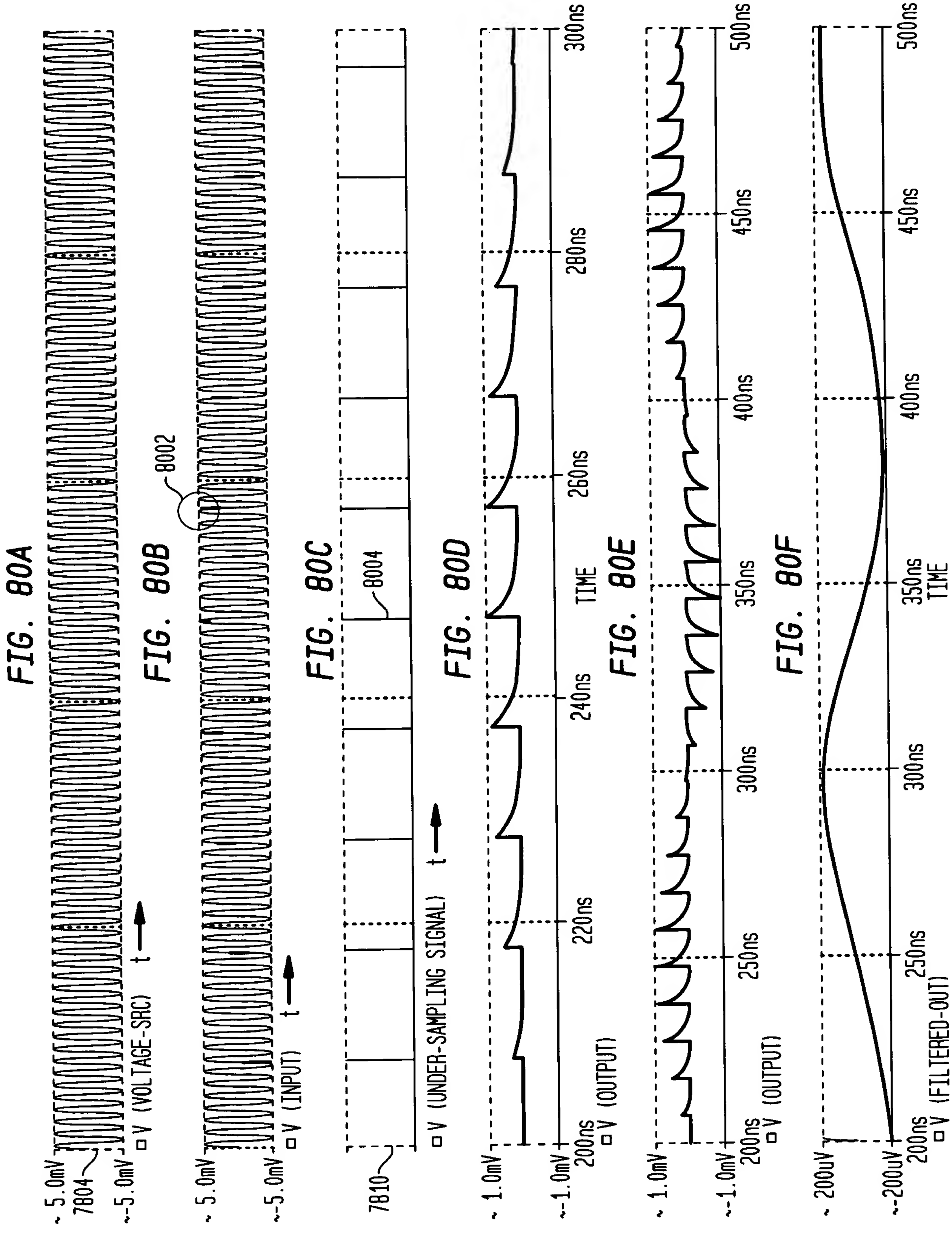


FIG. 80A
FIG. 80B
FIG. 80C
FIG. 80D
FIG. 80E
FIG. 80F

Replacement Sheet
Sheet 100 of 284
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Dkt No. 1744.0920001; Group Unit: 2634
Inventors: SORRELLS et al.
Tel. No.: 202-371-2600
For: Method and System for Down-Converting an Electromagnetic Signal, and Transforms for Same

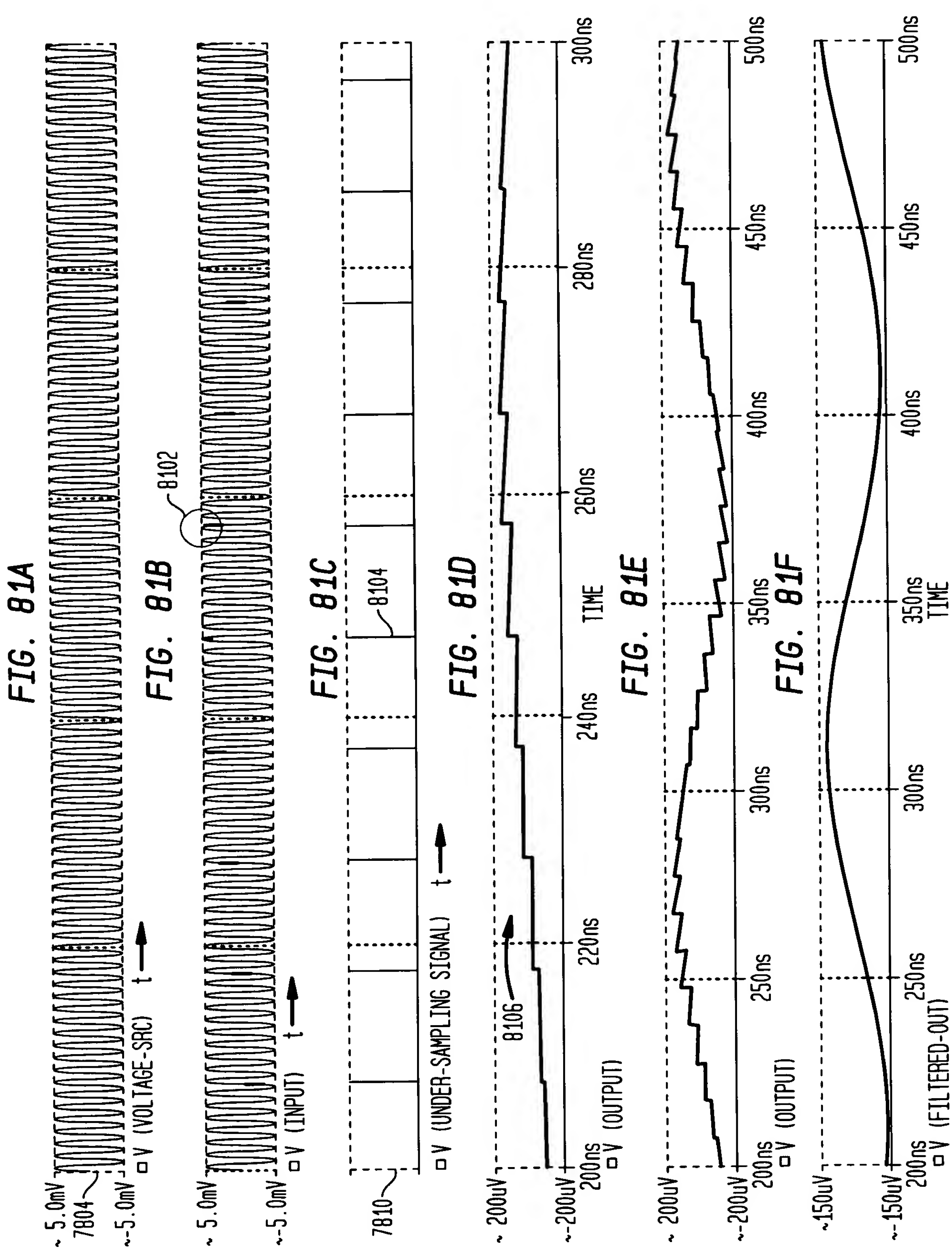


FIG. 81A

FIG. 81B

FIG. 81C

FIG. 81D

FIG. 81E

FIG. 81F

FIG. 82A

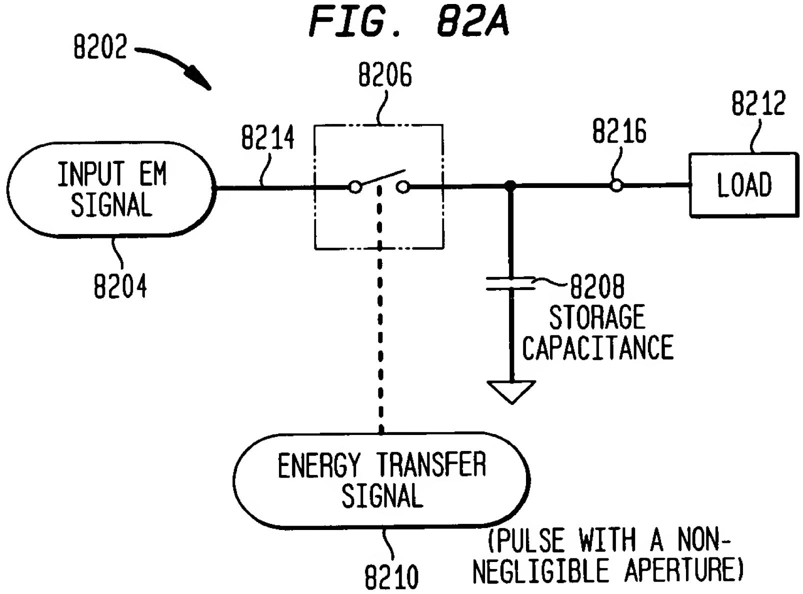
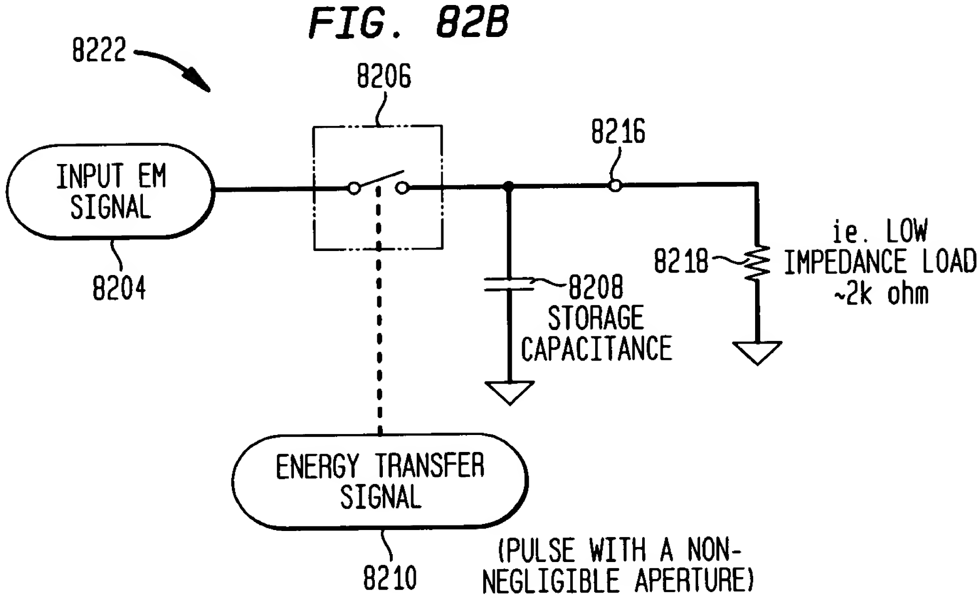


FIG. 82B



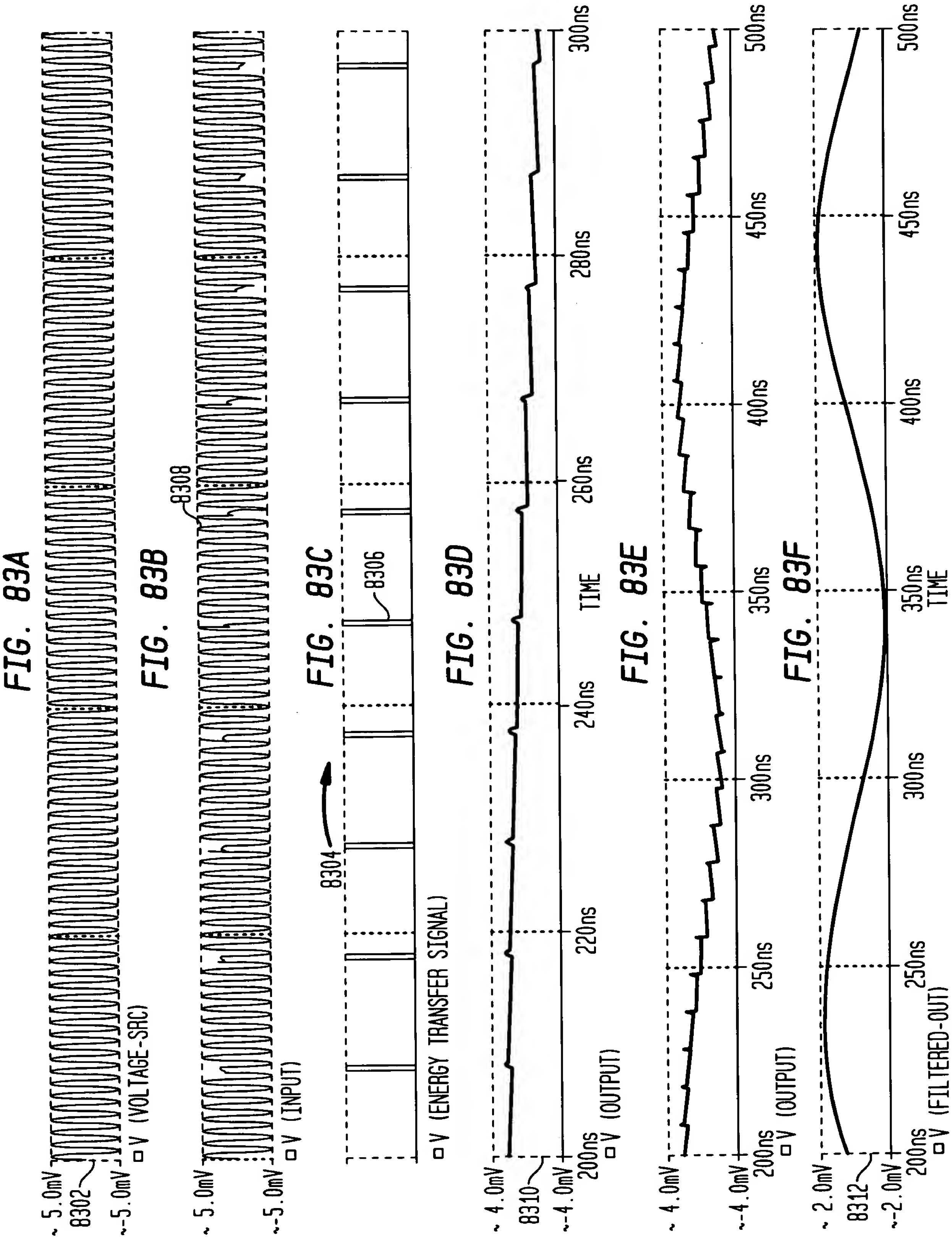


FIG. 83A
5.0mV
8302
-5.0mV
V (VOLTAGE-SRC)
FIG. 83B
8308
5.0mV
-5.0mV
V (INPUT)
FIG. 83C
8304
8306
V (ENERGY TRANSFER SIGNAL)
FIG. 83D
4.0mV
8310
-4.0mV
200ns
220ns
240ns
260ns
280ns
300ns
TIME
V (OUTPUT)
FIG. 83E
4.0mV
-4.0mV
200ns
250ns
300ns
350ns
400ns
450ns
500ns
V (OUTPUT)
FIG. 83F
2.0mV
8312
-2.0mV
200ns
250ns
300ns
350ns
400ns
450ns
500ns
TIME
V (FILTERED-OUT)

FIG. 84A

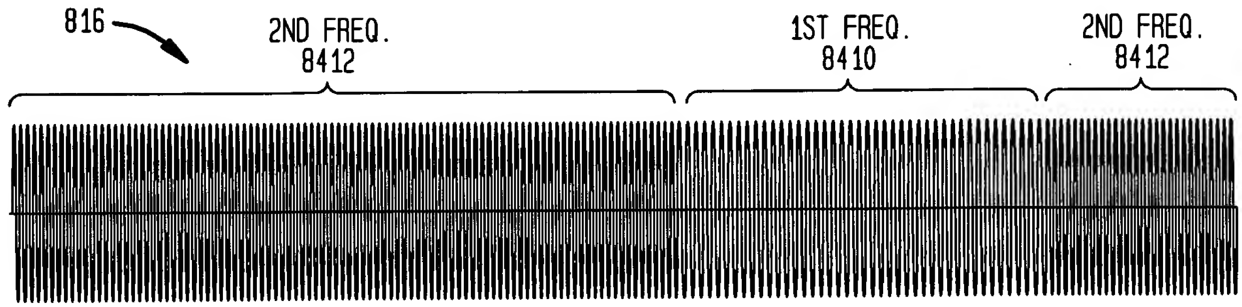


FIG. 84B

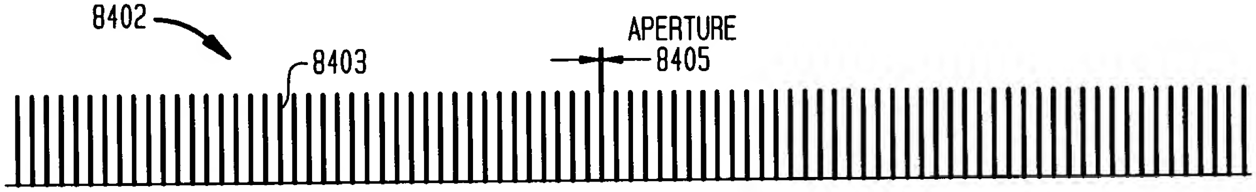


FIG. 84C

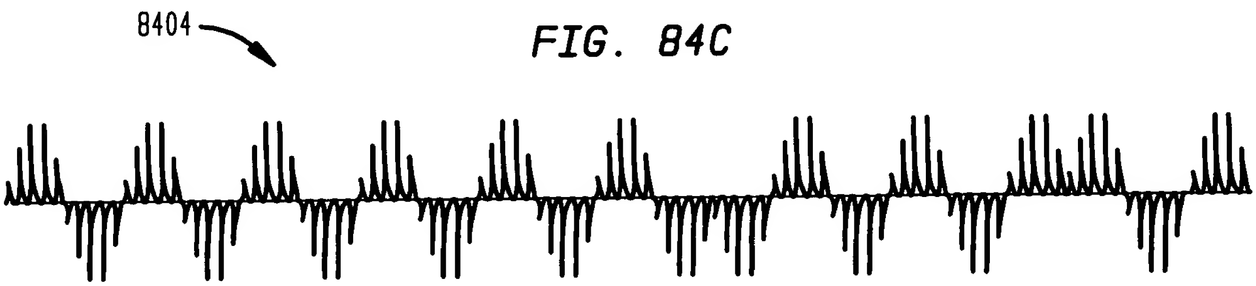
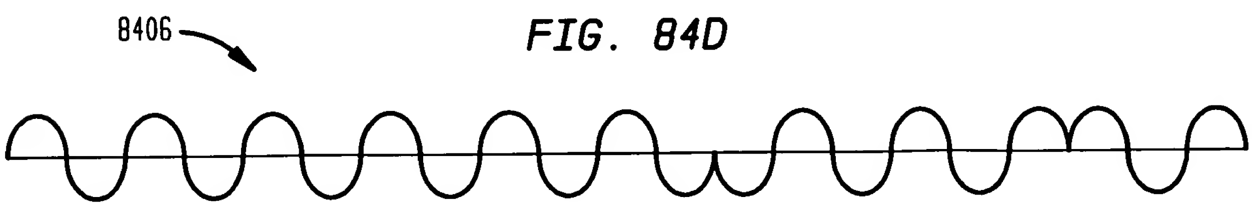


FIG. 84D



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Inventors: SORRELLS et al.
Tel. No.: 202-371-2600
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FIG. 85A

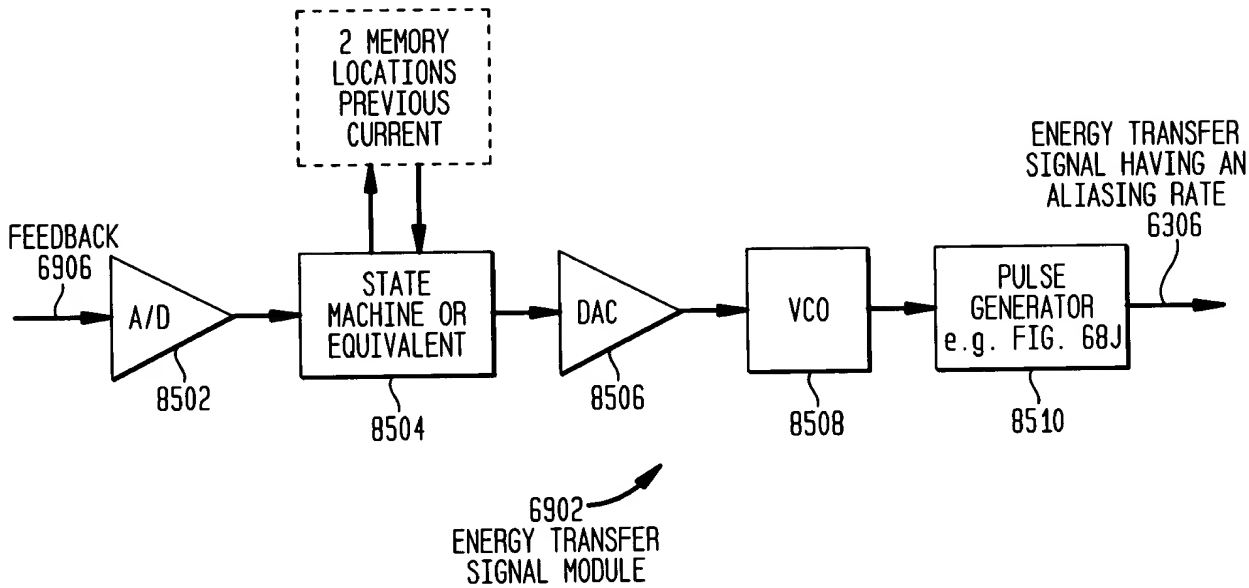
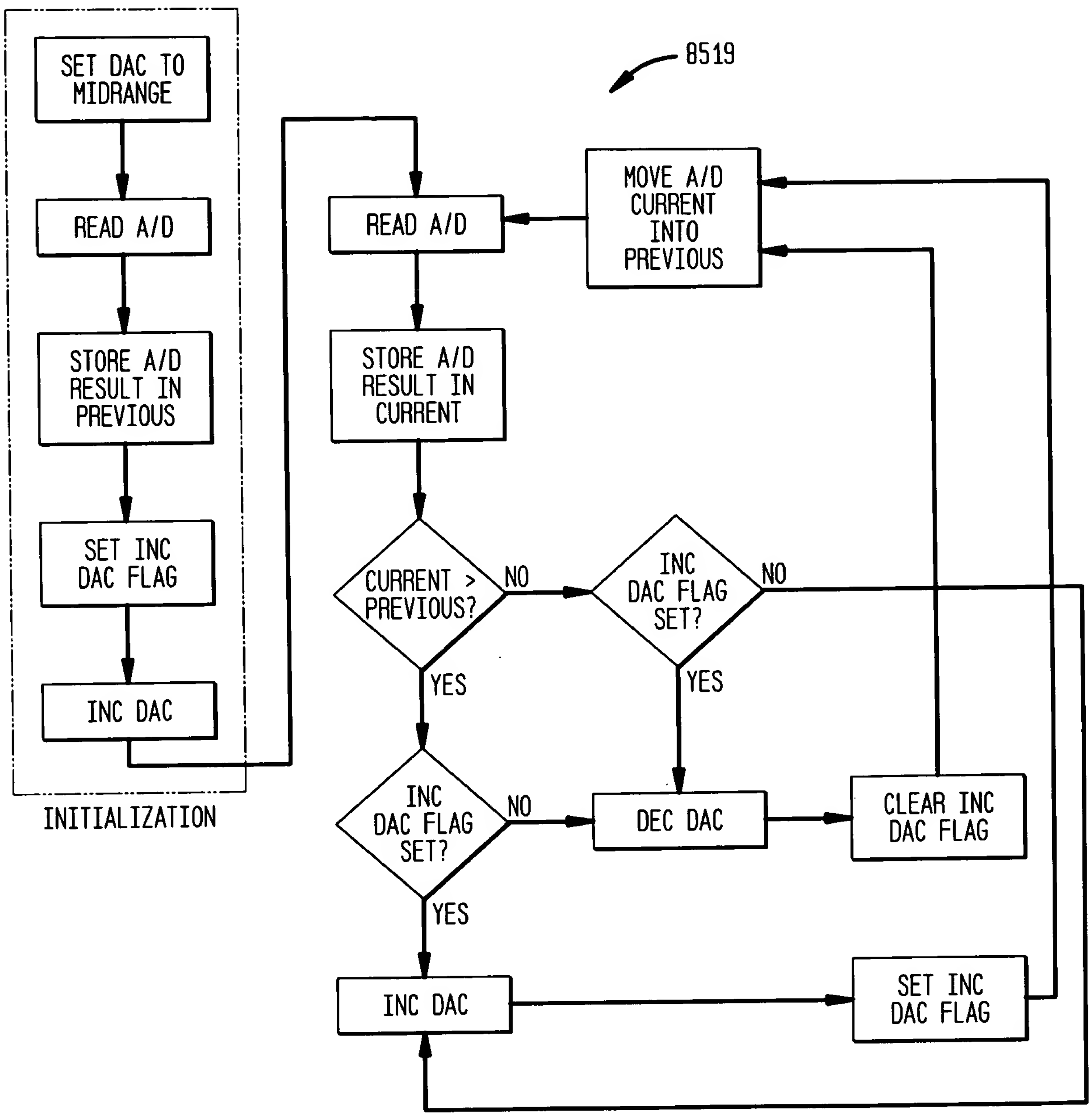
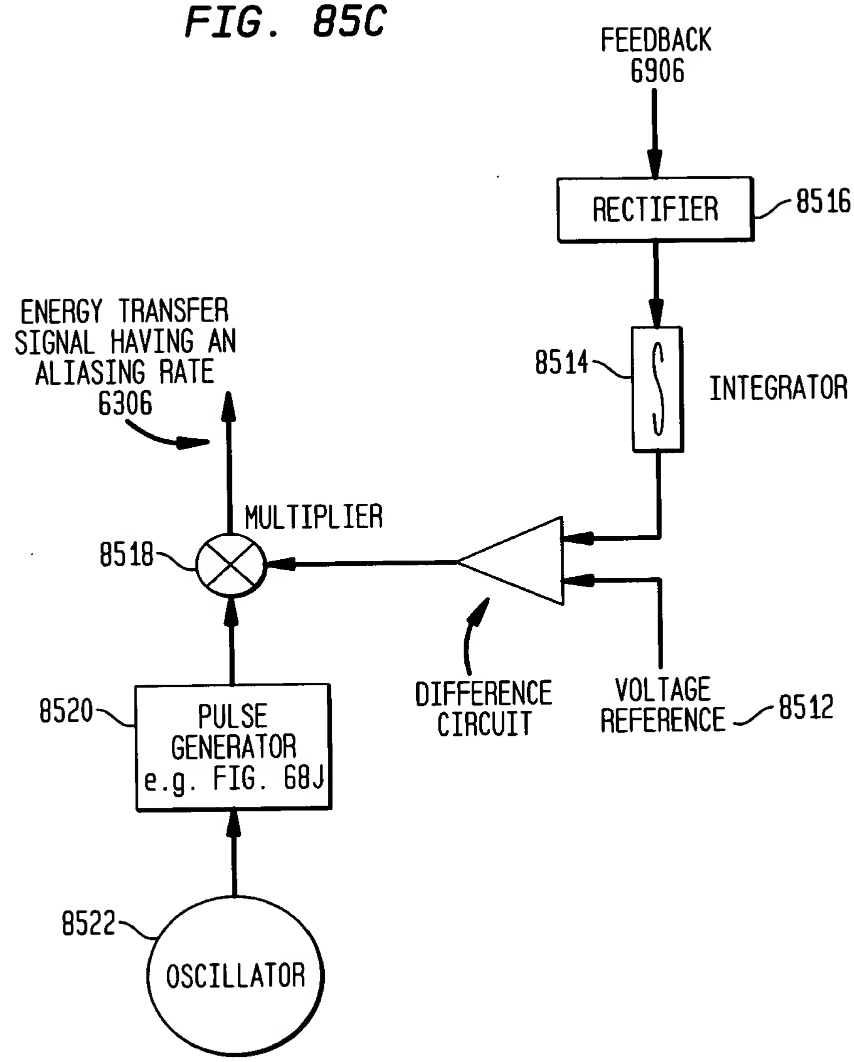


FIG. 85B



STATE MACHINE FLOWCHART

FIG. 85C



ENERGY TRANSFER SIGNAL MODULE 6902

Appl. No. 09/550,642; Filed: Apr 14, 2000
Dkt No. 1744.0920001; Group Unit: 2634
Inventors: SORRELLS et al.
Tel. No.: 202-371-2600
For: Method and System for Down-Converting an Electromagnetic Signal, and Transforms for Same

FIG. 86

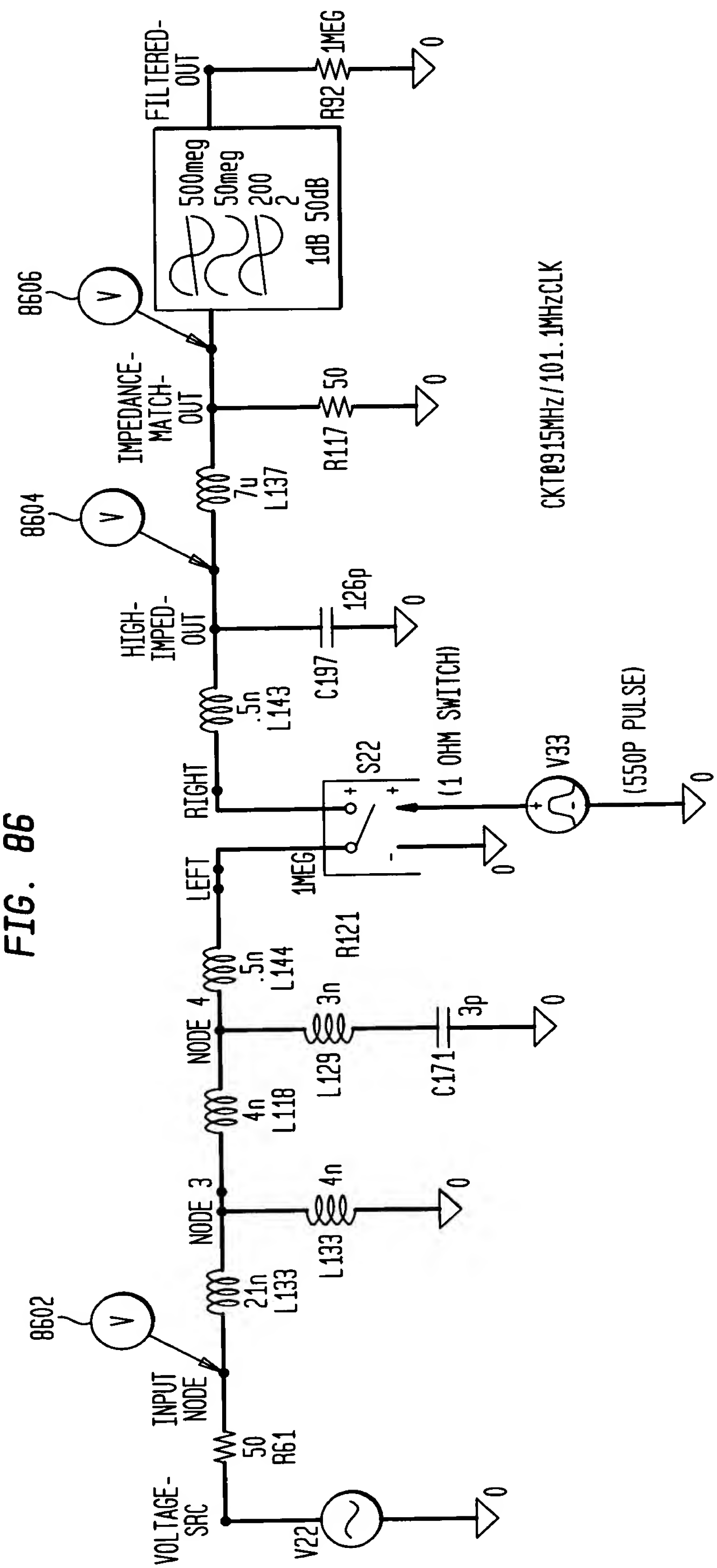
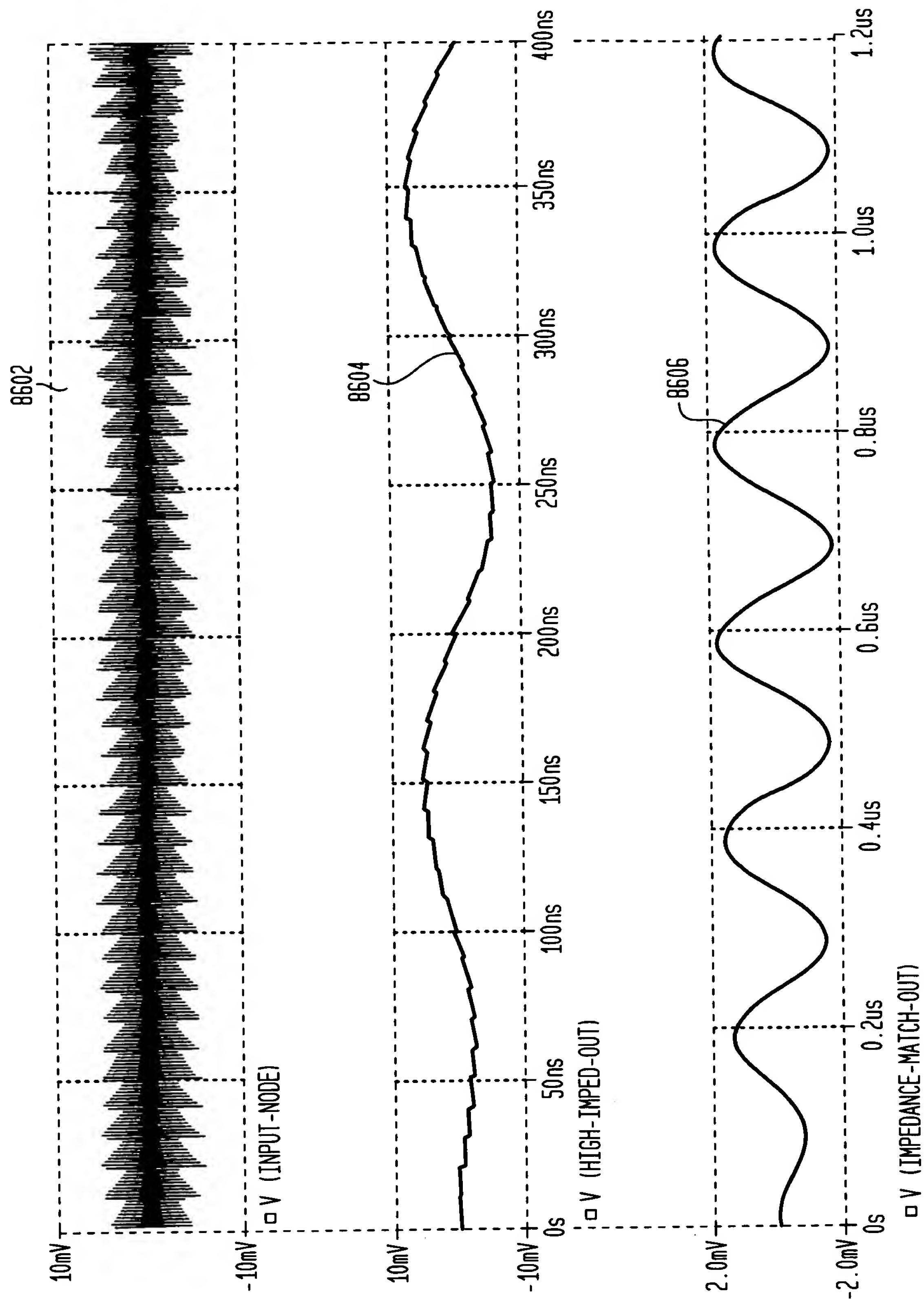


FIG. 87


8602
8604
8606
10mV
-10mV
V (INPUT-NODE)
V (HIGH-IMPED-OUT)
2.0mV
-2.0mV
V (IMPEDANCE-MATCH-OUT)
0s
50ns
100ns
150ns
200ns
250ns
300ns
350ns
400ns
0.2us
0.4us
0.6us
0.8us
1.0us
1.2us

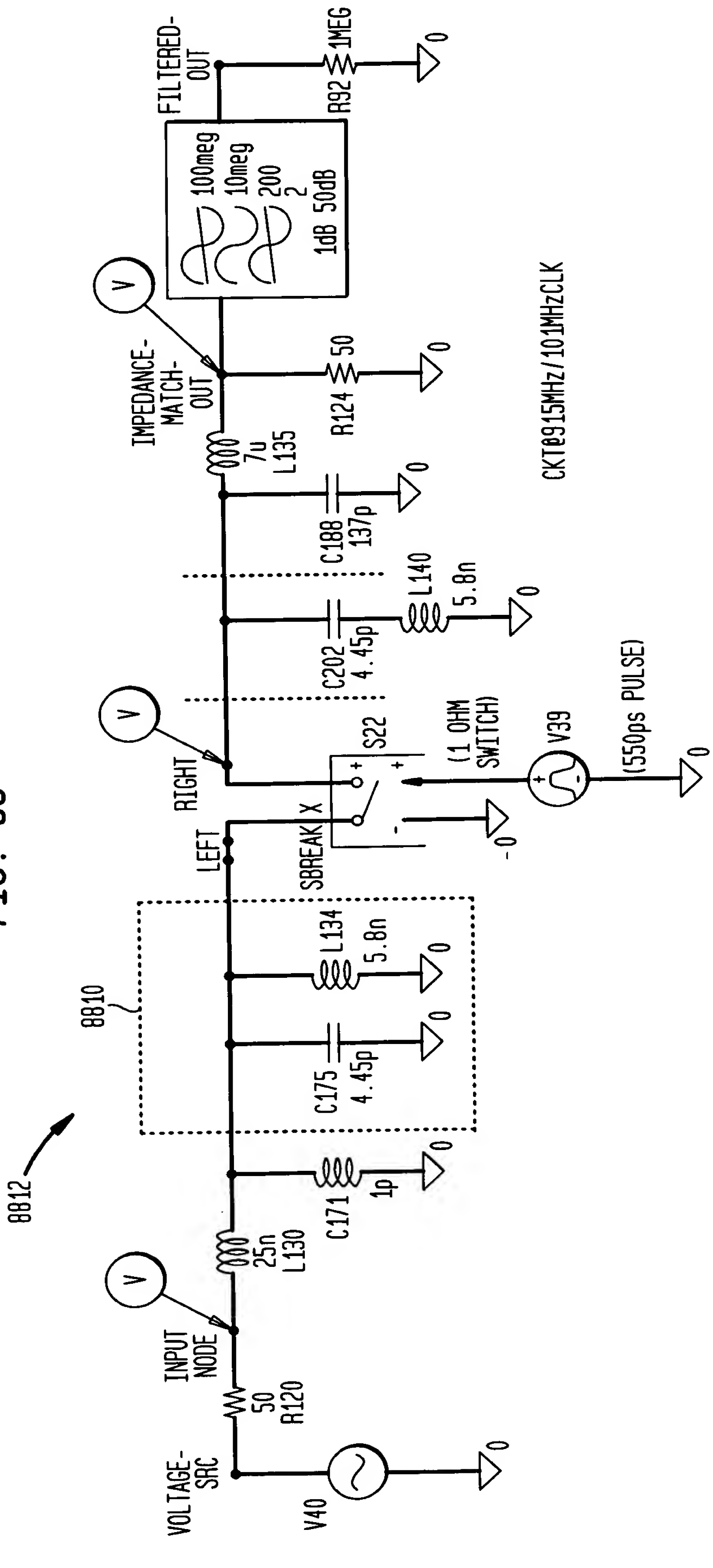
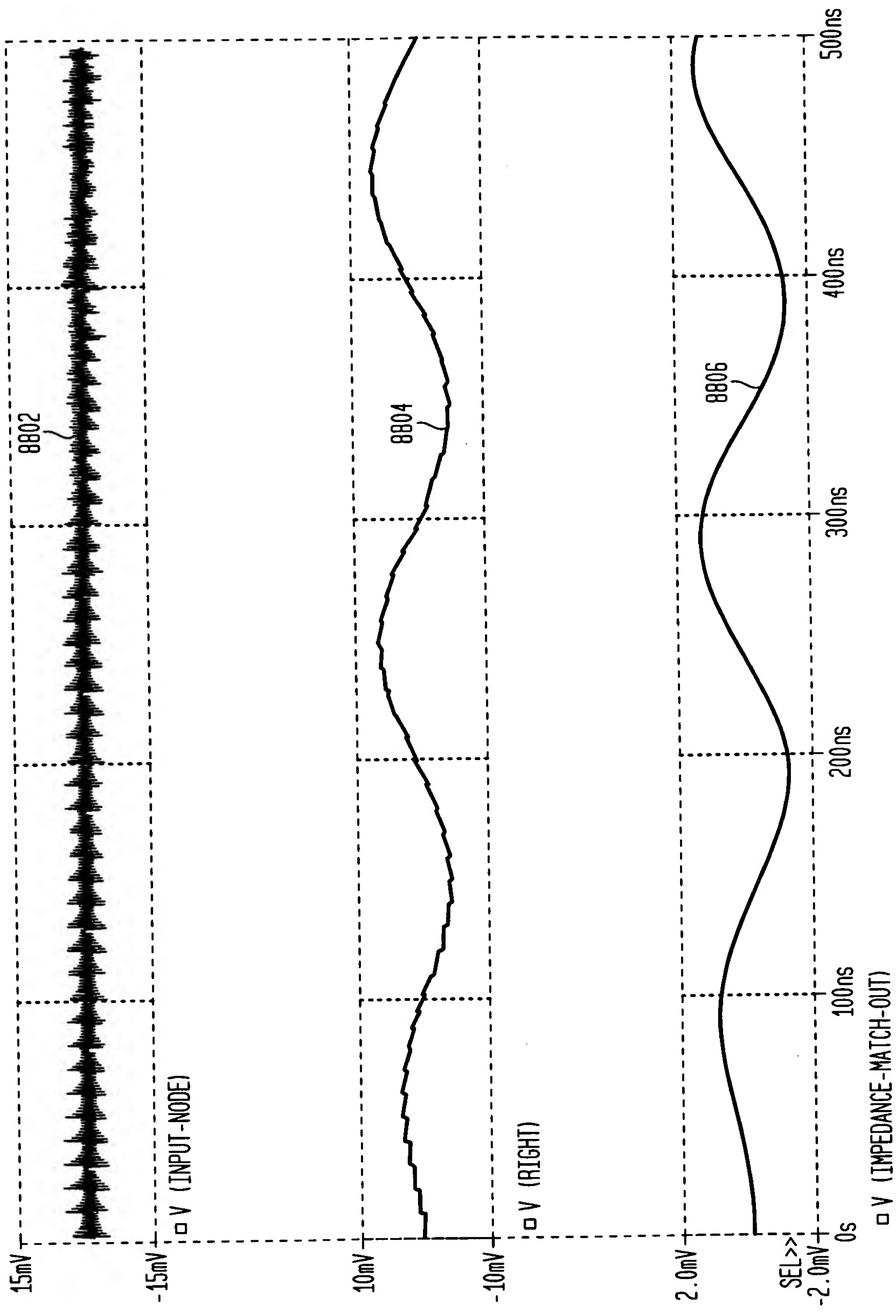

VOLTAGE-SRC
V40
0
50
R120
INPUT NODE
V
25n
L130
8812
C171
1p
0
8810
C175
4.45p
0
L134
5.8n
0
LEFT
SBREAK
X
S22
+
-
-0
(1 OHM SWITCH)
V39
(550ps PULSE)
0
RIGHT
V
C202
4.45p
L140
5.8n
0
C188
137p
0
7u
L135
IMPEDANCE-MATCH-OUT
V
R124
50
0
100meg
10meg
200
2
1dB 50dB
FILTERED-OUT
R92
1MEG
0
CKT@915MHz/101MHzCLK

FIG. 88

FIG. 89


15mV
-15mV
□ V (INPUT-NODE)
8802
10mV
-10mV
□ V (RIGHT)
8804
2.0mV
SEL>>
-2.0mV
□ V (IMPEDANCE-MATCH-OUT)
8806
0s
100ns
200ns
300ns
400ns
500ns

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Tel. No.: 202-371-2600
For: Method and System for Down-Converting an Electromagnetic Signal, and Transforms for Same

FIG. 90

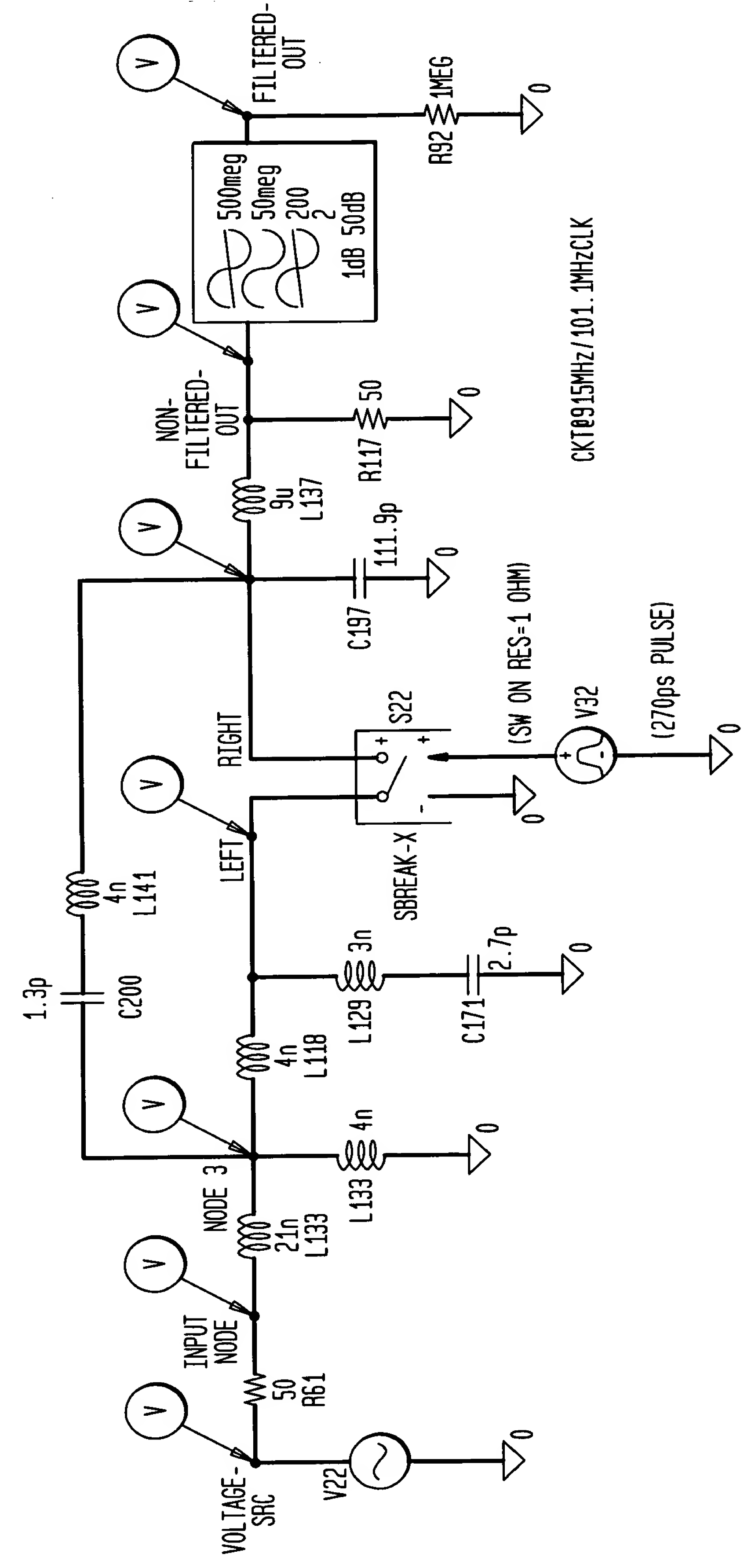
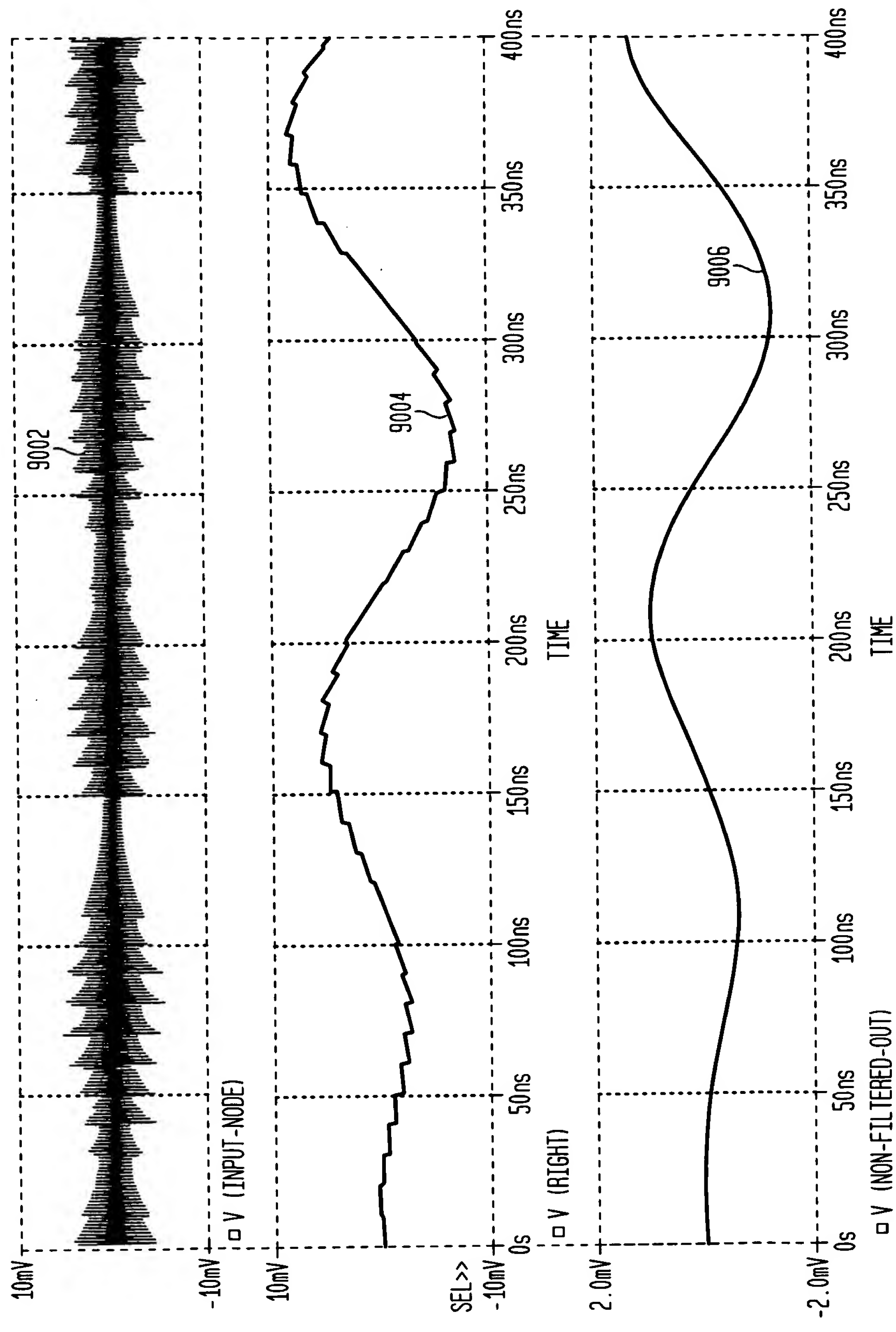


FIG. 91


10mV
-10mV
□ V (INPUT-NODE)
9002
10mV
SEL>>
-10mV
□ V (RIGHT)
9004
0s
50ns
100ns
150ns
200ns
250ns
300ns
350ns
400ns
TIME
2.0mV
-2.0mV
□ V (NON-FILTERED-OUT)
9006
TIME

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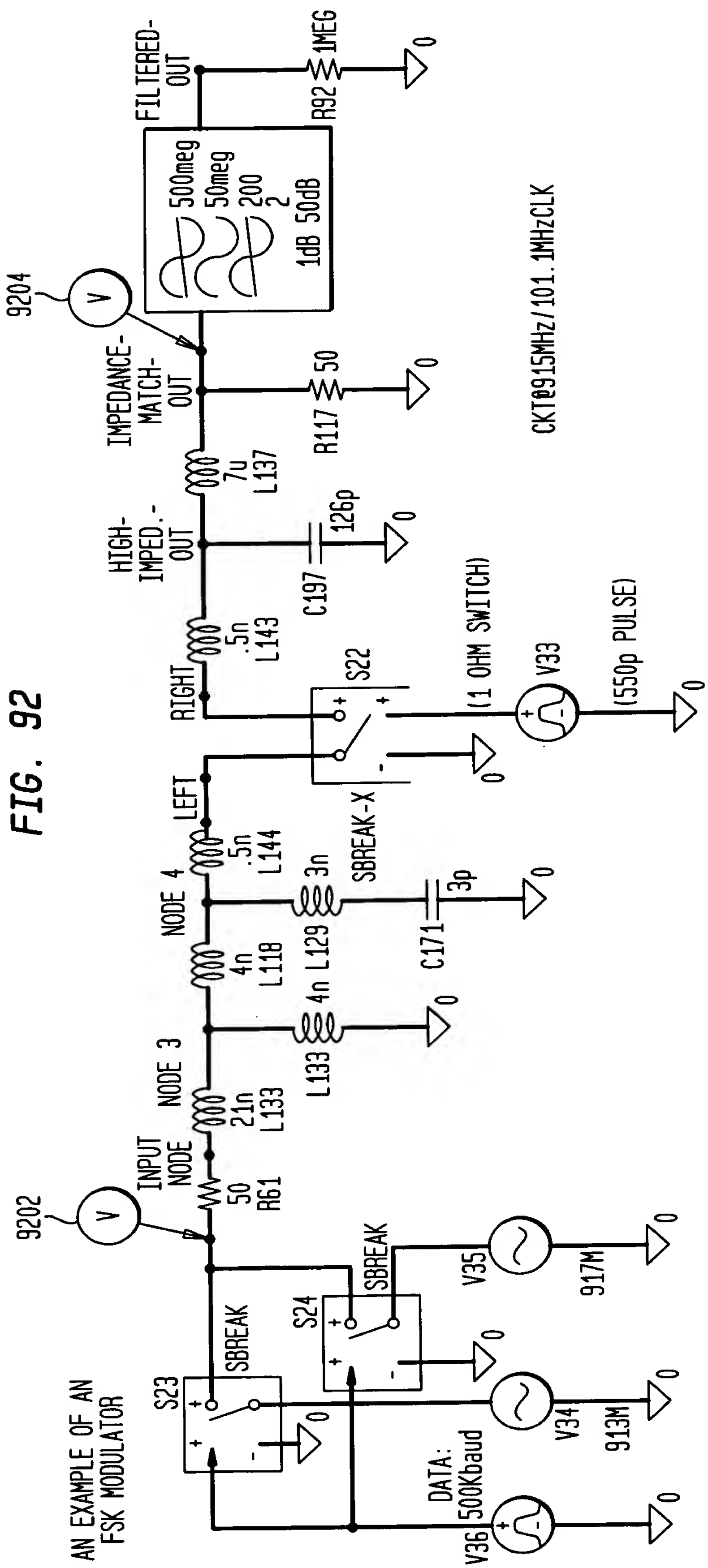
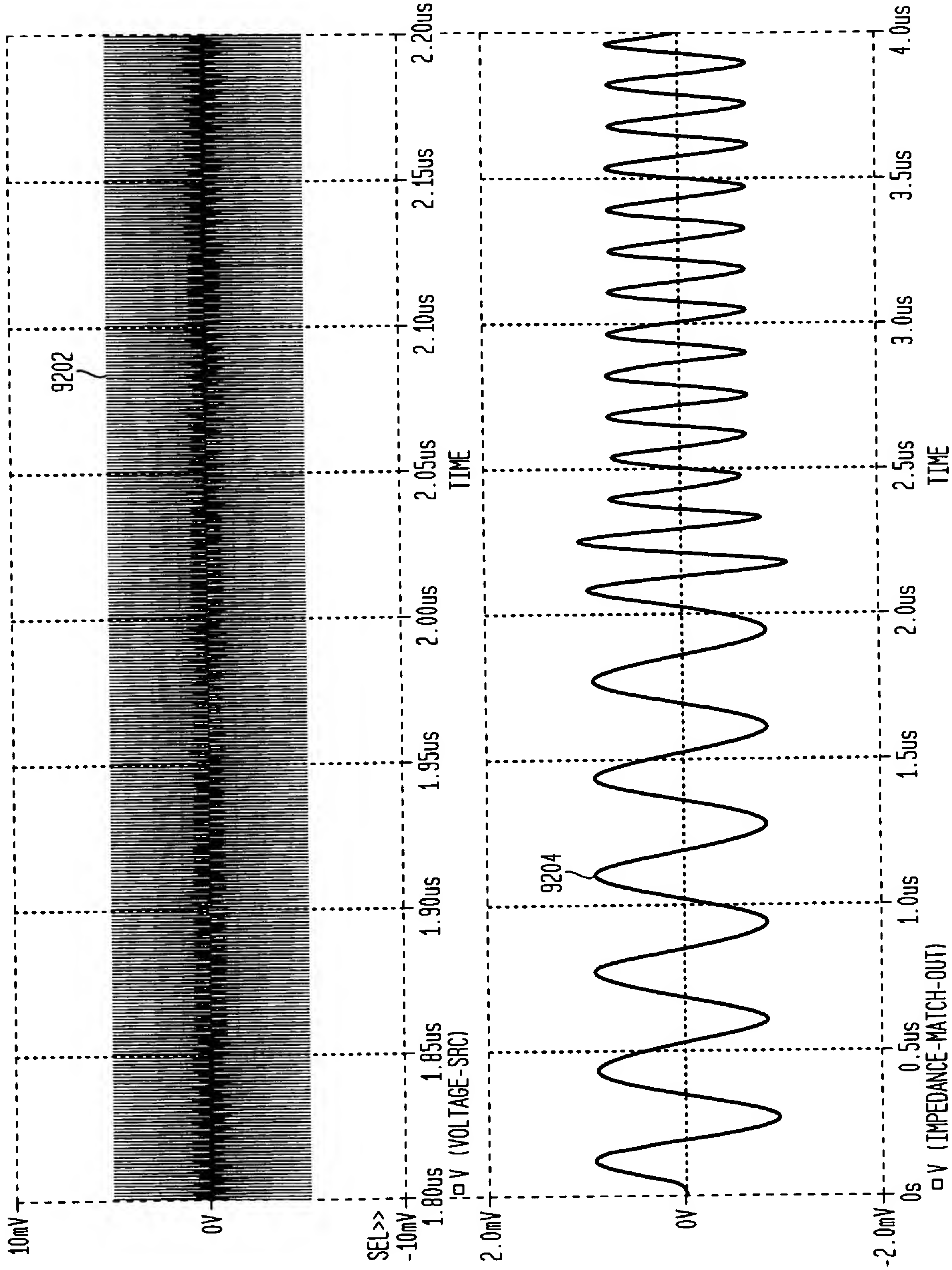


FIG. 92

FIG. 93


9202
10mV
0V
SEL>>
-10mV
1.80us
1.85us
1.90us
1.95us
2.00us
2.05us
2.10us
2.15us
2.20us
TIME
□ V (VOLTAGE-SRC)
9204
2.0mV
0V
-2.0mV
0s
0.5us
1.0us
1.5us
2.0us
2.5us
3.0us
3.5us
4.0us
TIME
□ V (IMPEDANCE-MATCH-OUT)

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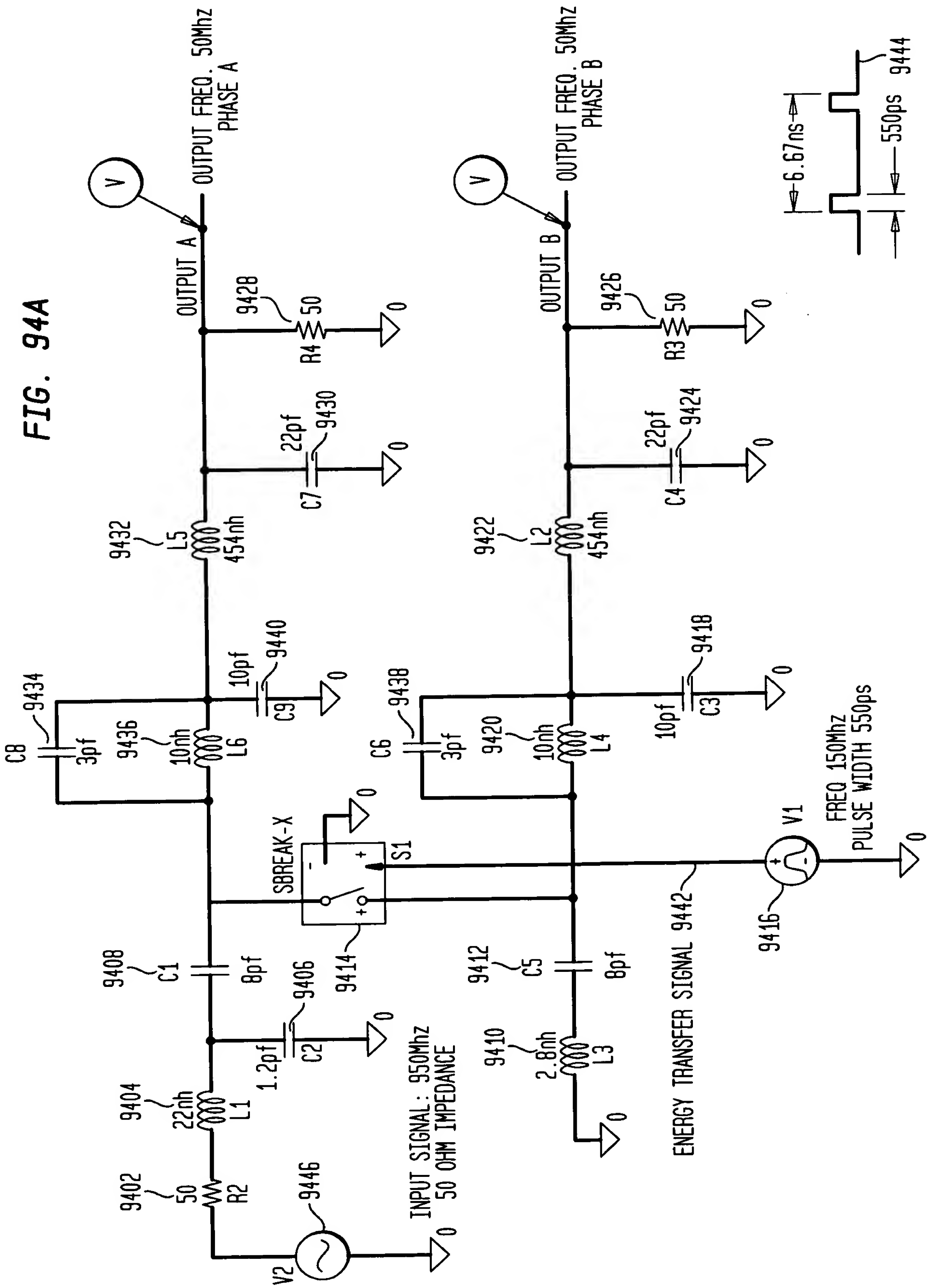

FIG. 94A

FIG. 94B

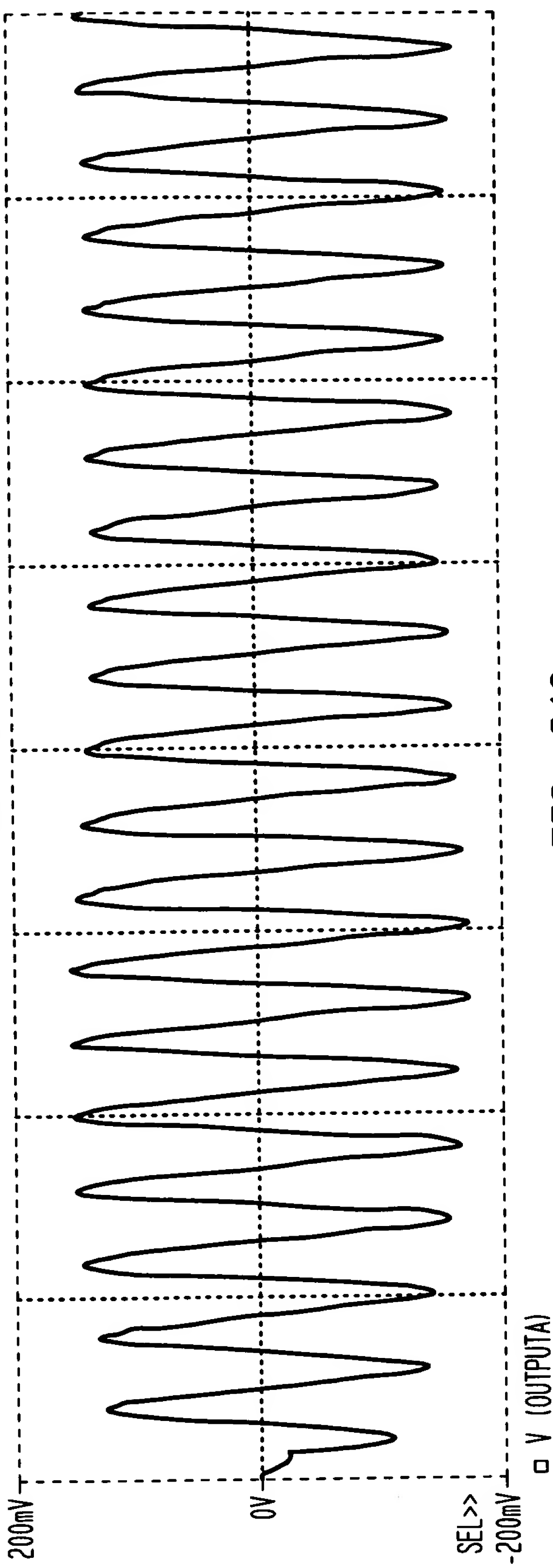

FIG. 94C

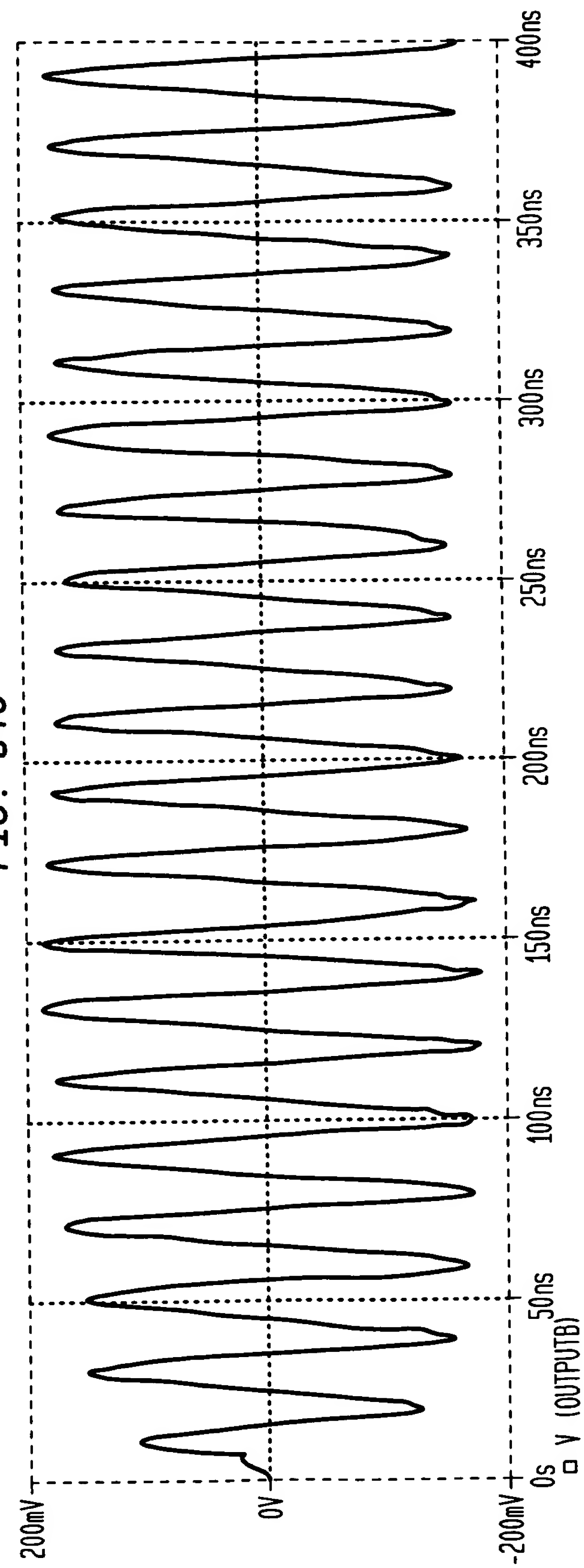

FIG. 95

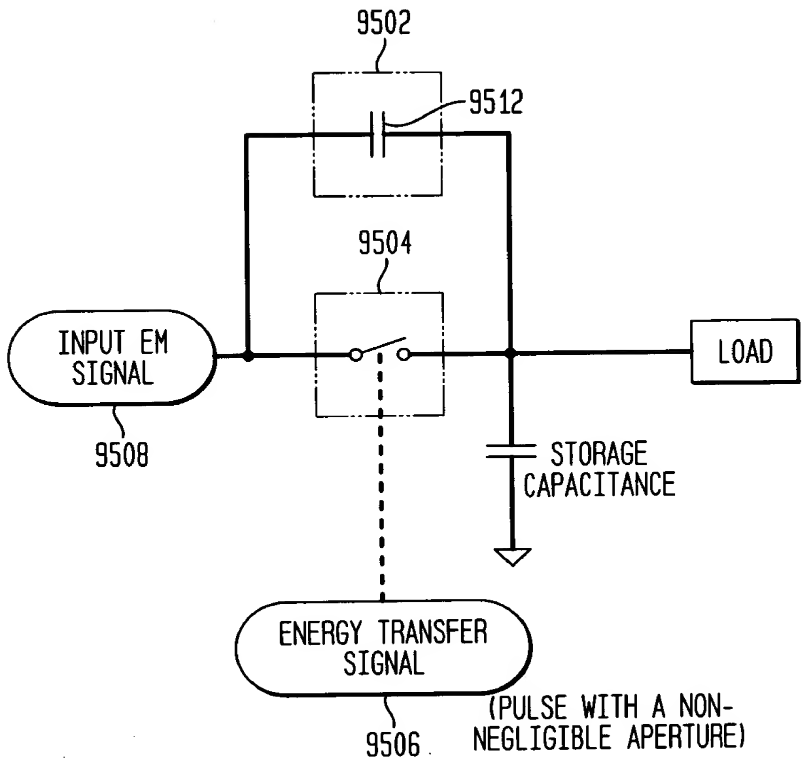
9502
9512
9504
INPUT EM SIGNAL
LOAD
9508
STORAGE CAPACITANCE
ENERGY TRANSFER SIGNAL
(PULSE WITH A NON-NEGLIGIBLE APERTURE)
9506

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FIG. 96

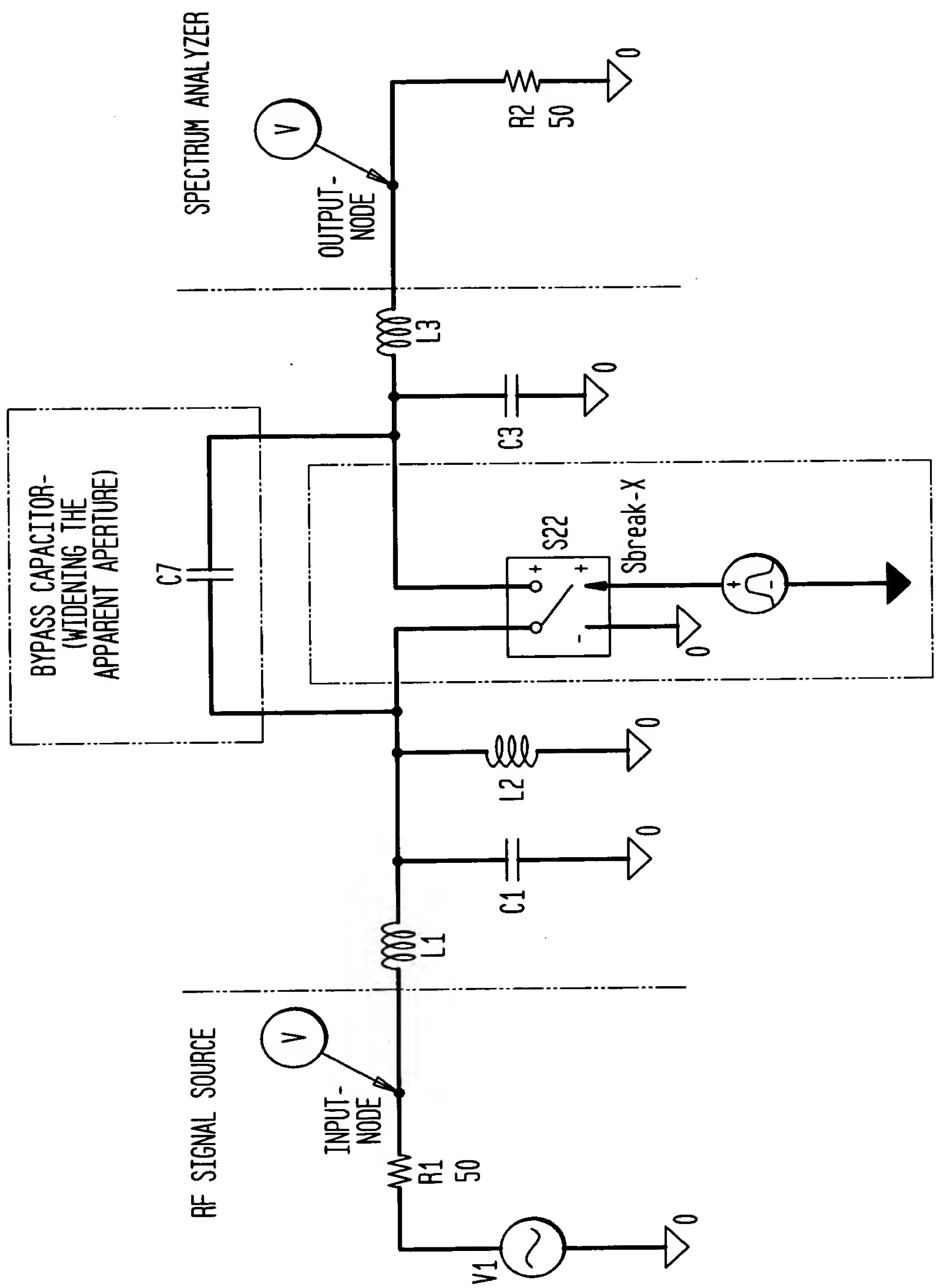

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FIG. 97

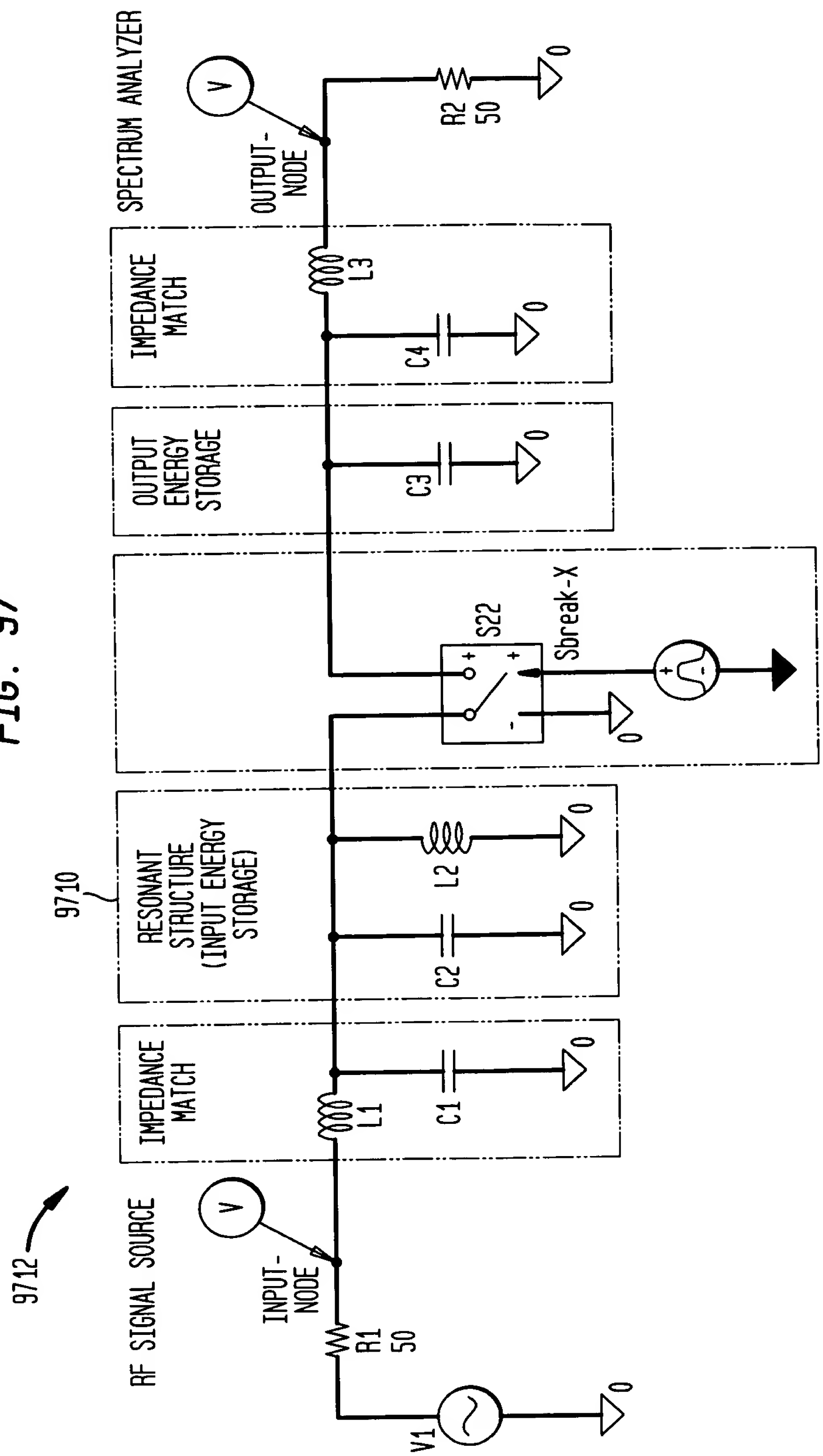
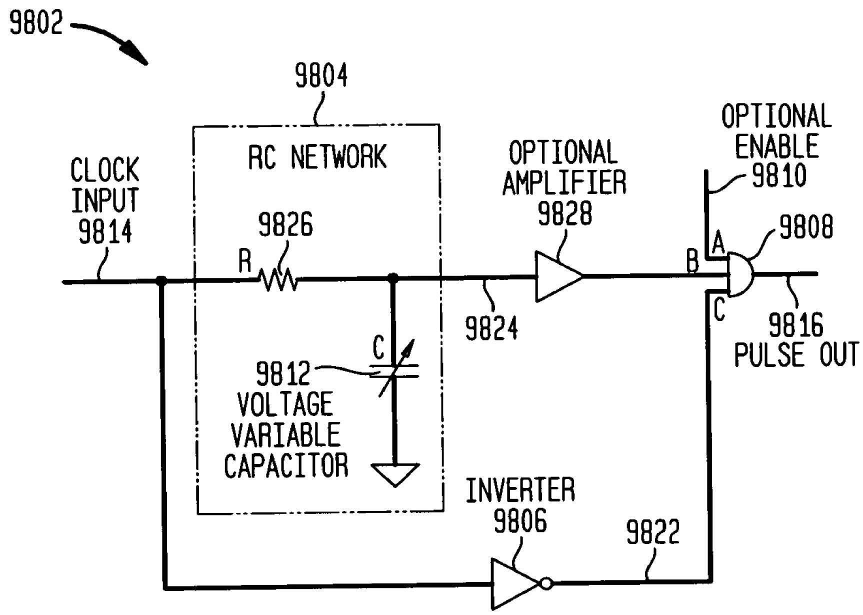


FIG. 98A


9802
9804
RC NETWORK
CLOCK
INPUT
9814
9826
R
C
9812
VOLTAGE
VARIABLE
CAPACITOR
9824
OPTIONAL
AMPLIFIER
9828
OPTIONAL
ENABLE
9810
A
B
C
9808
9816
PULSE OUT
INVERTER
9806
9822

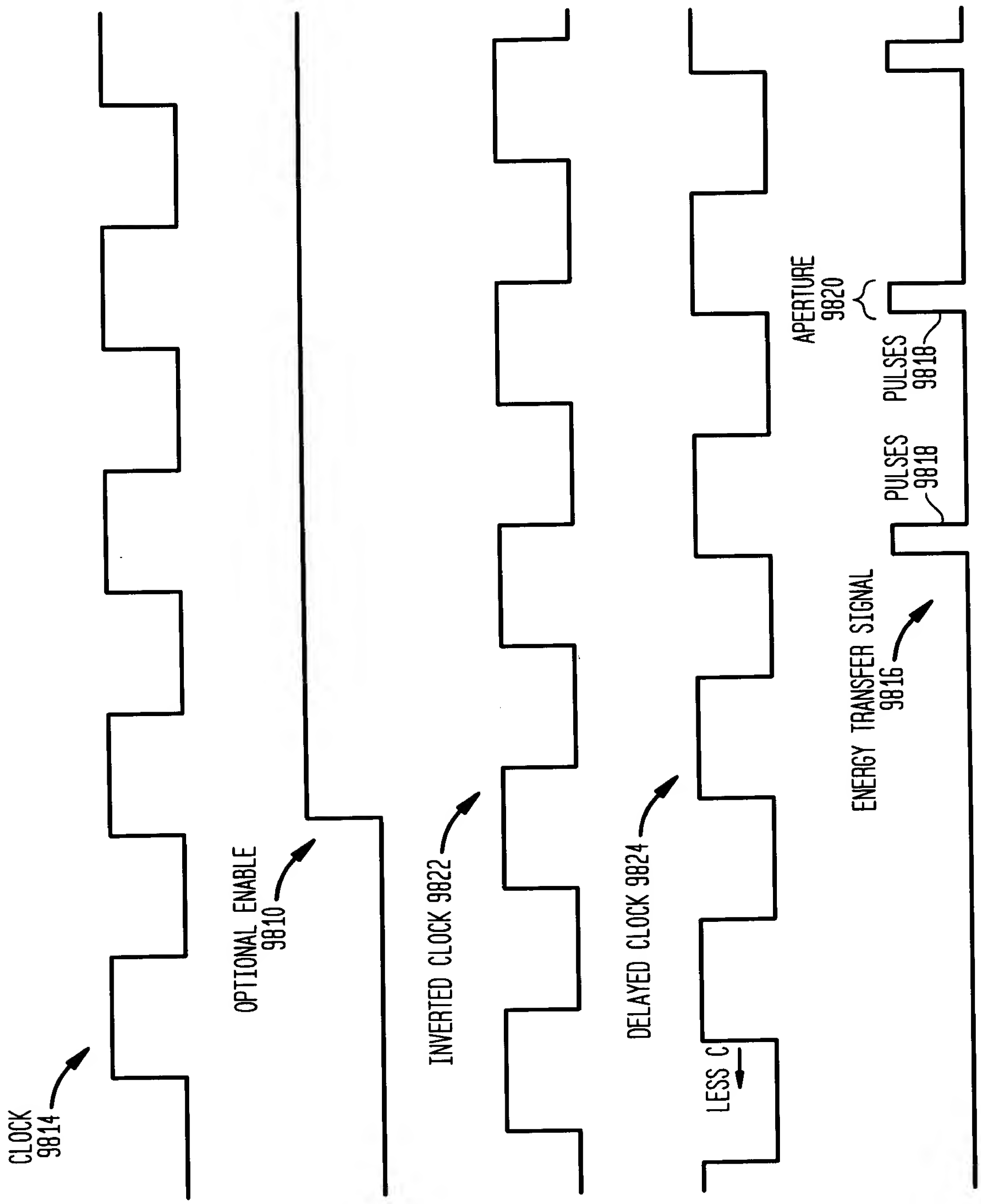


FIG. 98B

FIG. 98C

FIG. 98D

FIG. 98E

FIG. 98F

FIG. 99

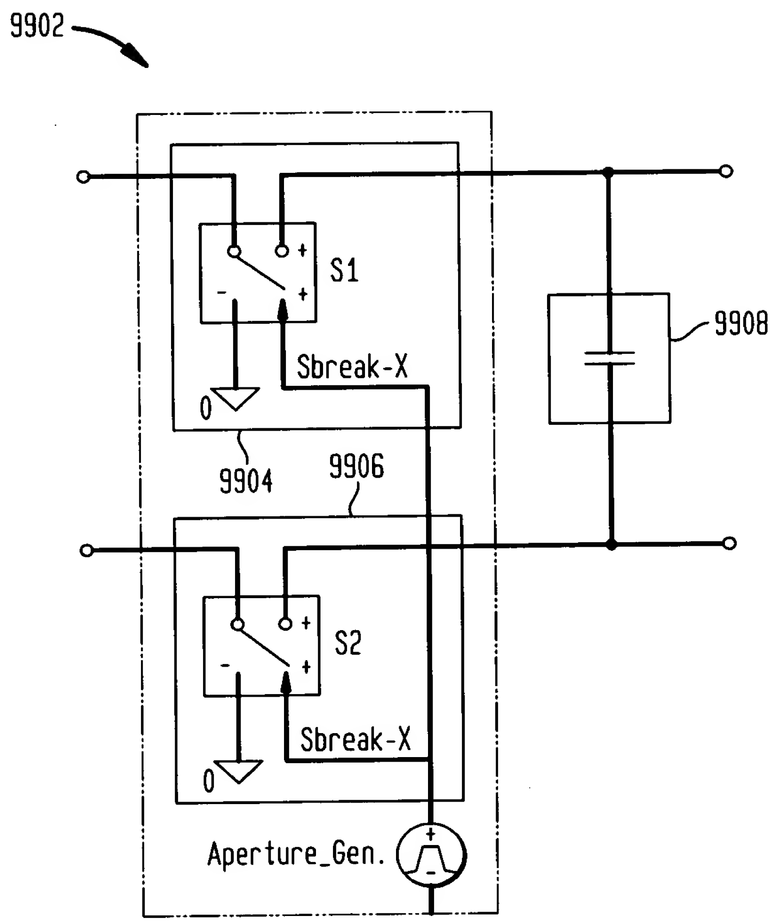


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FIG. 100

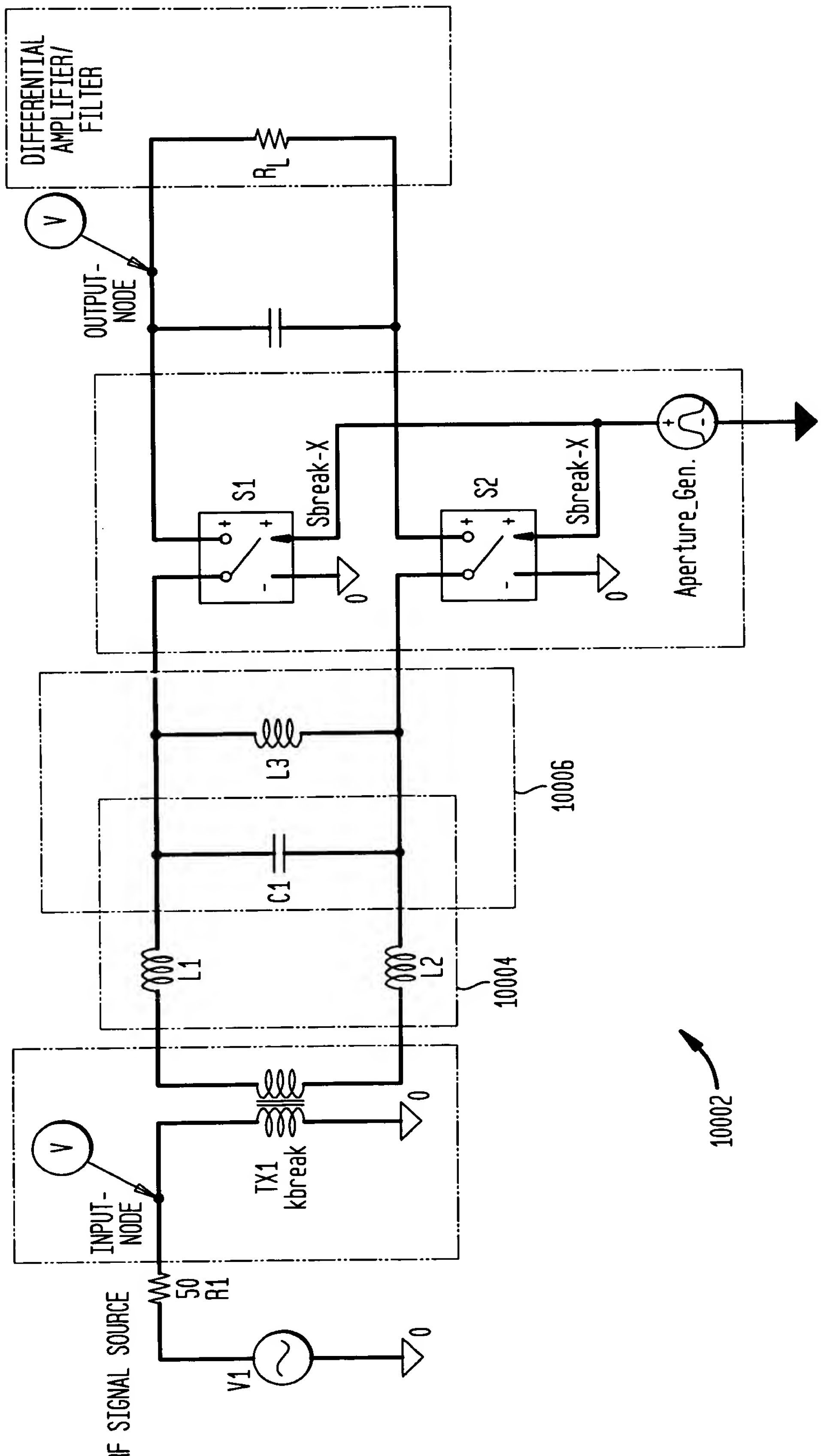

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FIG. 101

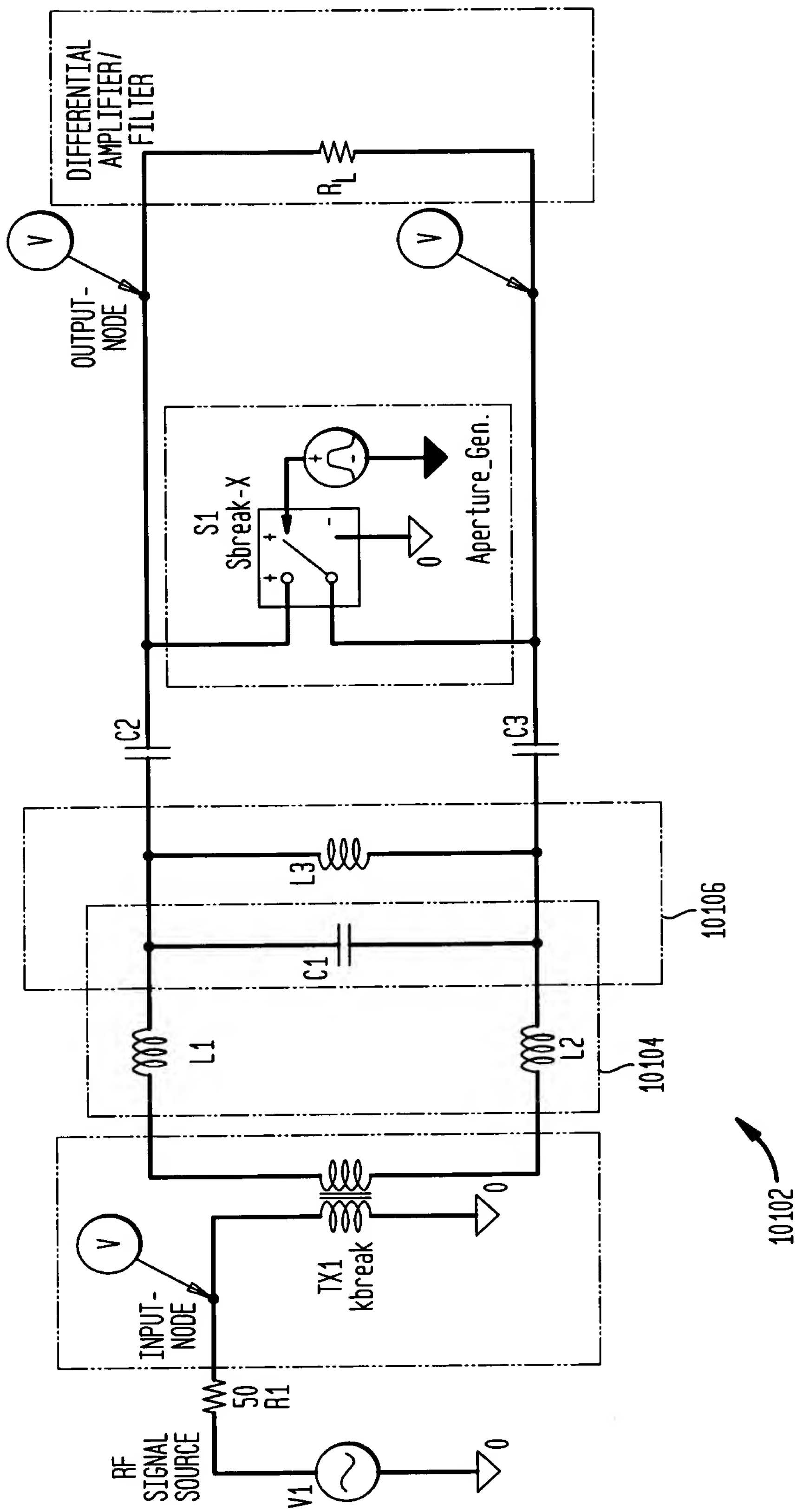

FIG. 102

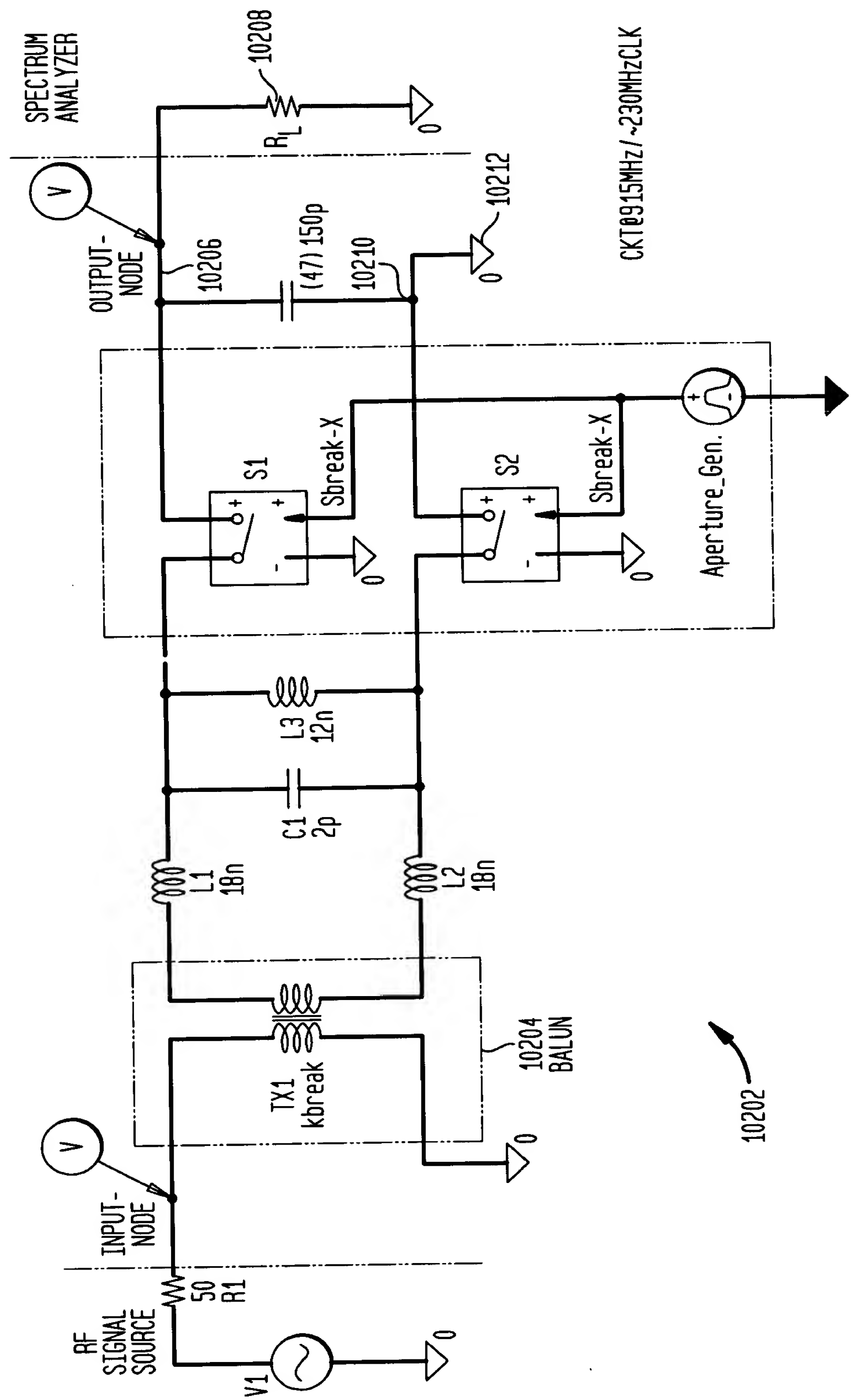
SPECTRUM ANALYZER
10208
R_L
0
V
OUTPUT-NODE
10206
(47) 150p
10210
10212
0
CKT@915MHz/~230MHzCLK
S1
Sbreak-X
0
S2
Sbreak-X
0
Aperture_Gen.
L3
12n
C1
2p
L1
18n
L2
18n
TX1
kbreak
10204
BALUN
0
10202
V
INPUT-NODE
RF SIGNAL SOURCE
50
R1
V1
0

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FIG. 103

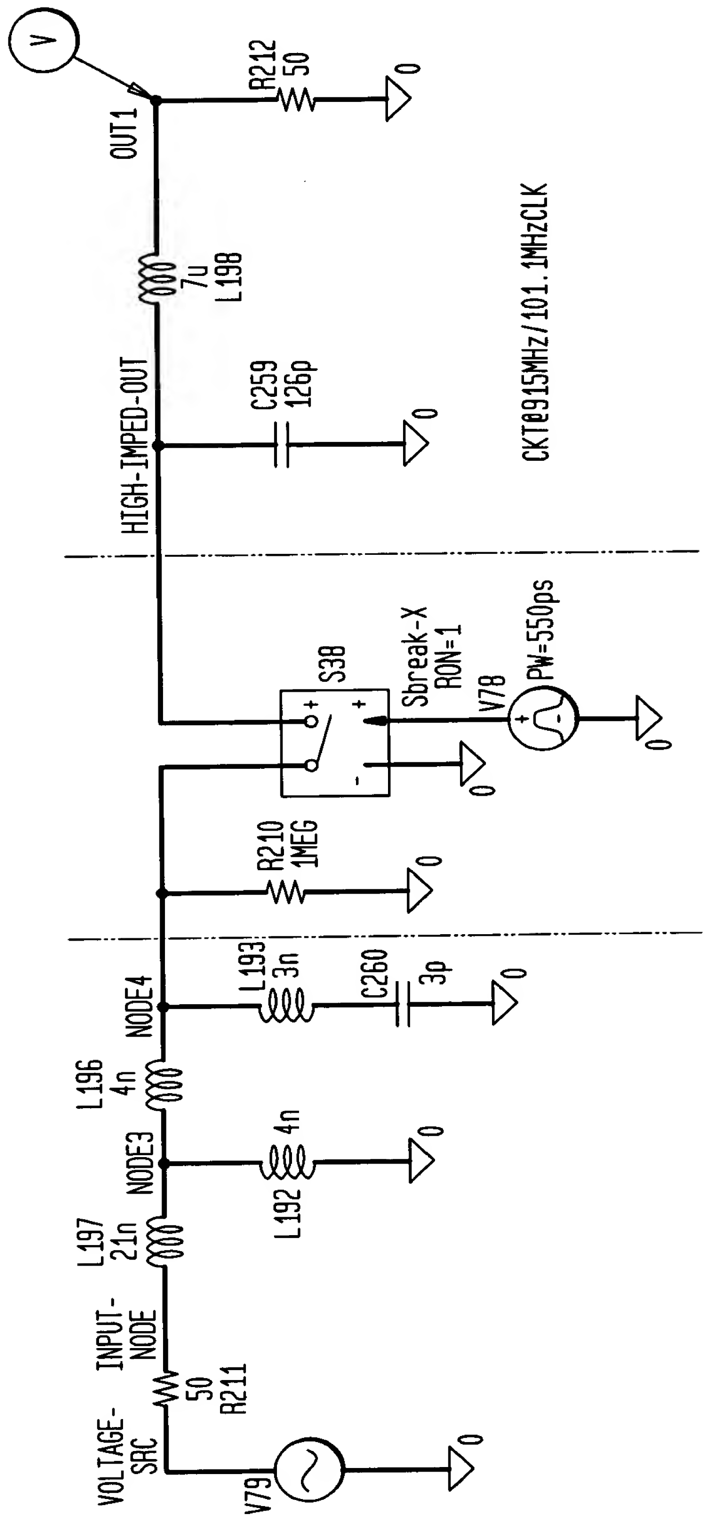

FIG. 104

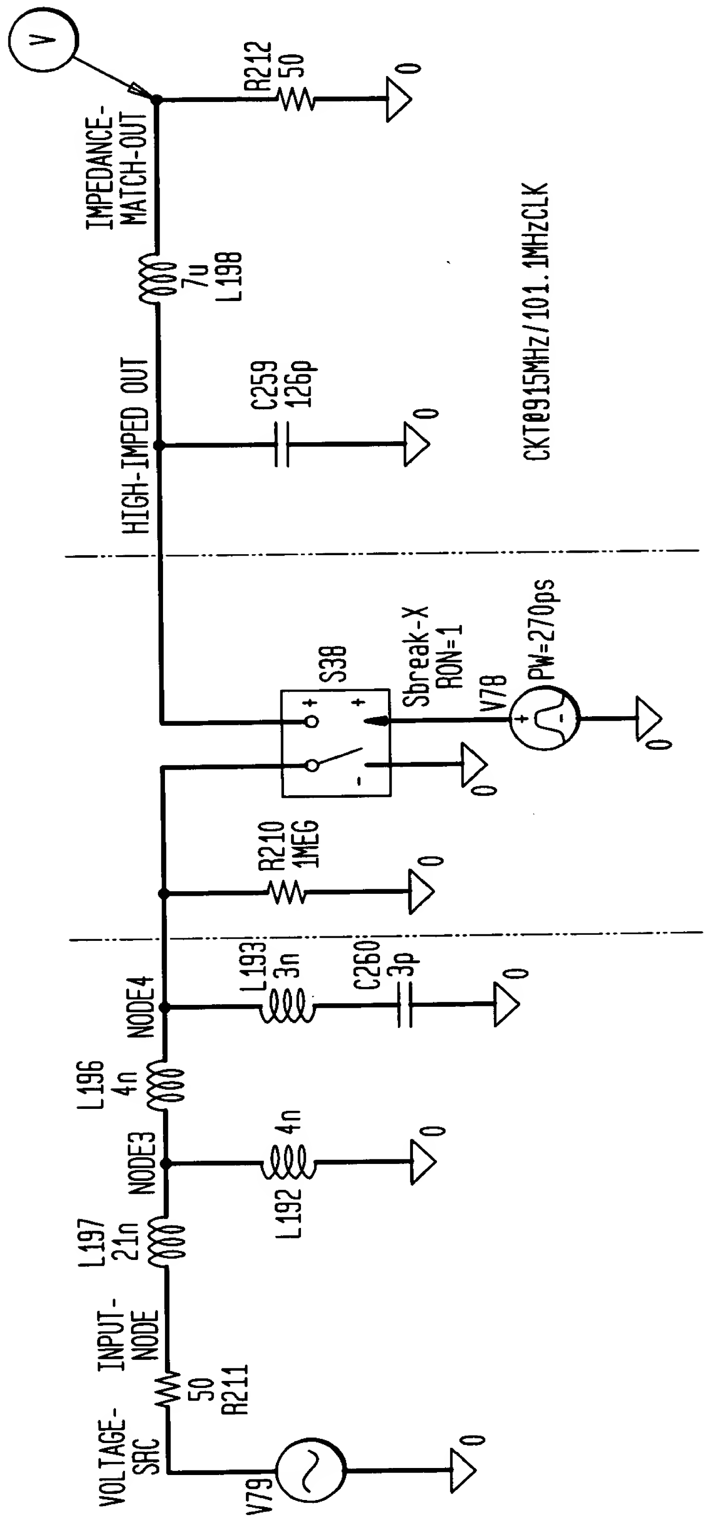
V
IMPEDANCE-
MATCH-OUT
R212
50
0
7u
L198
HIGH-IMPED OUT
C259
126p
0
CKT@915MHz/101.1MHzCLK
S38
Sbreak-X
RON=1
V78
PW=270ps
0
0
R210
1MEG
0
NODE4
L193
3n
C260
3p
0
L196
4n
NODE3
4n
L192
0
L197
21n
INPUT-
NODE
50
R211
VOLTAGE-
SRC
V79
0

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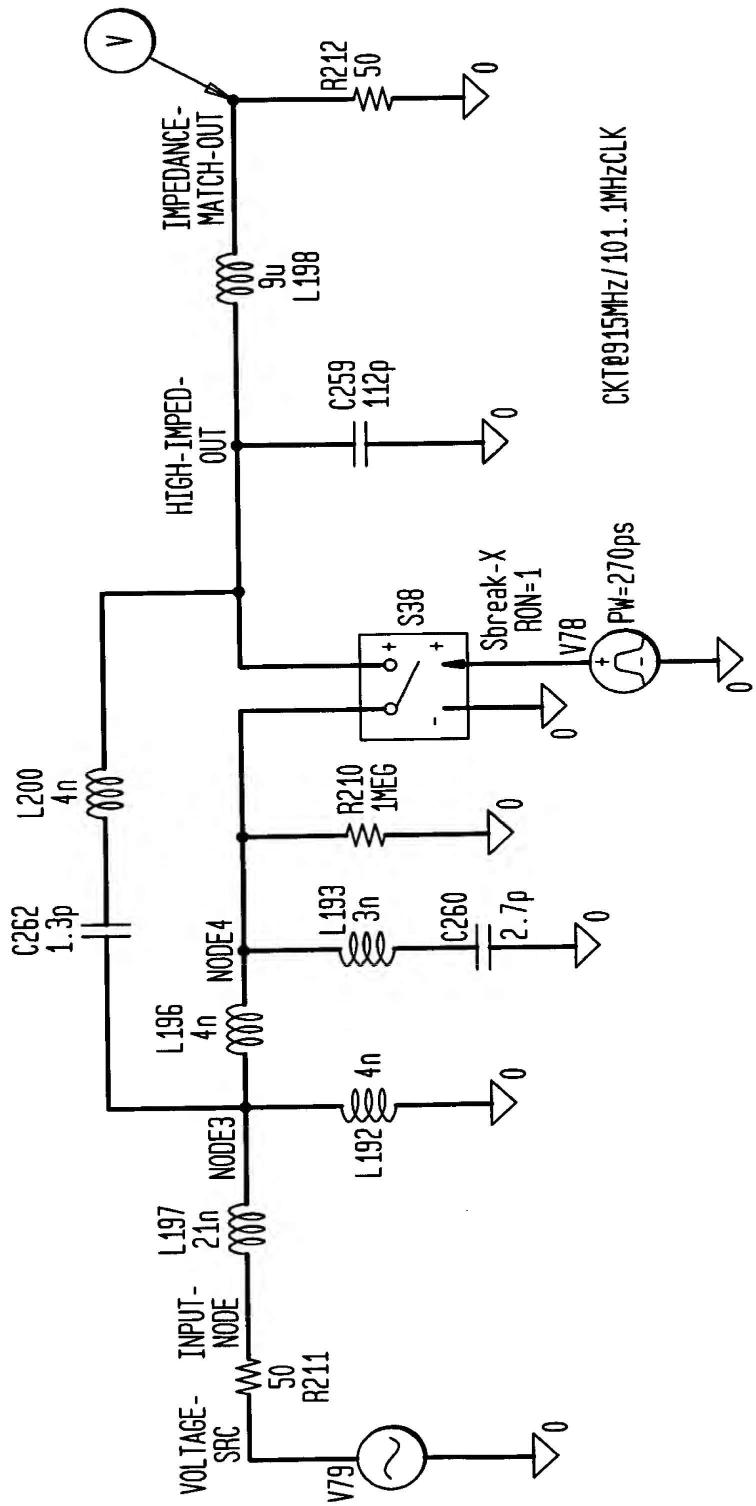
FIG. 105



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Dkt No. 1744.0920001; Group Unit: 2634
Inventors: SORRELLS et al.
Tel. No.: 202-371-2600
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Electromagnetic Signal, and Transforms for Same

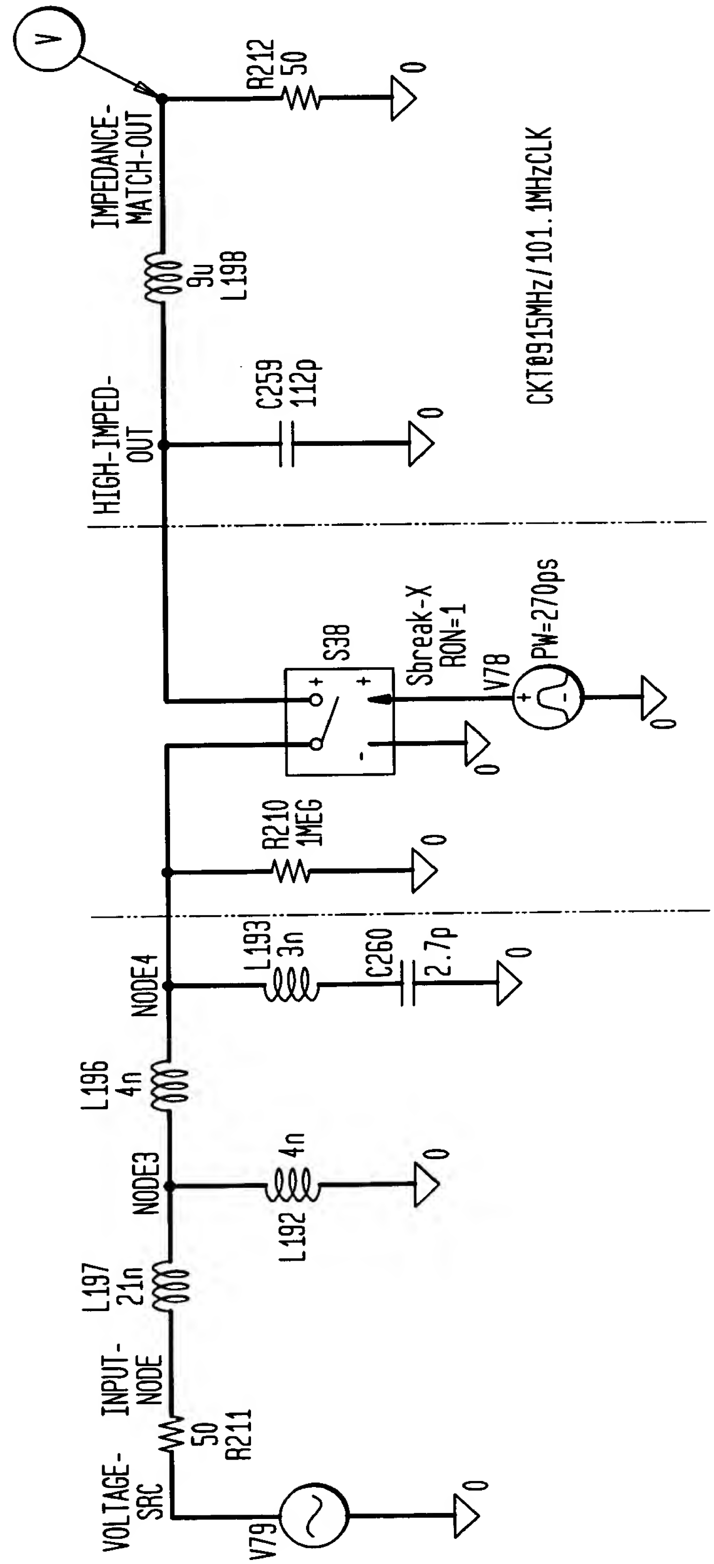

FIG. 106

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FIG. 107A

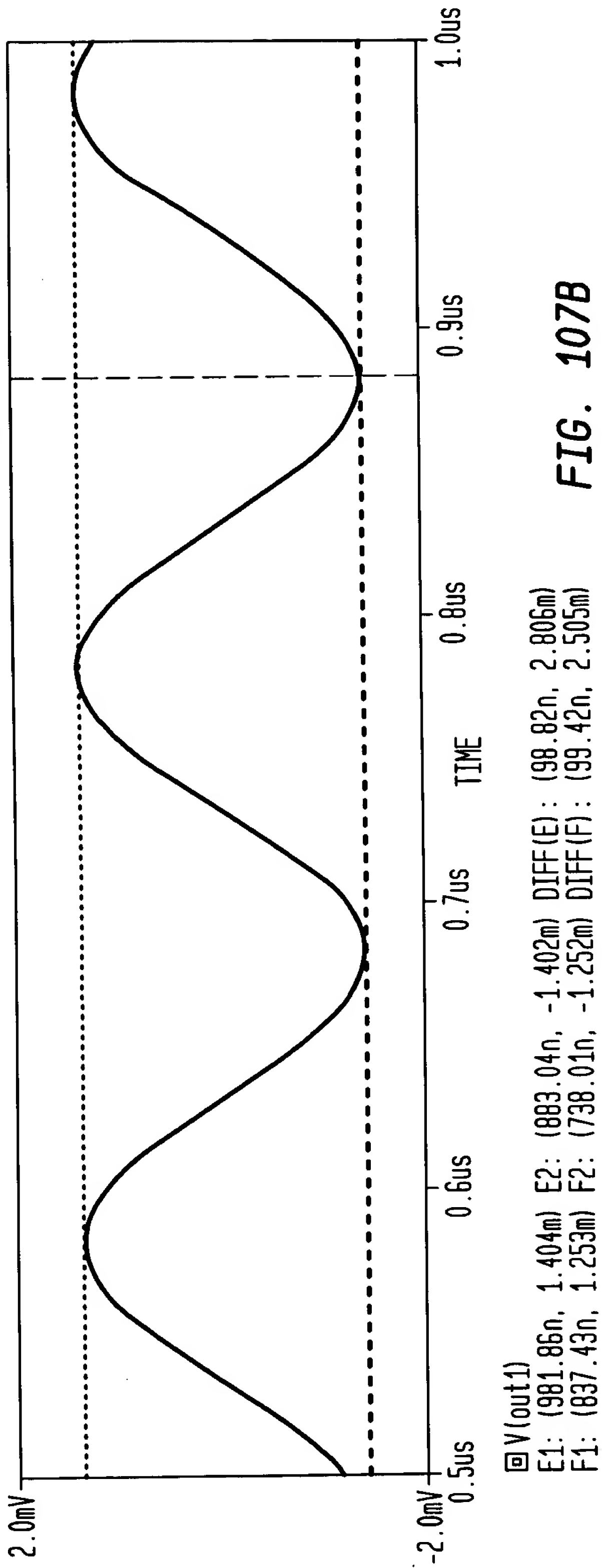
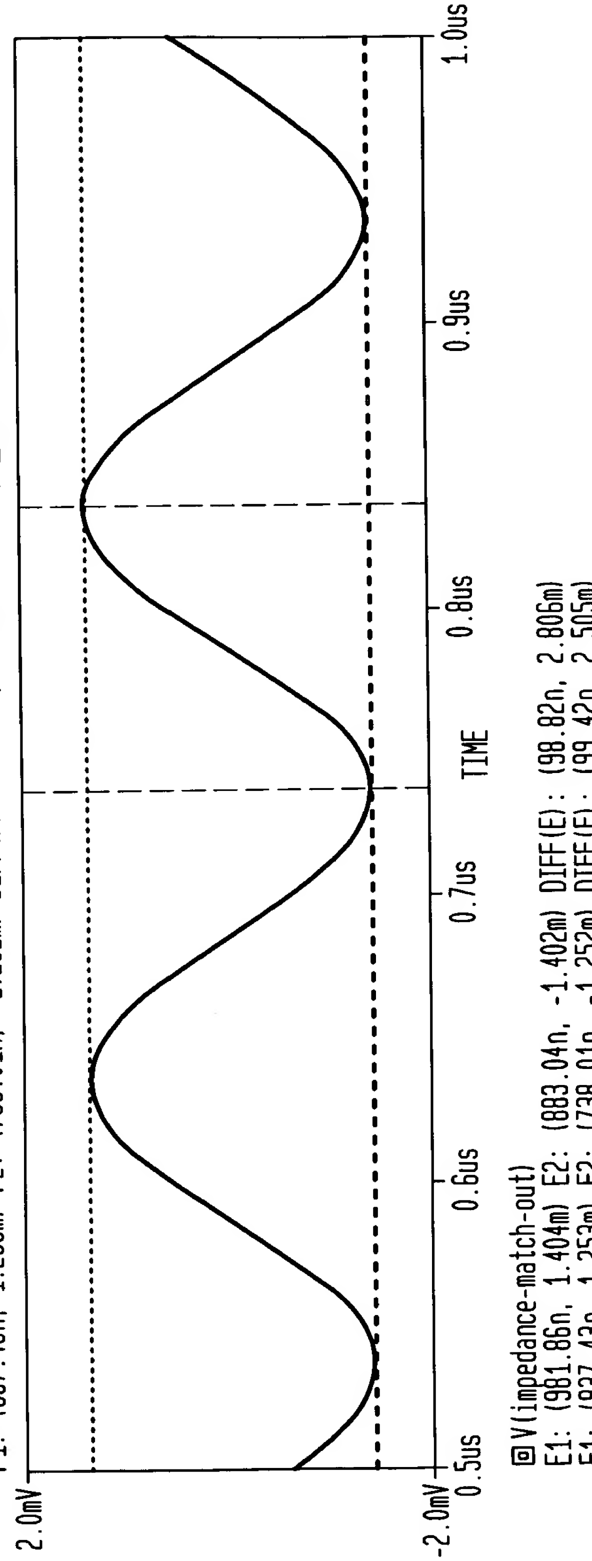


FIG. 107B



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Inventors: SORRELLS et al.
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FIG. 108A

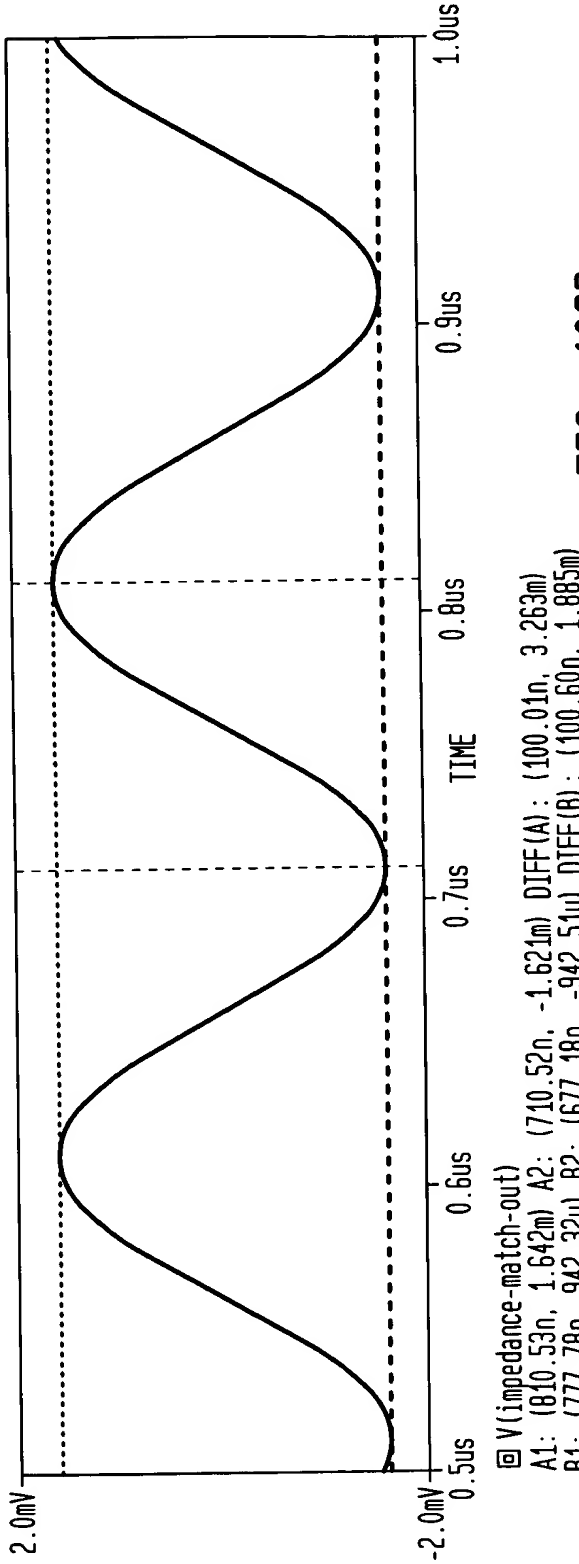

FIG. 108B

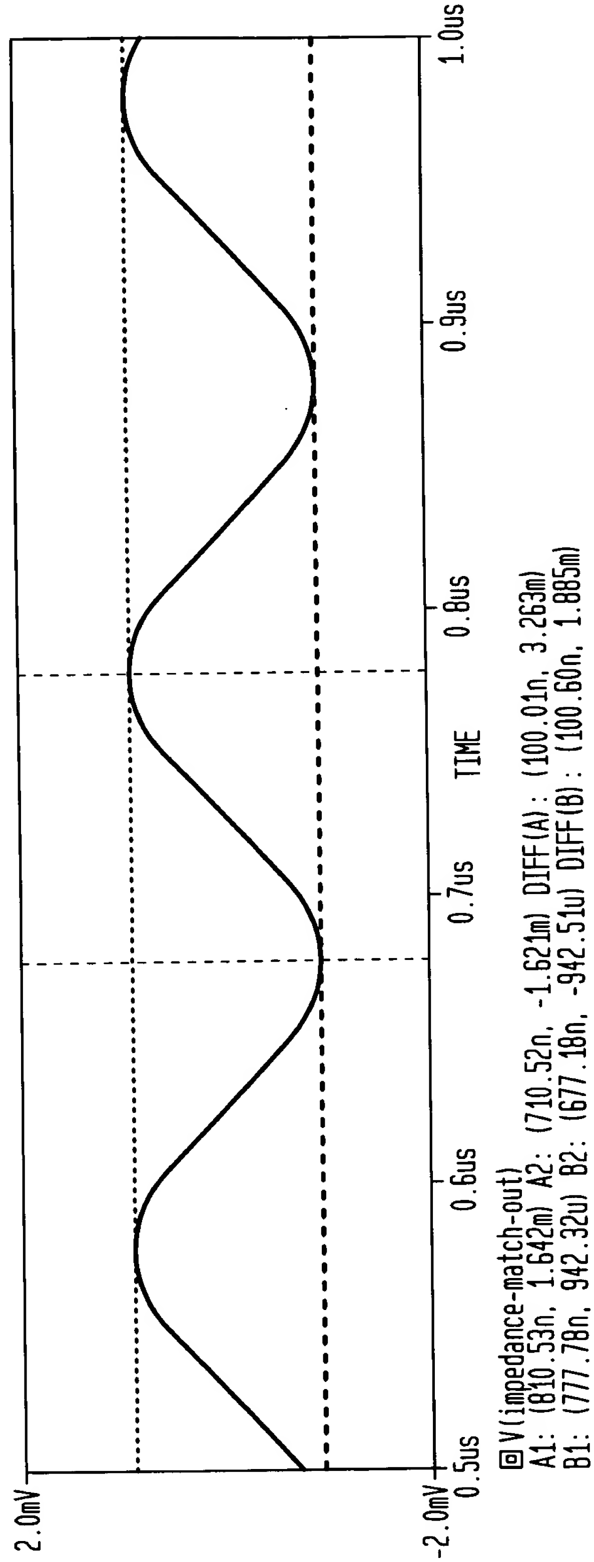

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FIG. 109A

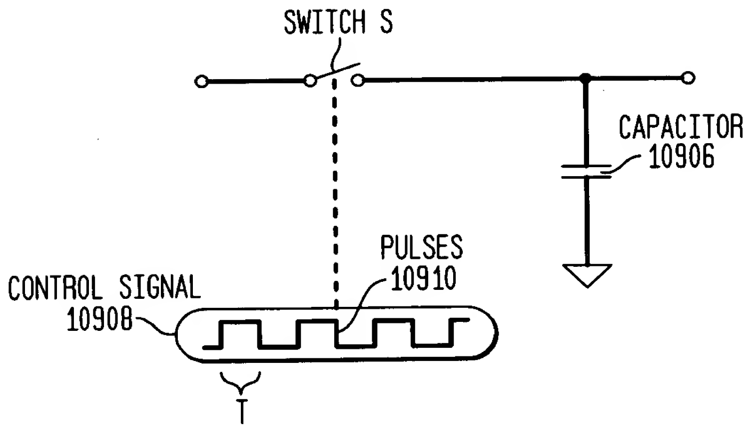


FIG. 109B

$q = C \cdot V$	EQ. 10
$V = A \cdot \sin(t)$	EQ. 11
$q(t) = C \cdot A \cdot \sin(t)$	EQ. 12
$\Delta q(t) = C \cdot A \cdot \sin(t) - C \cdot A \cdot \sin(t-T)$	EQ. 13
$\Delta q(t) = C \cdot A \cdot (\sin(t) - \sin(t-T))$	EQ. 14
$\sin(\alpha) - \sin(\beta) = 2 \cdot \sin(\frac{\alpha - \beta}{2}) \cdot \cos(\frac{\alpha + \beta}{2})$	EQ. 15
$\Delta q(t) = 2 \cdot C \cdot A \cdot \sin[\frac{t-(t-T)}{2}] \cdot \cos[\frac{t+(t-T)}{2}]$	EQ. 16
$\Delta q(t) = 2 \cdot C \cdot A \cdot \sin(\frac{1}{2} \cdot T) \cdot \cos(t - \frac{1}{2} \cdot T)$	EQ. 17
$q(t) = \int C \cdot A \cdot (\sin(t) - \sin(t-T)) dt$	EQ. 18
$q(t) = -\cos(t) \cdot C \cdot A + \cos(t-T) \cdot C \cdot A$	EQ. 19
$q(t) = C \cdot A \cdot (\cos(t-T) - \cos(t))$	EQ. 20

FIG. 109C

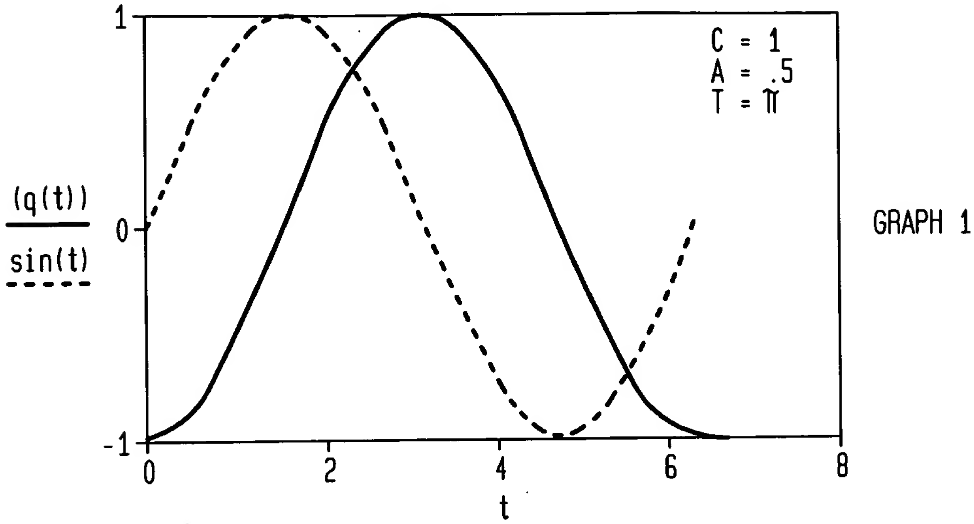


FIG. 109D

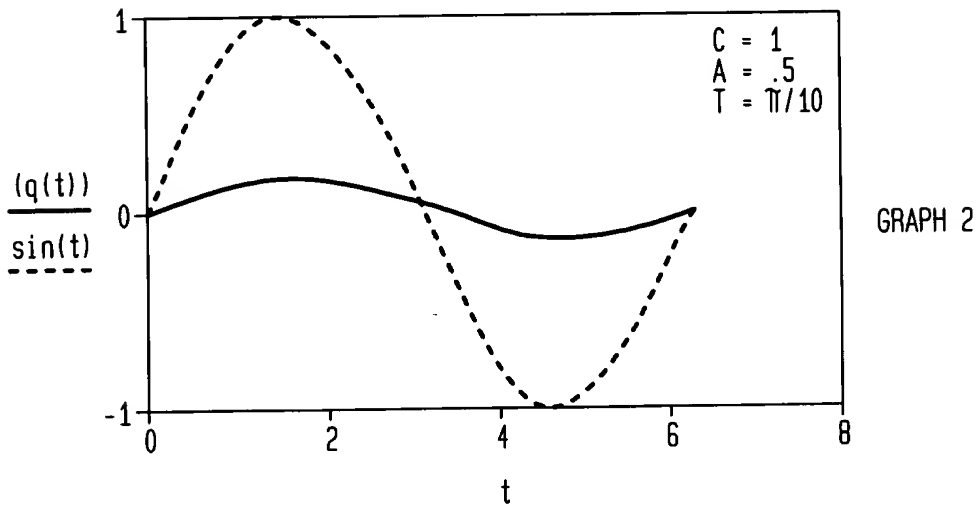


FIG. 109E

POWER-CHARGE RELATIONSHIP

$q=C\cdot V$	EQ. 21
$V=q/C$	EQ. 22
$V=J/C$	EQ. 23
$J=q^2/C$	EQ. 24
$P=J/S$	EQ. 25
$P=\frac{q^2}{C\cdot S}$	EQ. 26

FIG. 109F

INSERTION LOSS

INSERTION LOSS IN dB IS EXPRESSED BY:

$$IL_{dB}=10\cdot\log\left(\frac{P_{in}}{P_{out}}\right) \text{ or}$$

$$IL_{dB}=10\cdot\log\left[\frac{\left(\frac{V_{in}^2}{R_{in}}\right)}{\left(\frac{V_{out}^2}{R_{out}}\right)}\right]$$

FIG. 110A

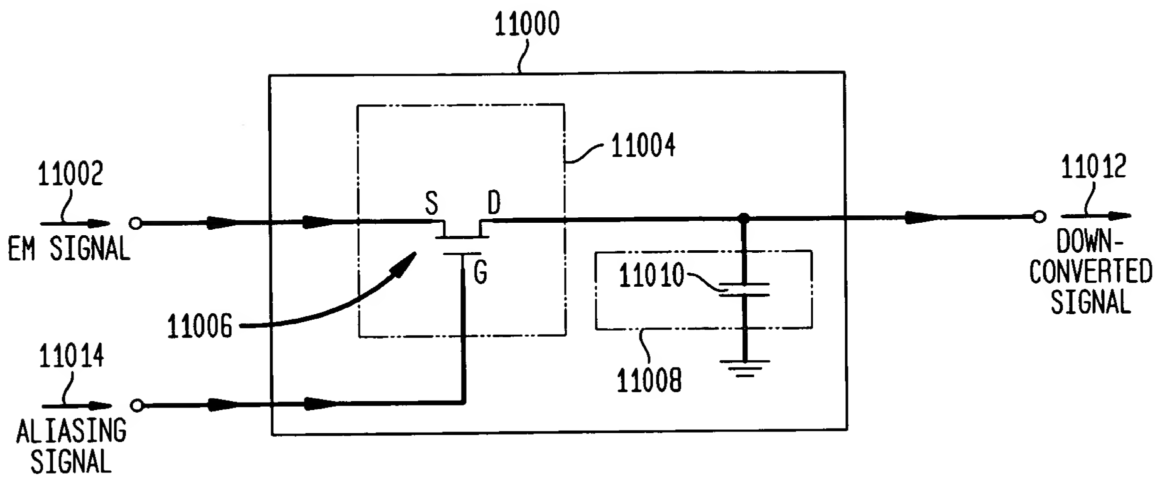
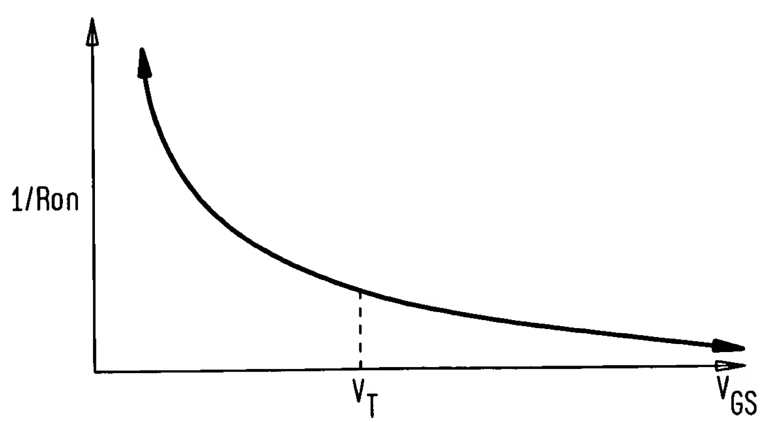


FIG. 110B



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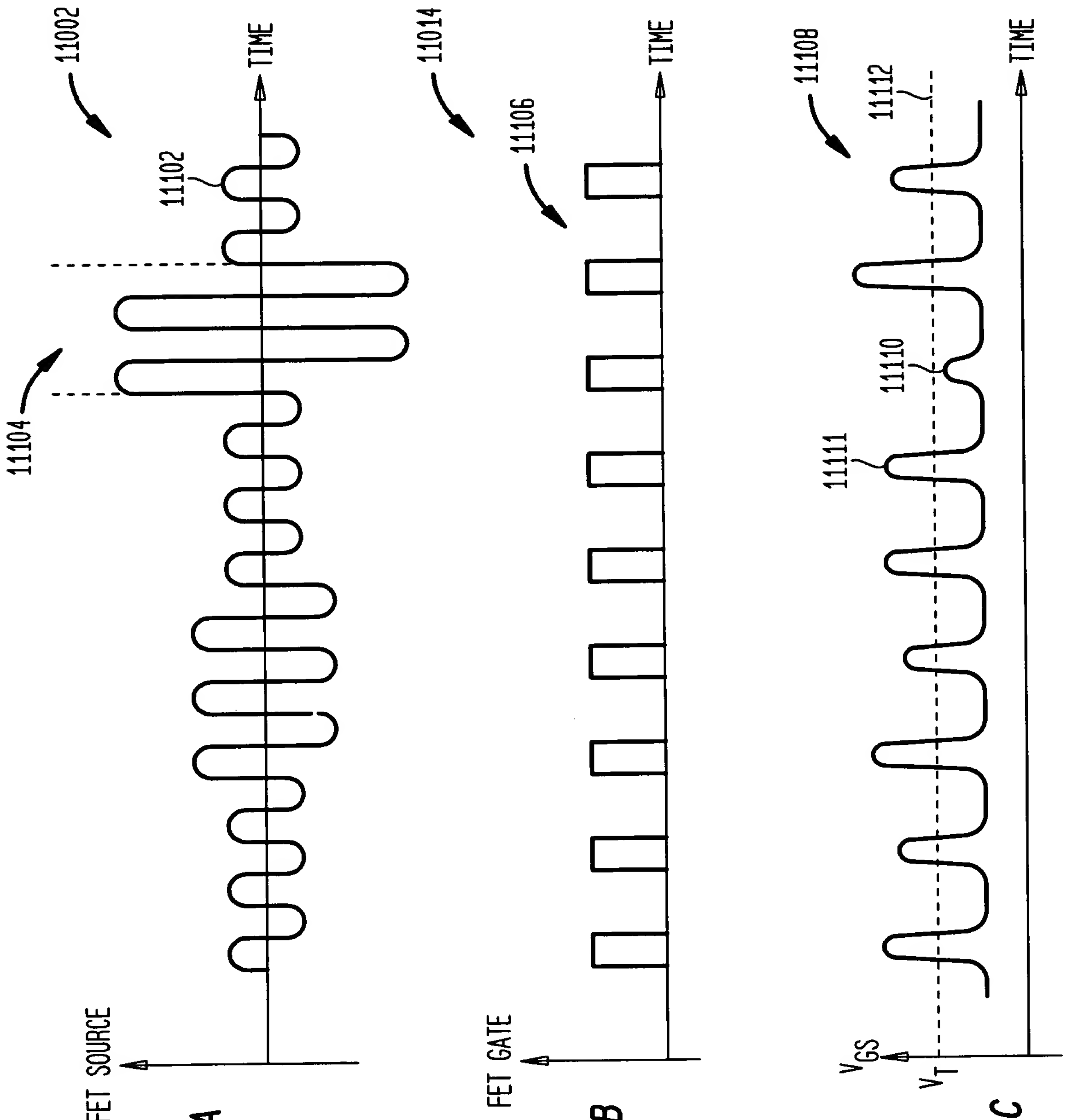

FIG. 111A

FIG. 111B

FIG. 111C

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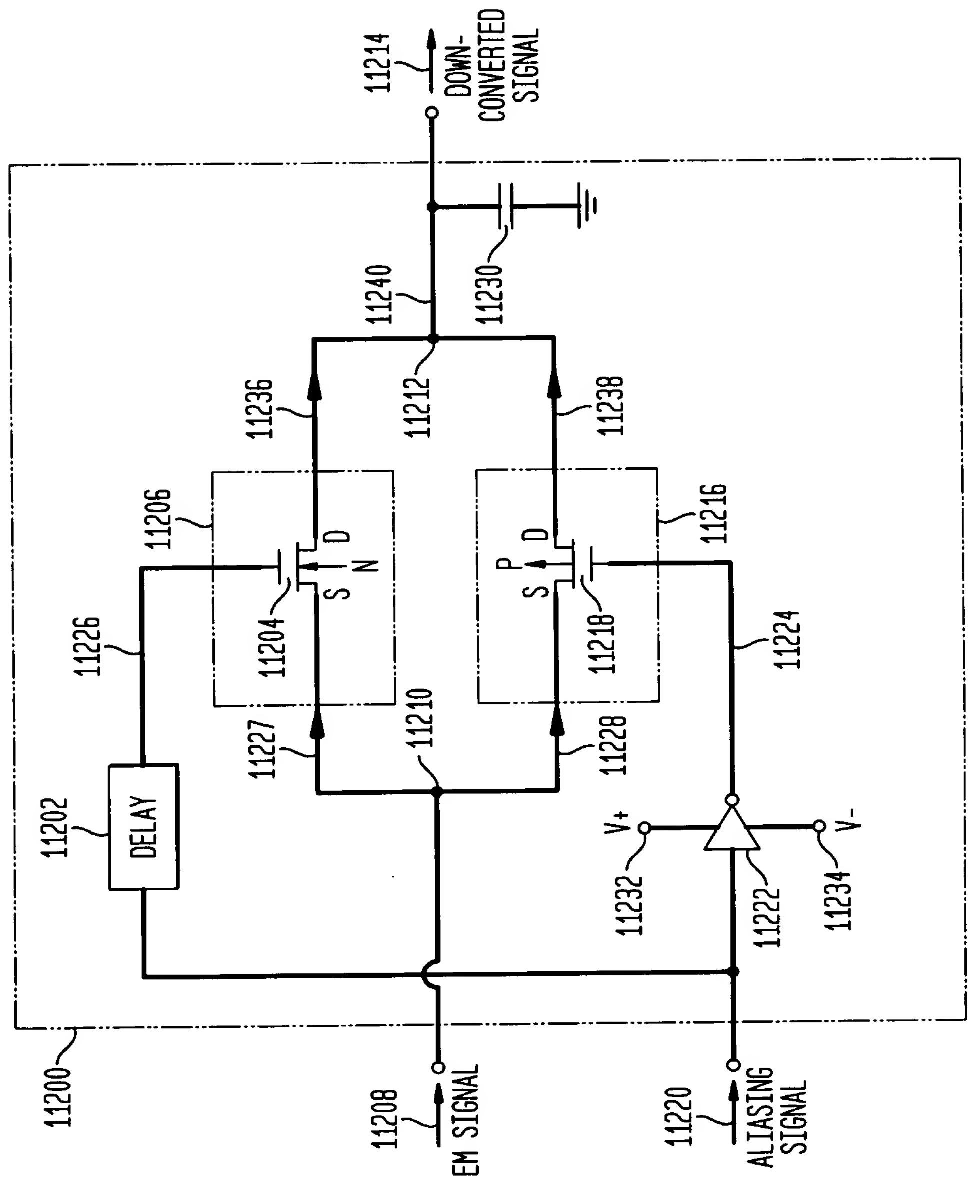
FIG. 112



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Inventors: SORRELLS et al.
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FIG. 113A

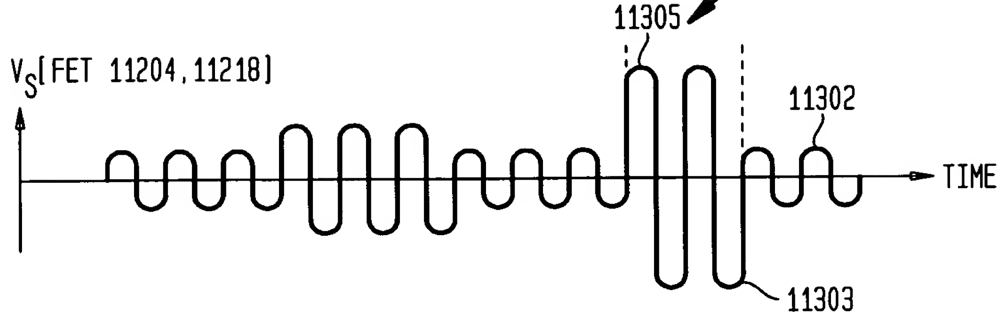


FIG. 113B

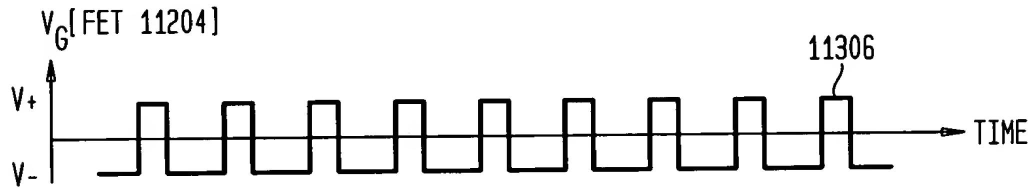


FIG. 113C

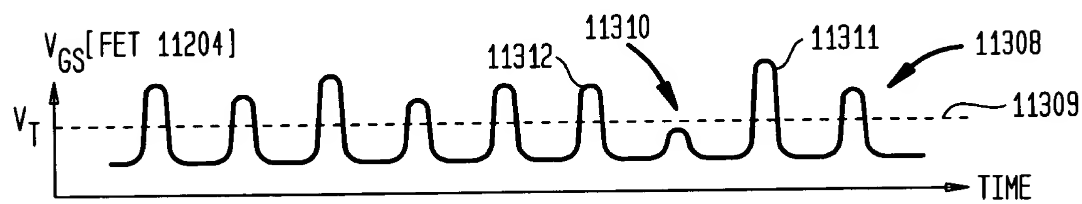


FIG. 113D

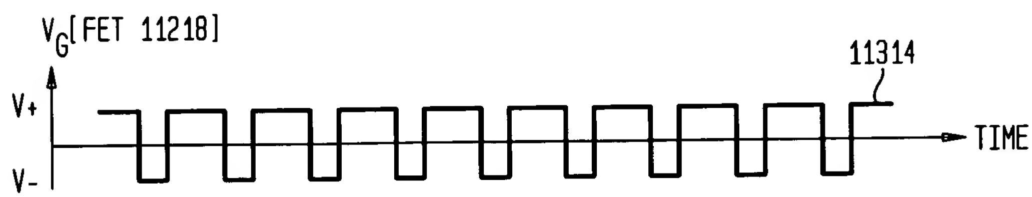
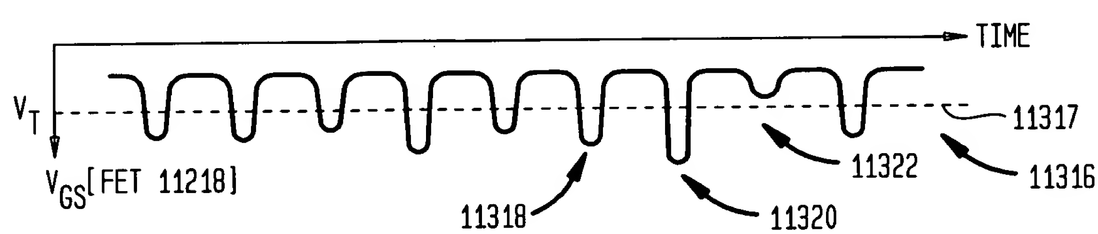


FIG. 113E



Appl. No. 09/550,642; Filed: Apr 14, 2000
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Inventors: SORRELLS et al.
Tel. No.: 202-371-2600
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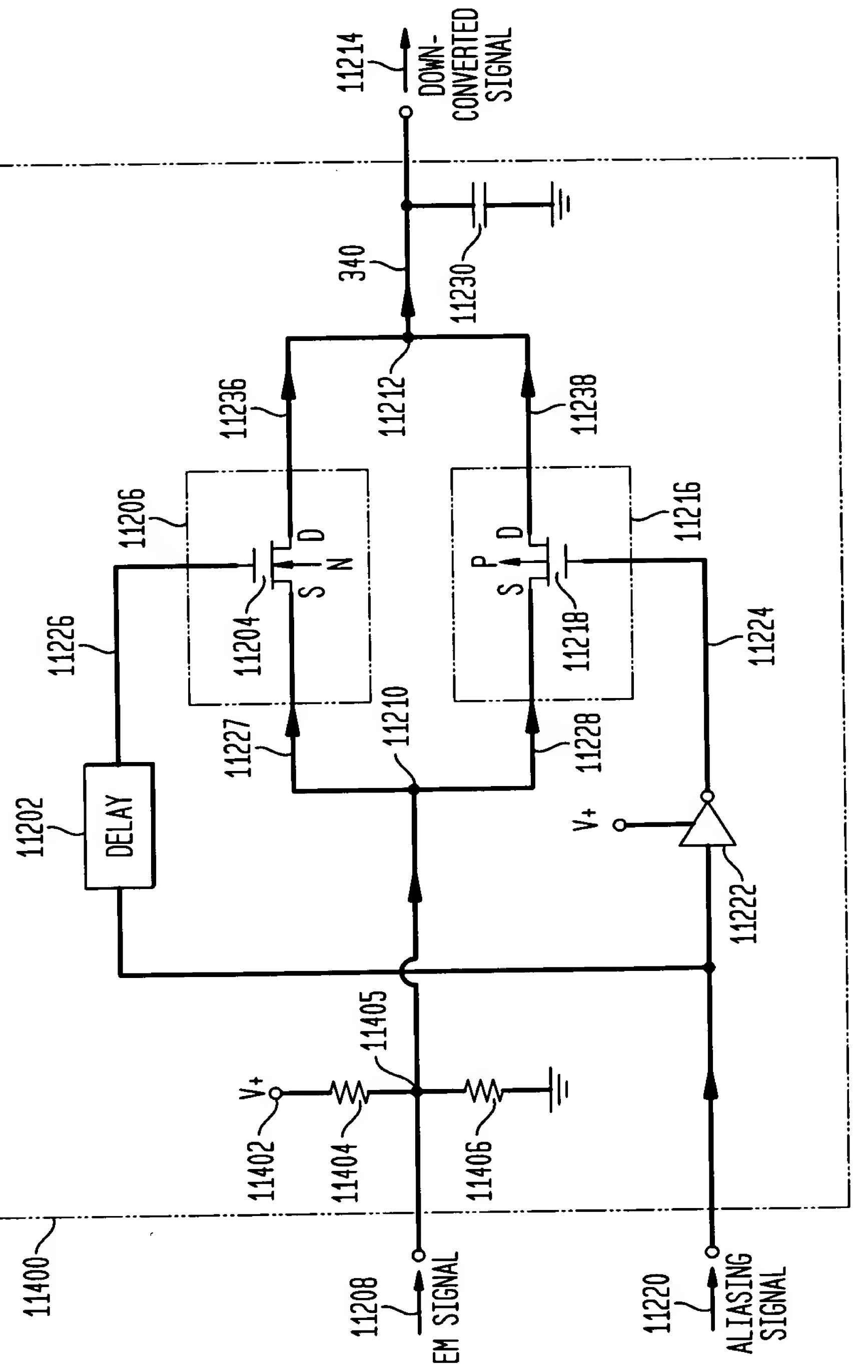
FIG. 114



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Inventors: SORRELLS et al.
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FIG. 115

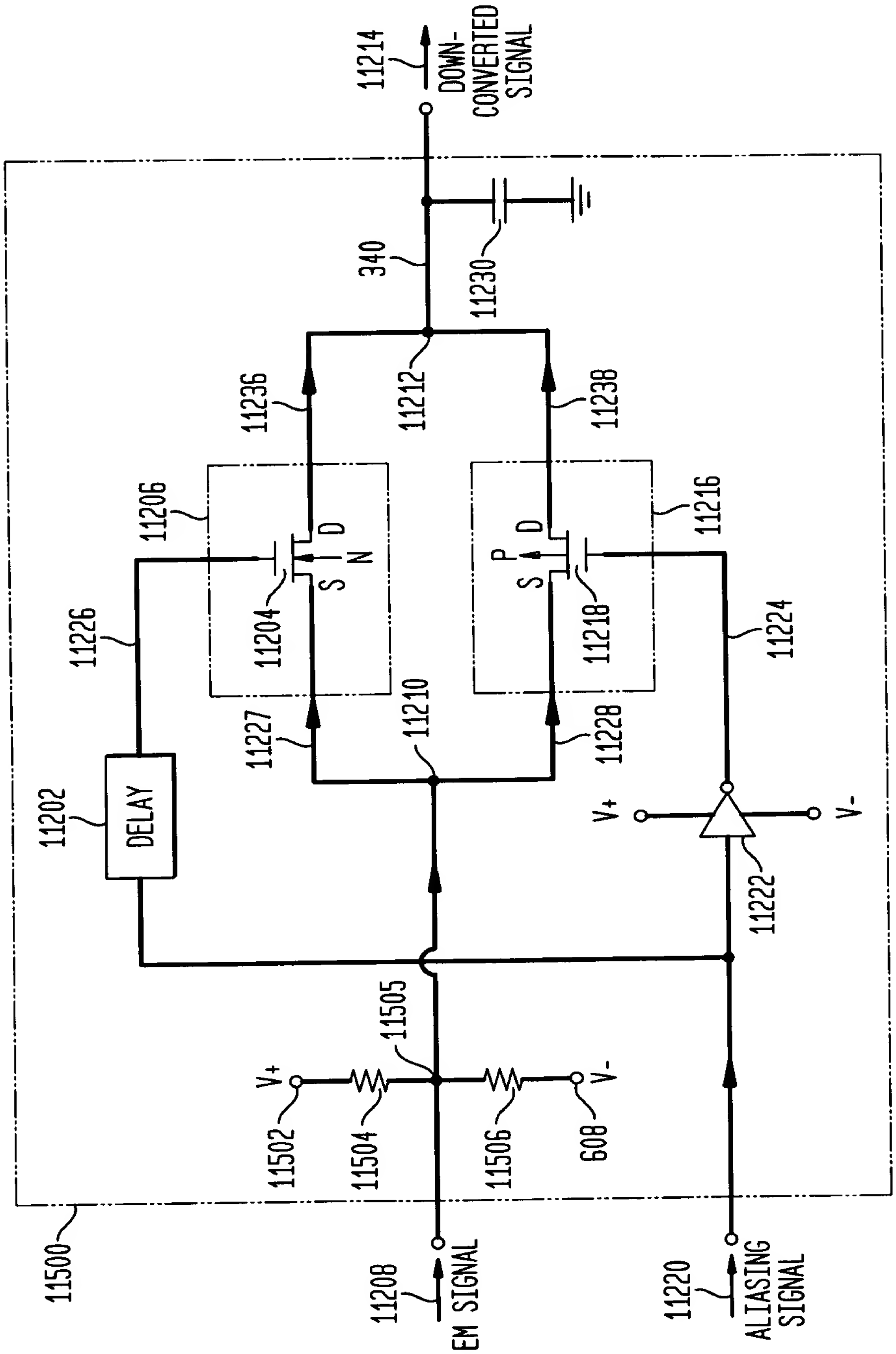


FIG. 116

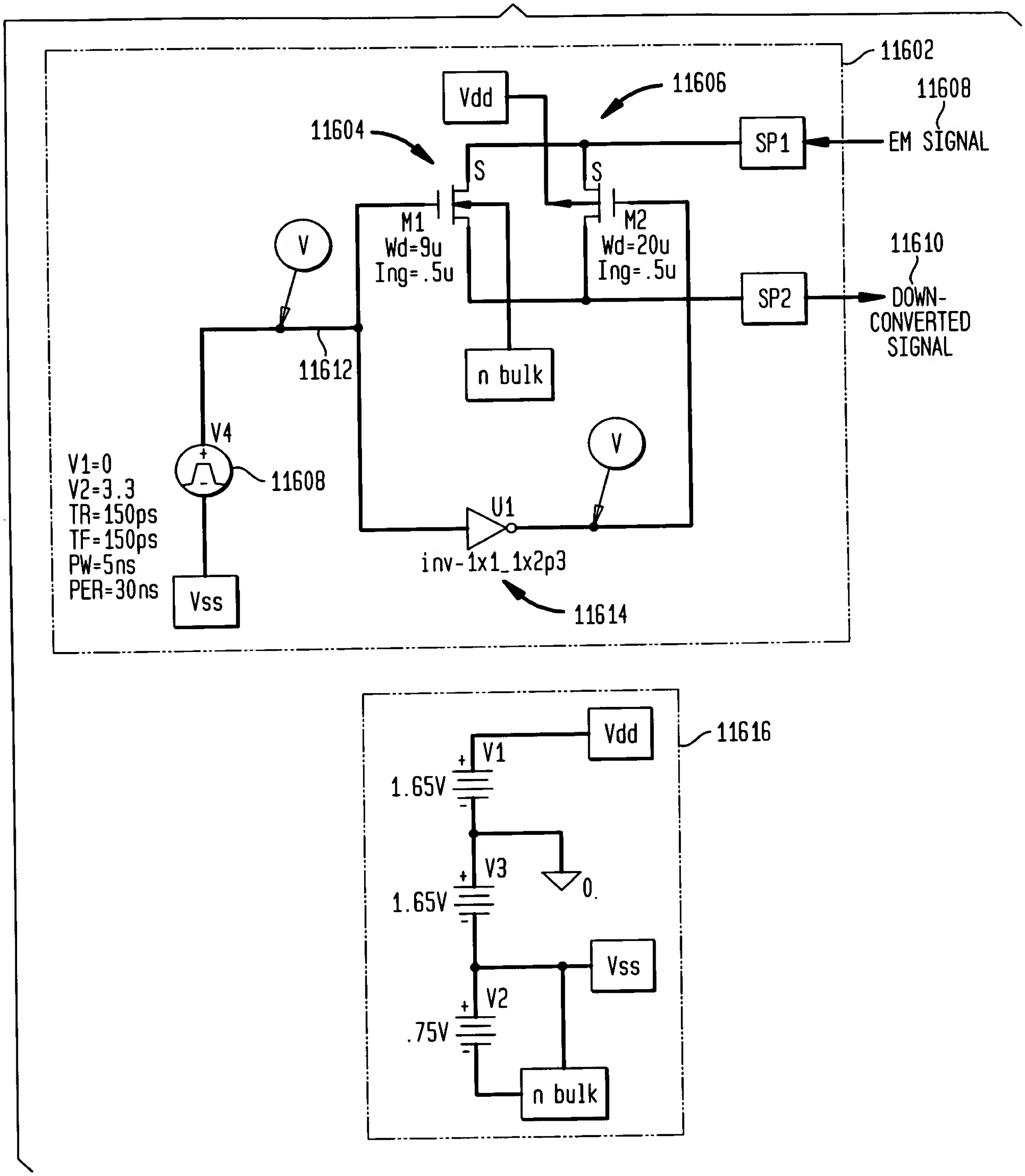
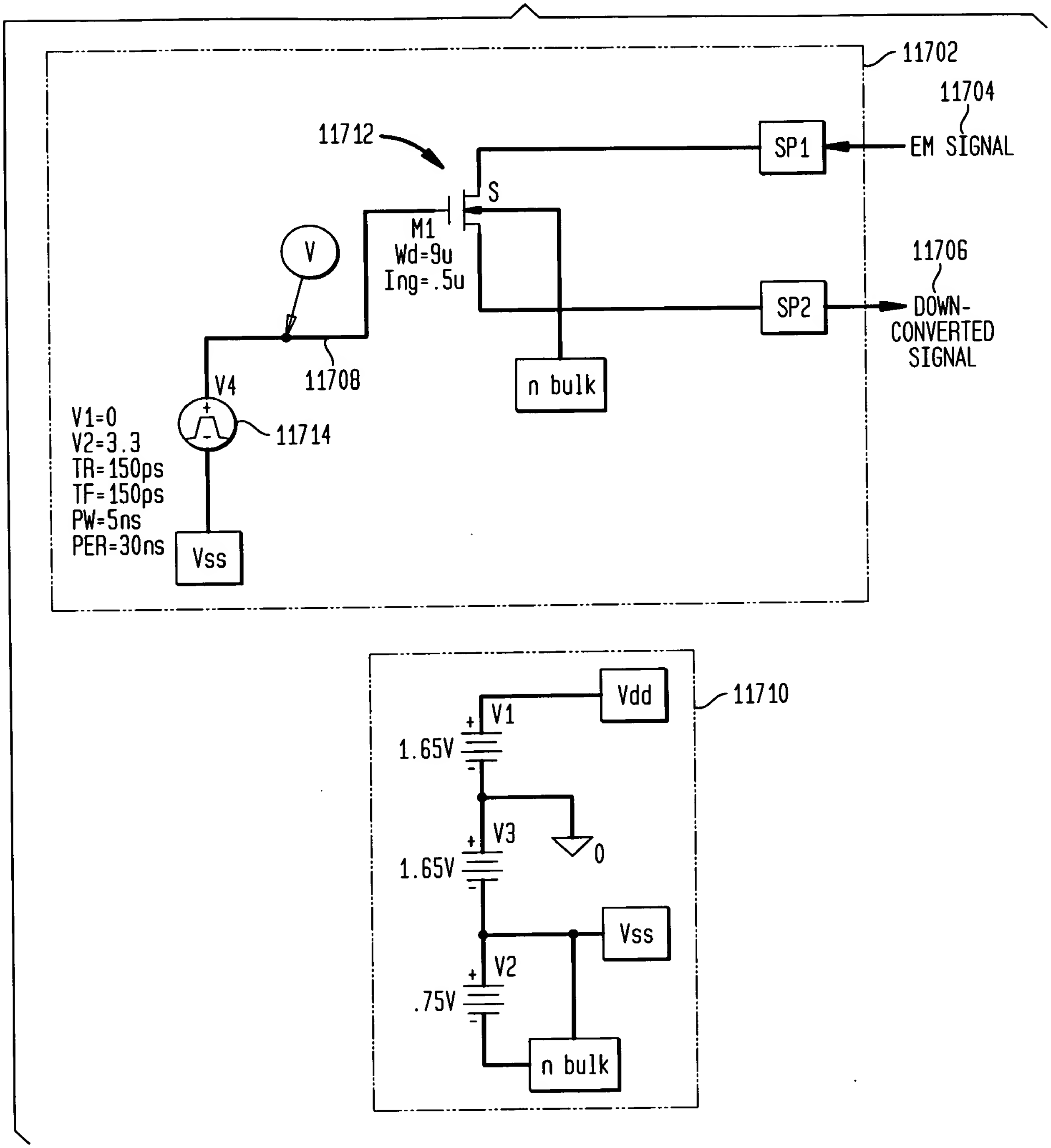

11602
11606
11604
Vdd
SP1
11608
EM SIGNAL
S
S
M1
Wd=9u
Lng=.5u
M2
Wd=20u
Lng=.5u
V
SP2
11610
DOWN-CONVERTED SIGNAL
11612
n bulk
V4
V
V1=0
V2=3.3
TR=150ps
TF=150ps
PW=5ns
PER=30ns
11608
U1
inv-1x1_1x2p3
Vss
11614
Vdd
11616
V1
1.65V
V3
1.65V
0
Vss
V2
.75V
n bulk

FIG. 117


11702
11704
EM SIGNAL
SP1
11712
S
M1
Wd=9u
Lng=.5u
V
SP2
11706
DOWN-
CONVERTED
SIGNAL
V4
11708
n bulk
V1=0
V2=3.3
TR=150ps
TF=150ps
PW=5ns
PER=30ns
11714
Vss
Vdd
11710
V1
1.65V
V3
1.65V
0
Vss
V2
.75V
n bulk

Replacement Sheet
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Inventors: SORRELLS et al.
Tel. No.: 202-371-2600
For: Method and System for Down-Converting an Electromagnetic Signal, and Transforms for Same

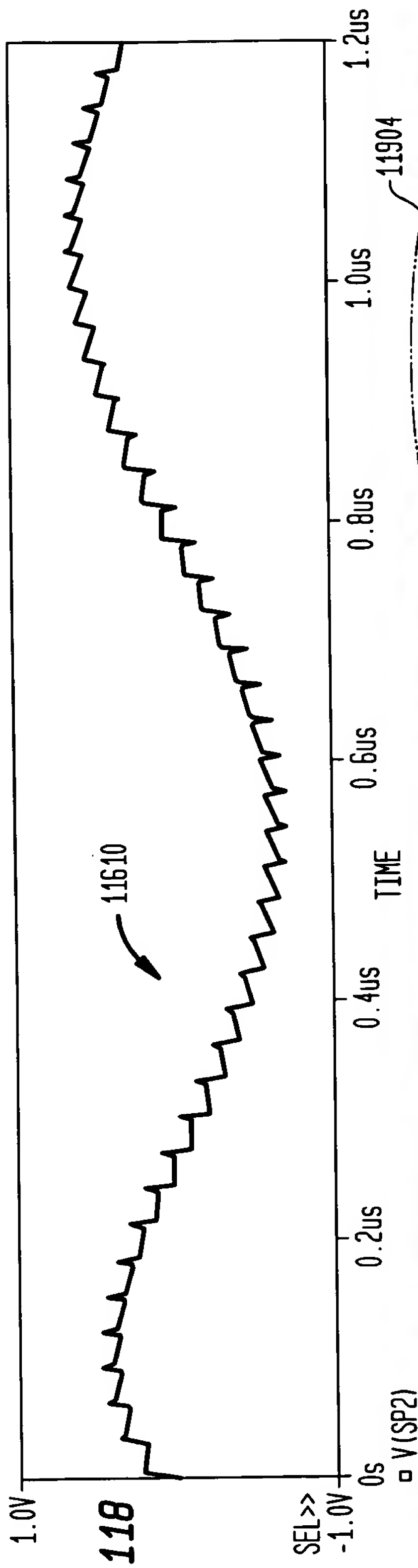

FIG. 118

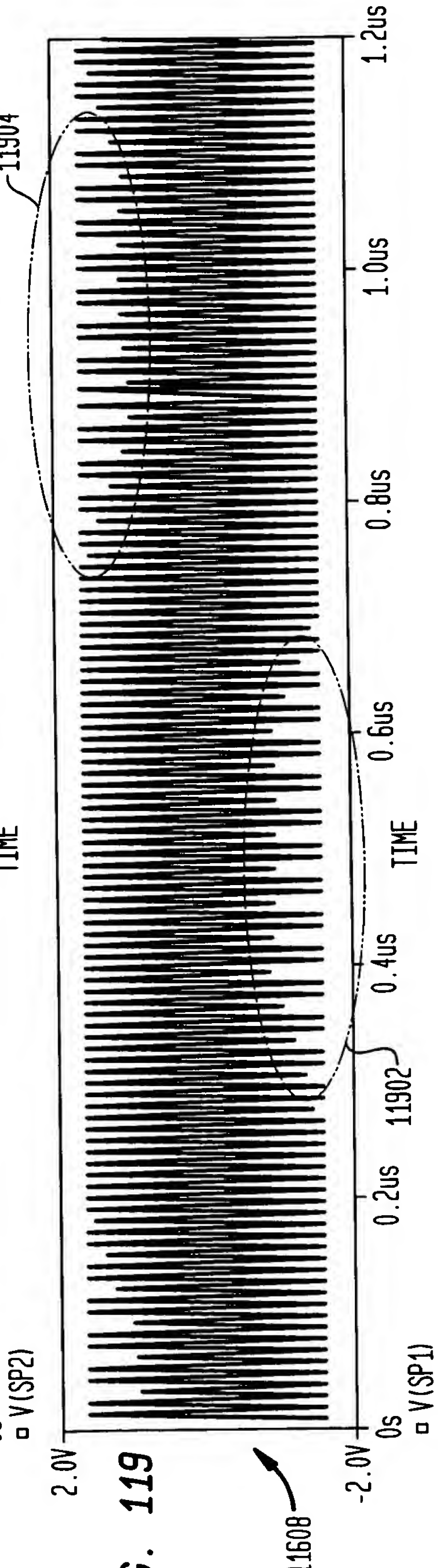

FIG. 119

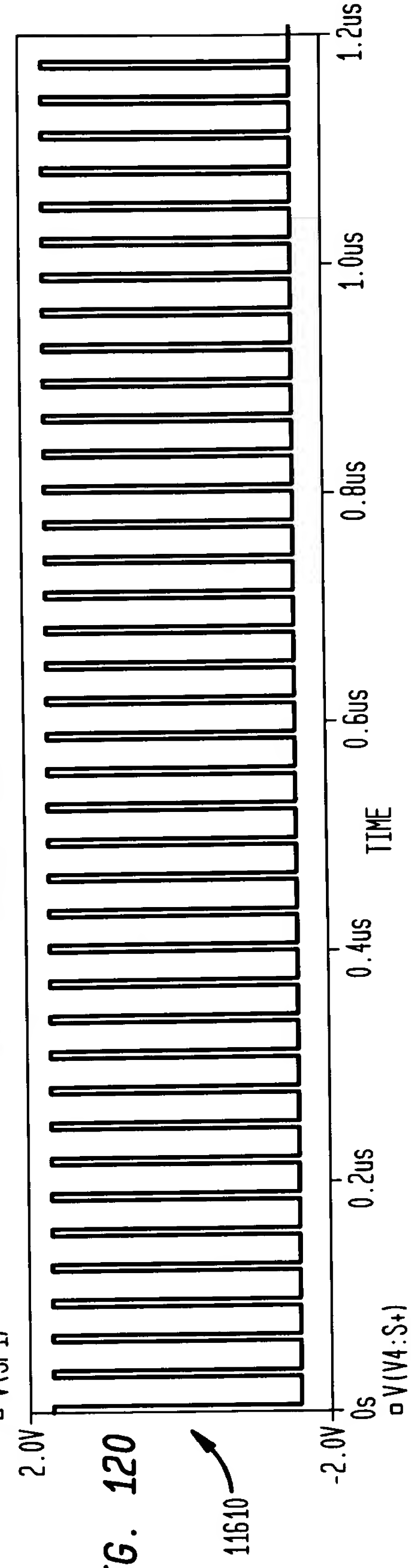

FIG. 120

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Inventors: SORRELLS et al.
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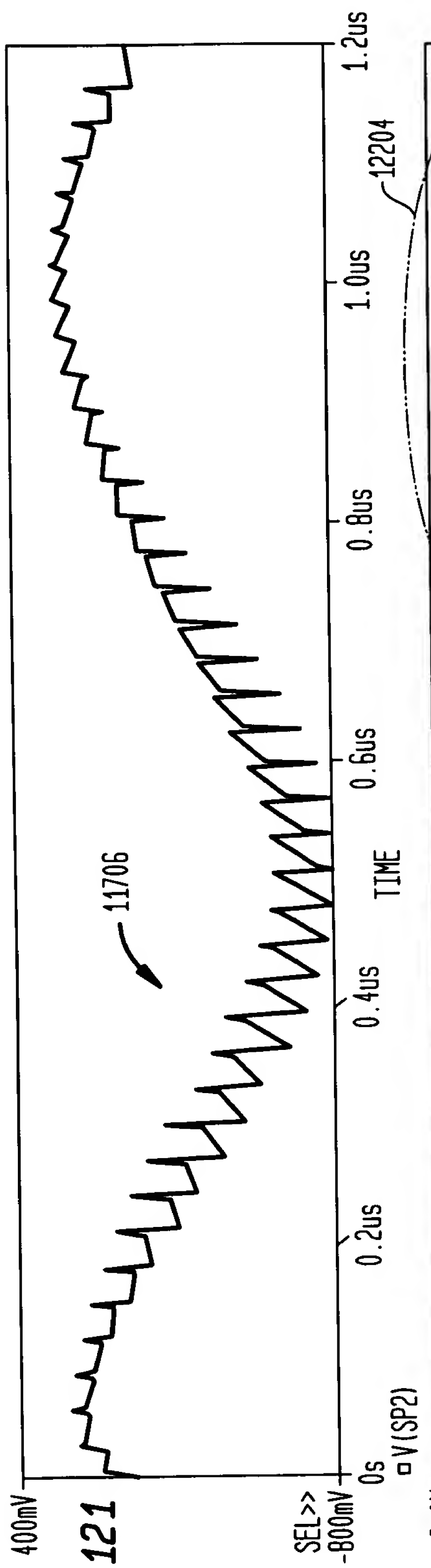

FIG. 121

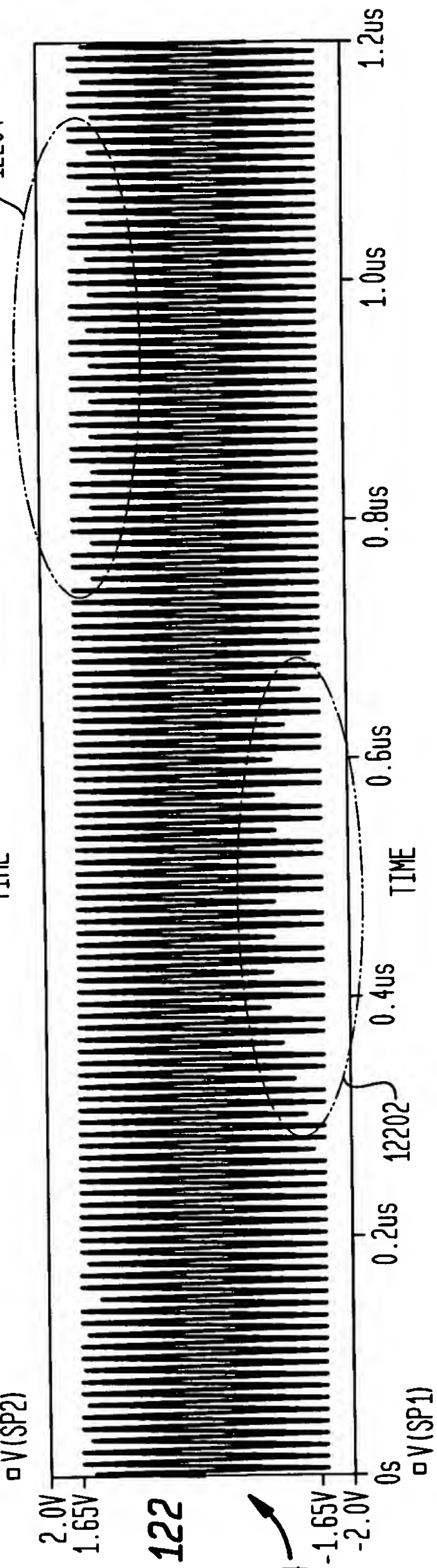

FIG. 122

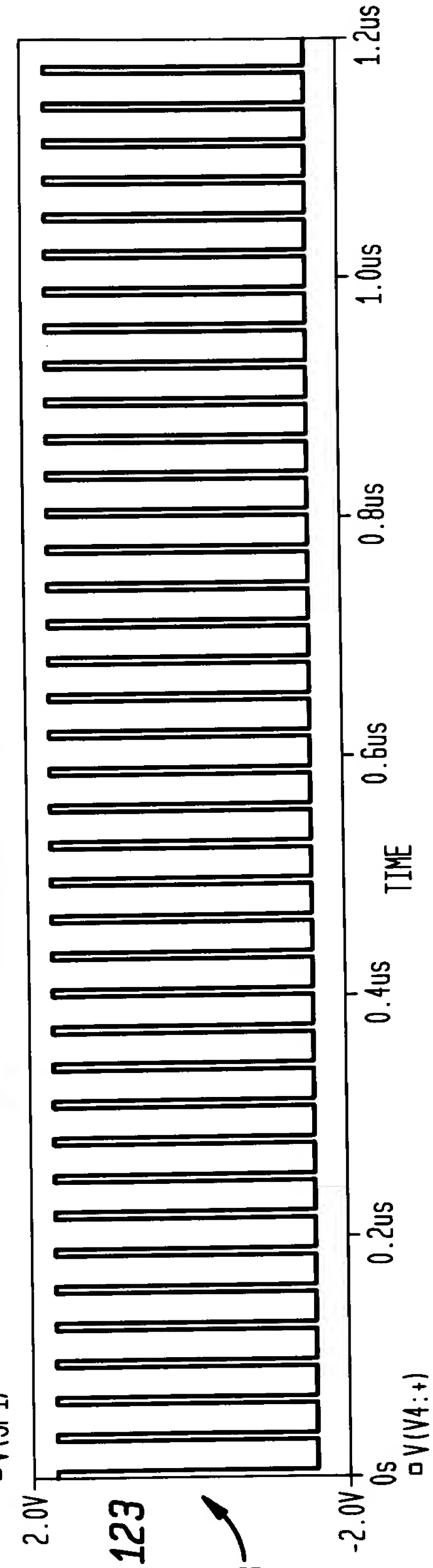

FIG. 123

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Inventors: SORRELLS et al.
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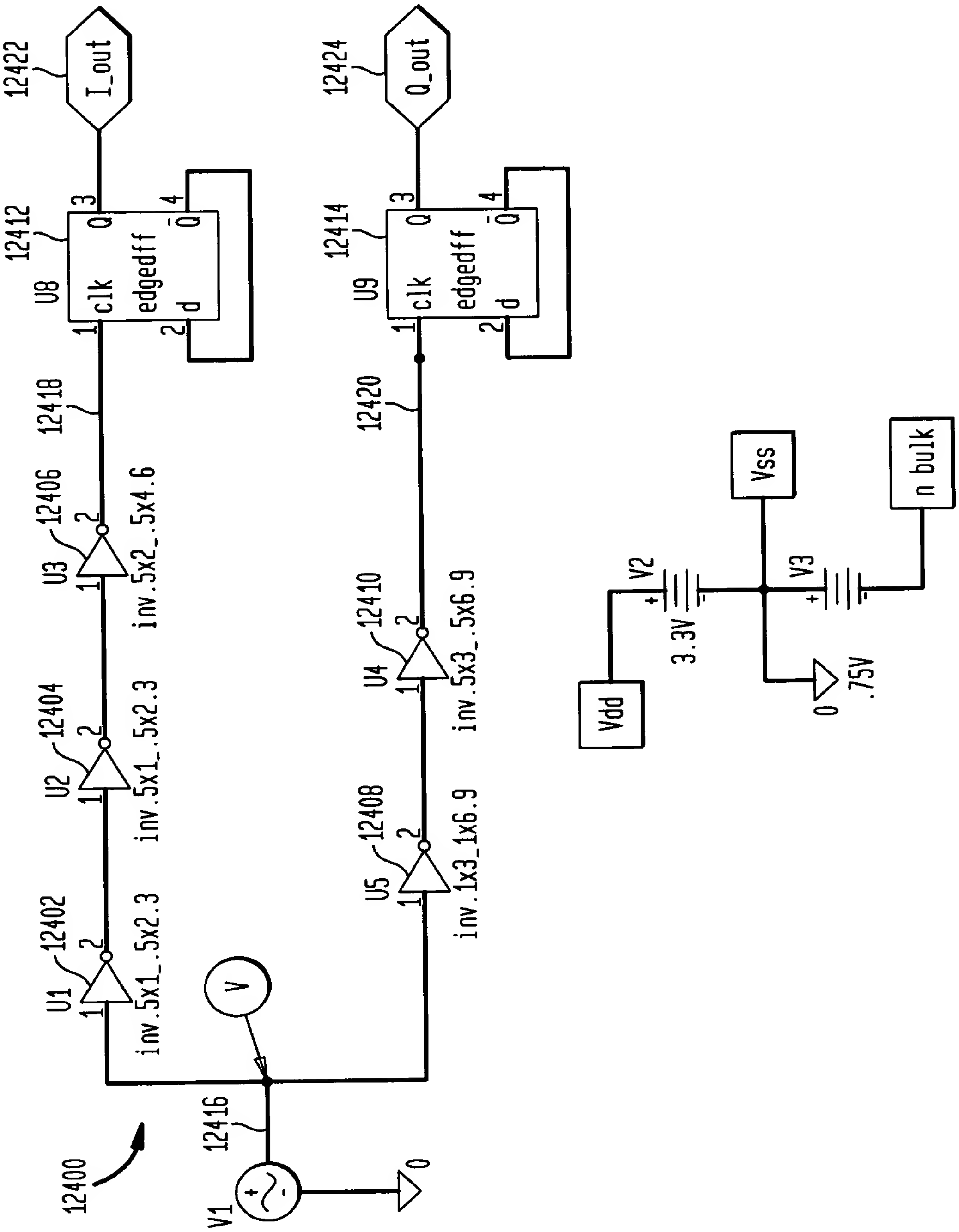
FIG. 124A



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Inventors: SORRELLS et al.
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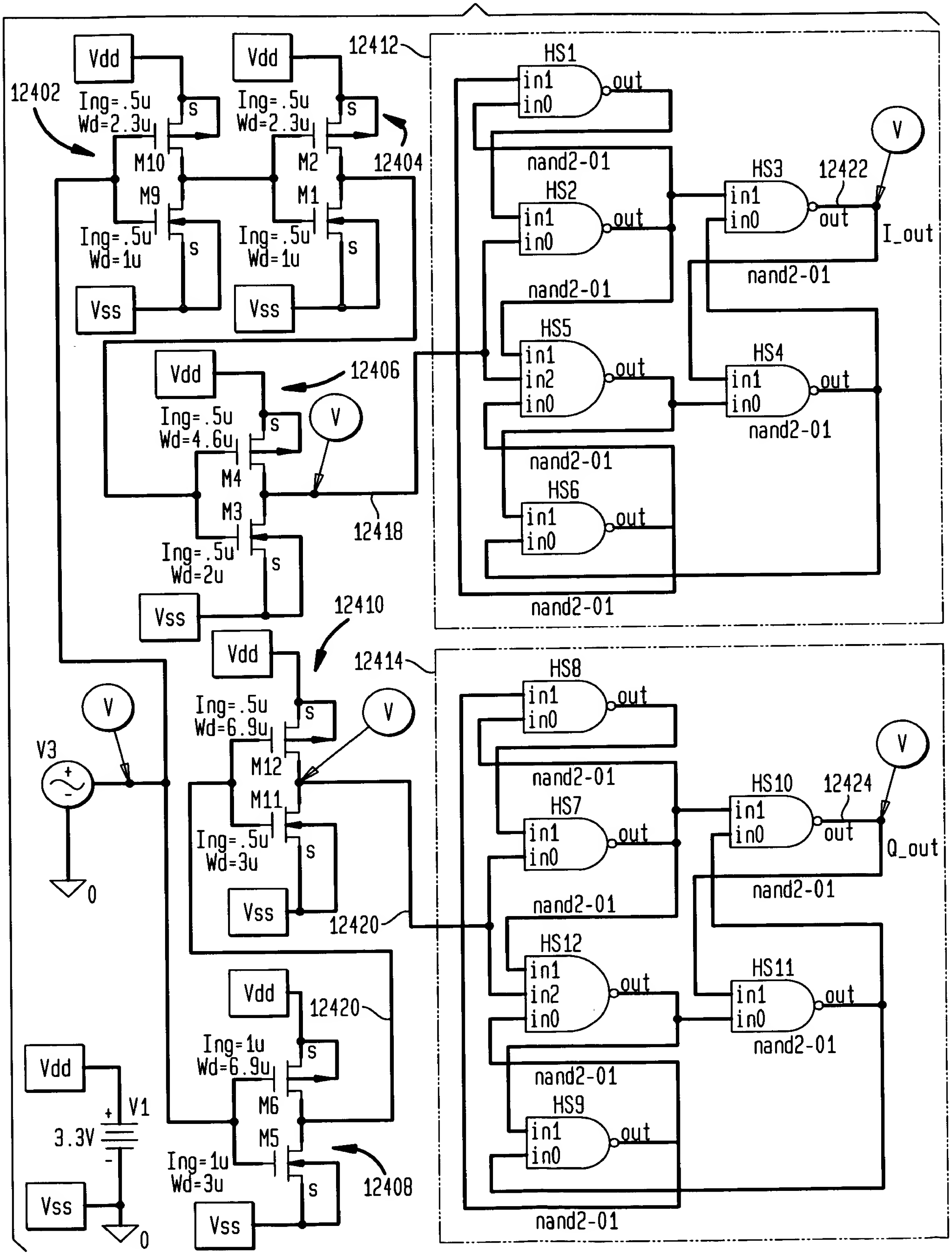
FIG. 124B



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Inventors: SORRELLS et al.
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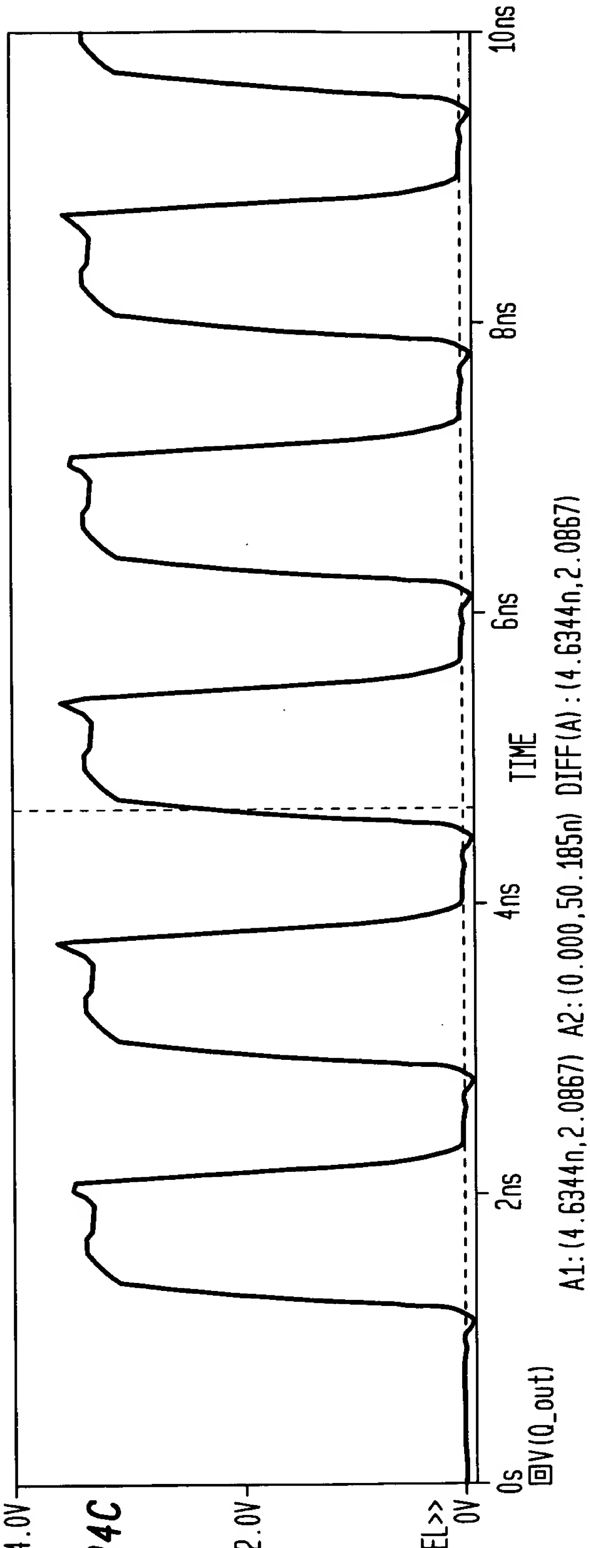

FIG. 124C

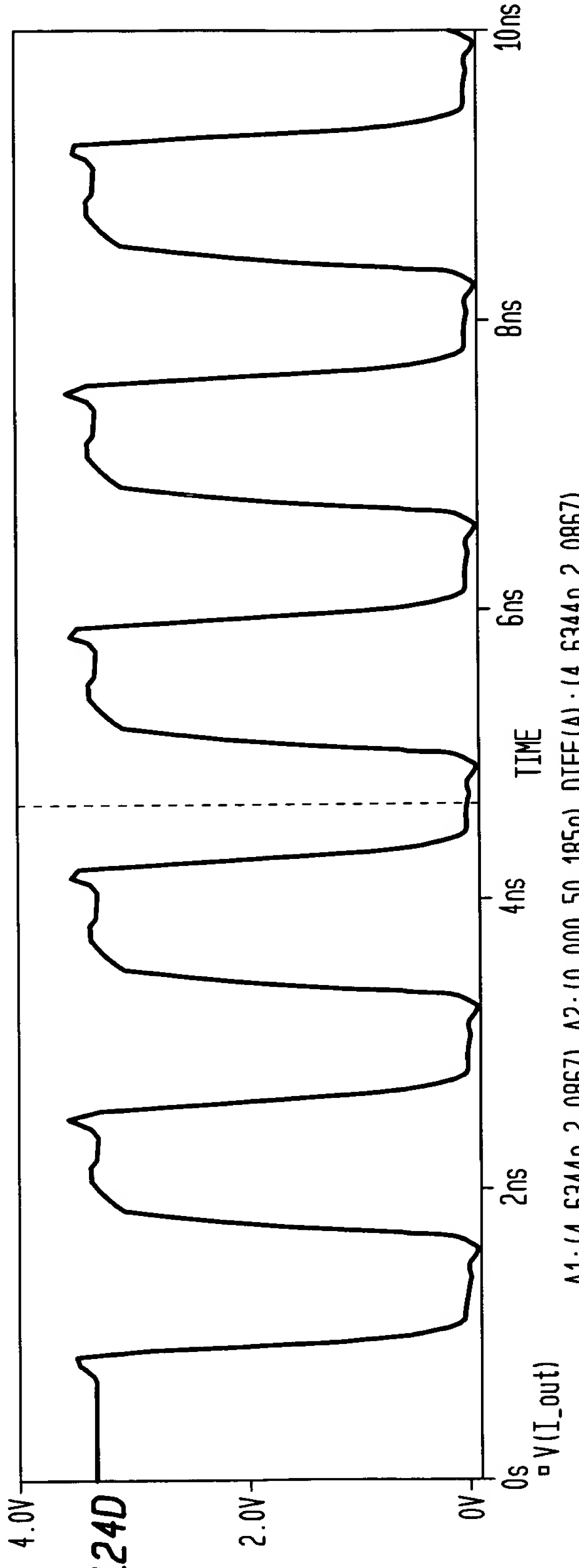

FIG. 124D

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Inventors: SORRELLS et al.
Tel. No.: 202-371-2600
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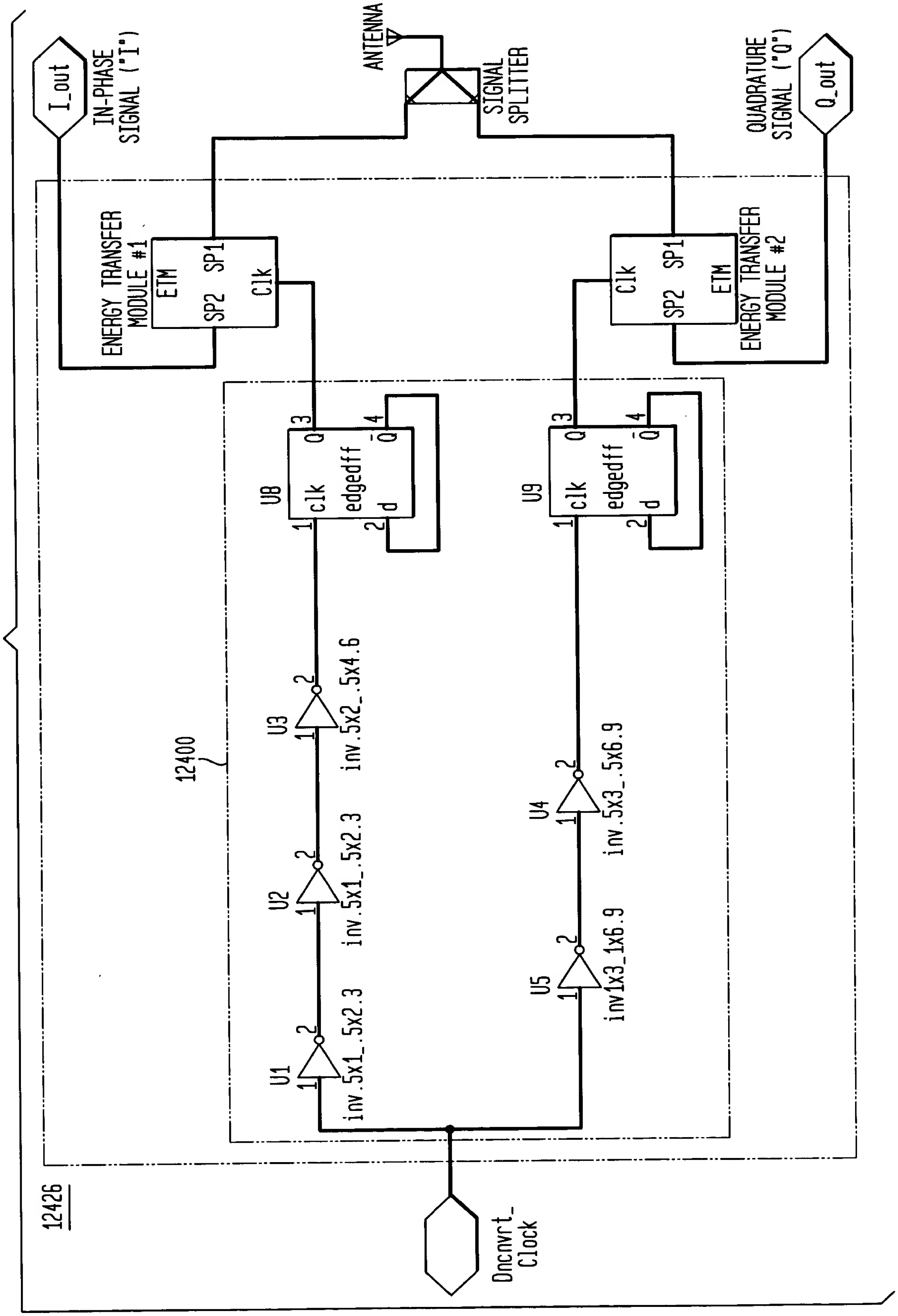

FIG. 124E

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Dkt No. 1744.0920001; Group Unit: 2634
Inventors: SORRELLS et al.
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FIG. 124F

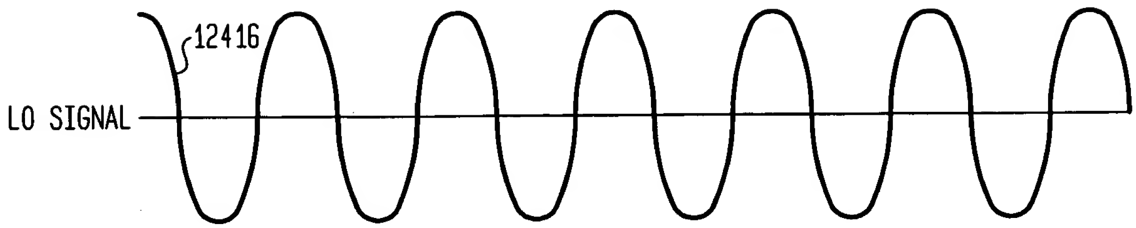

FIG. 124G

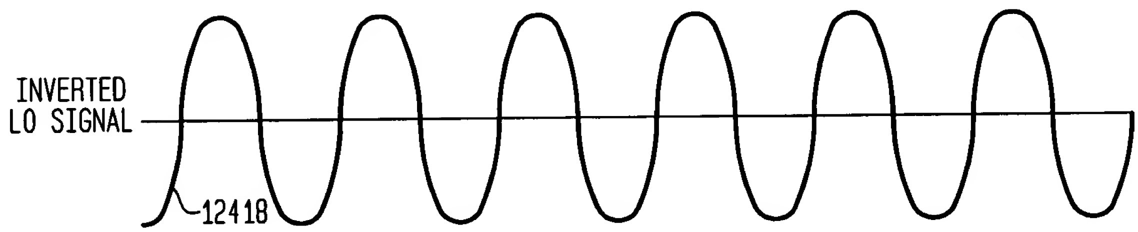

FIG. 124H

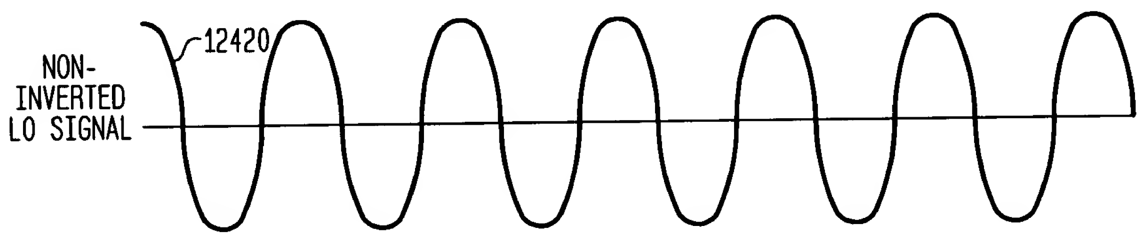

FIG. 124I

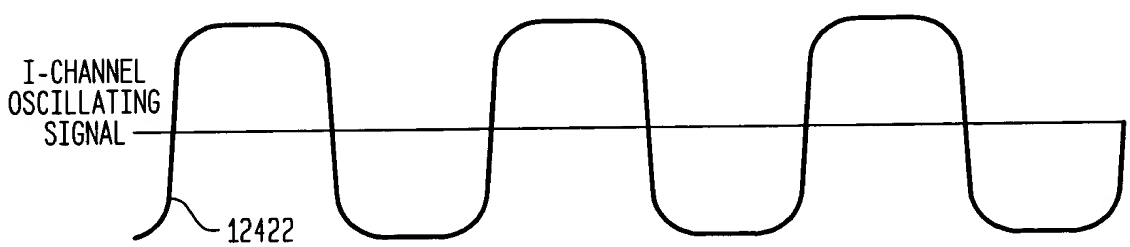

FIG. 124J

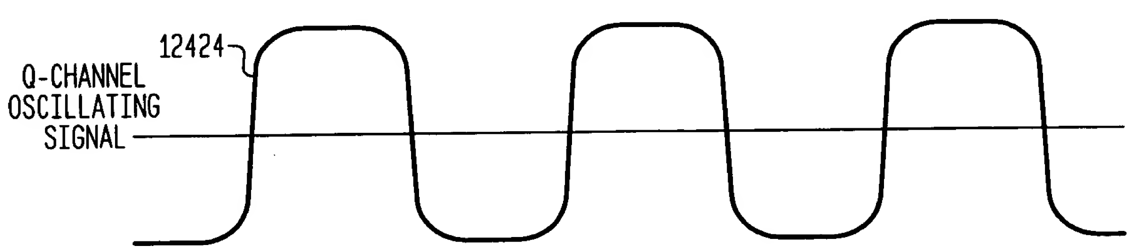

FIG. 125

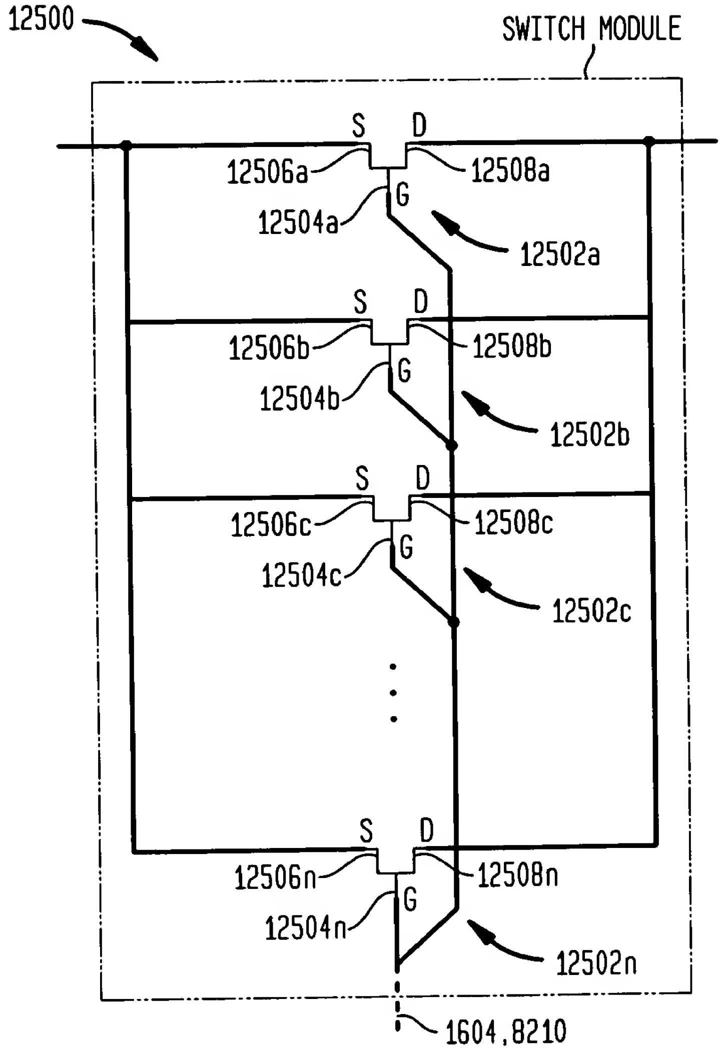
12500
SWITCH MODULE
S
D
12506a
12508a
G
12504a
12502a
S
D
12506b
12508b
G
12504b
12502b
S
D
12506c
12508c
G
12504c
12502c
S
D
12506n
12508n
G
12504n
12502n
1604,8210

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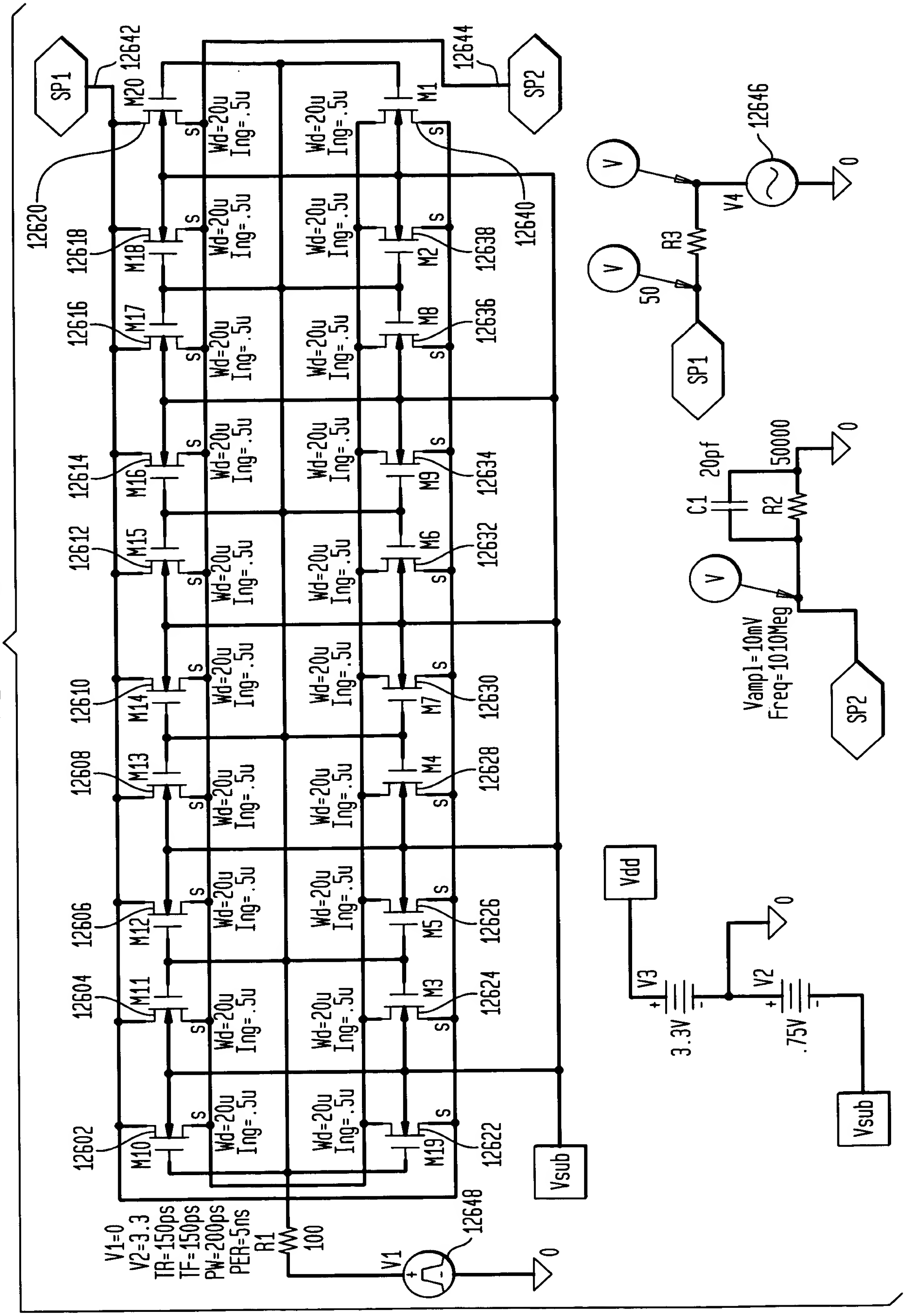
FIG. 126A



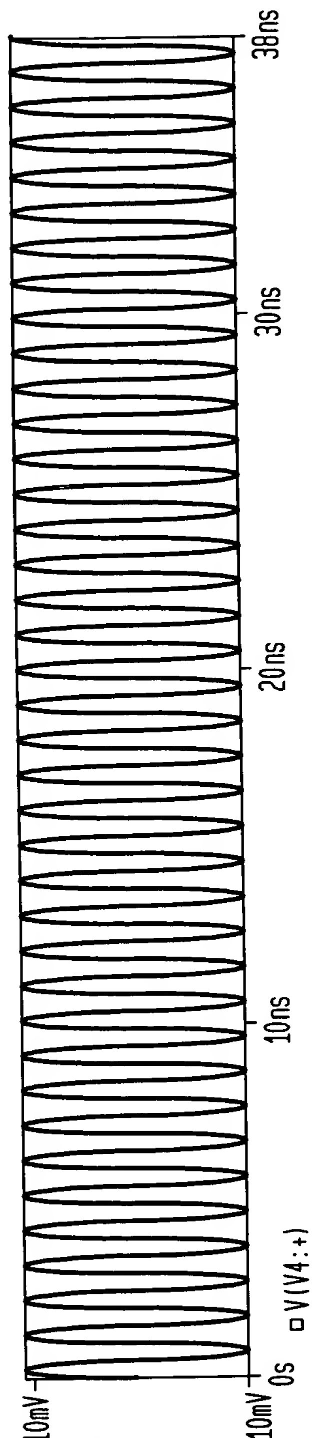


FIG. 126B

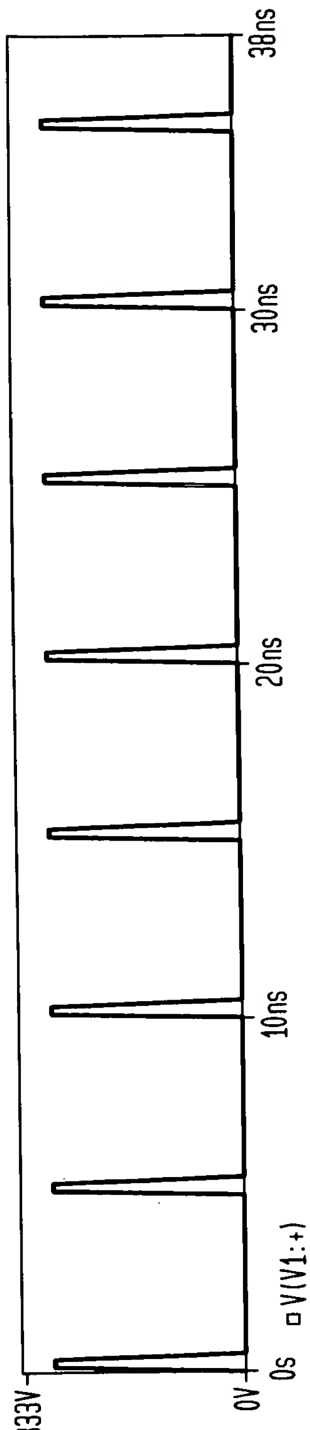


FIG. 126C

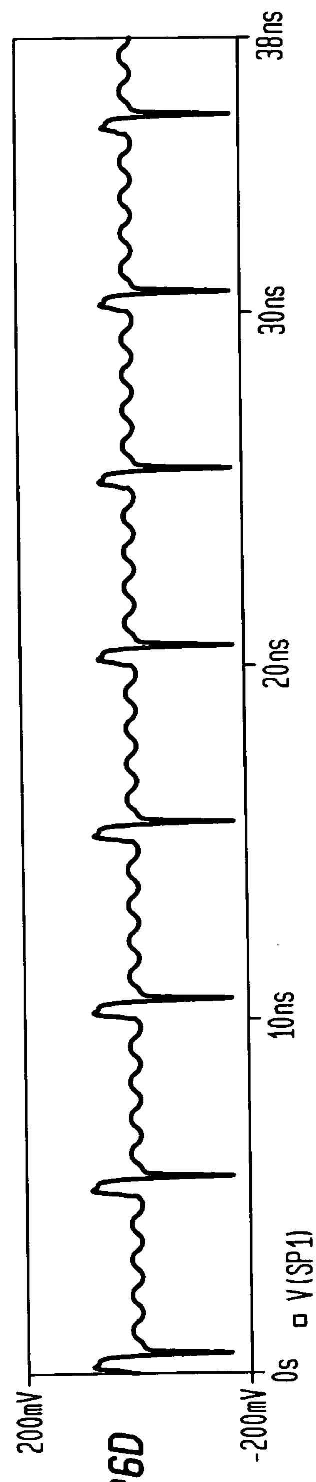


FIG. 126D

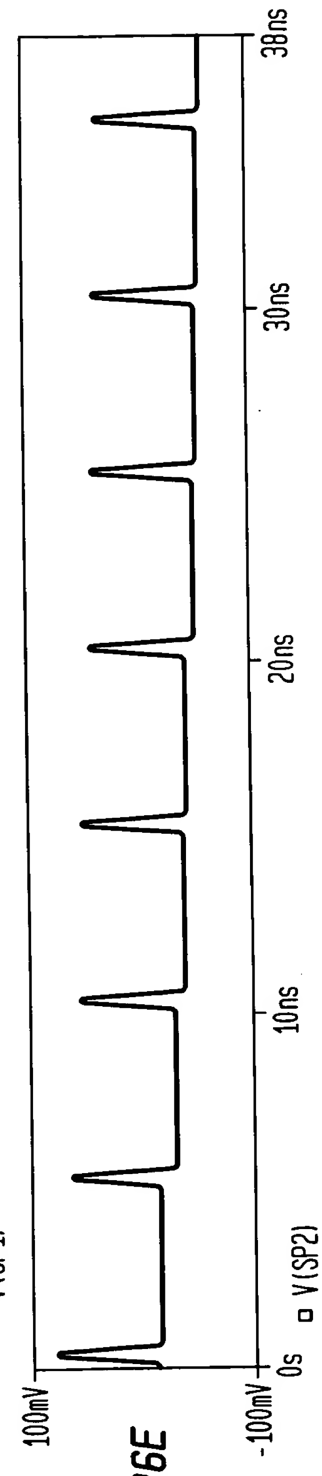


FIG. 126E

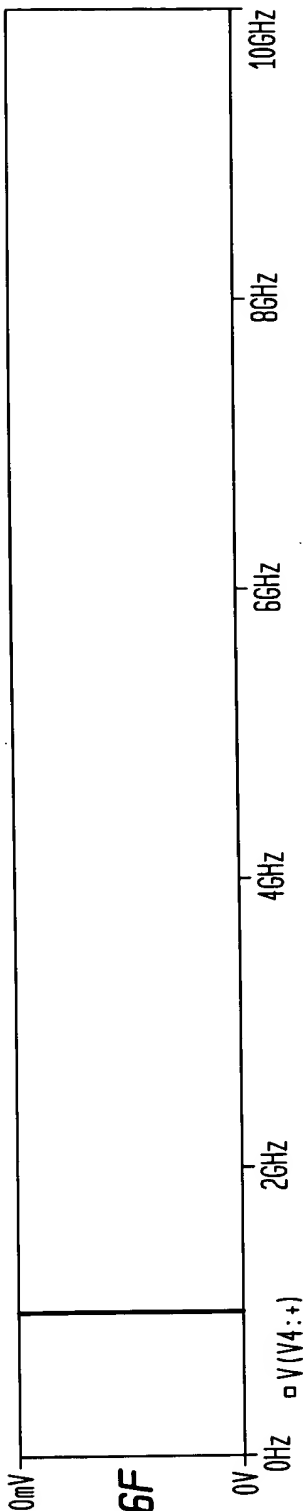


FIG. 126F

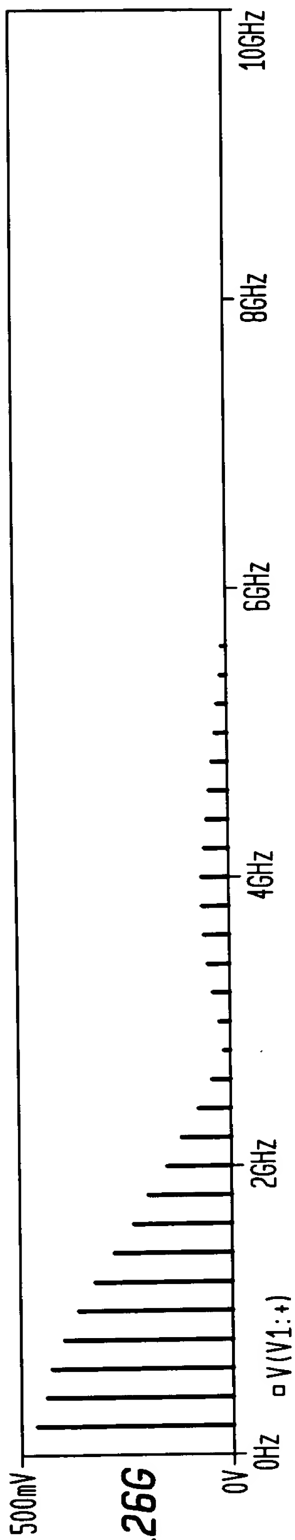


FIG. 126G

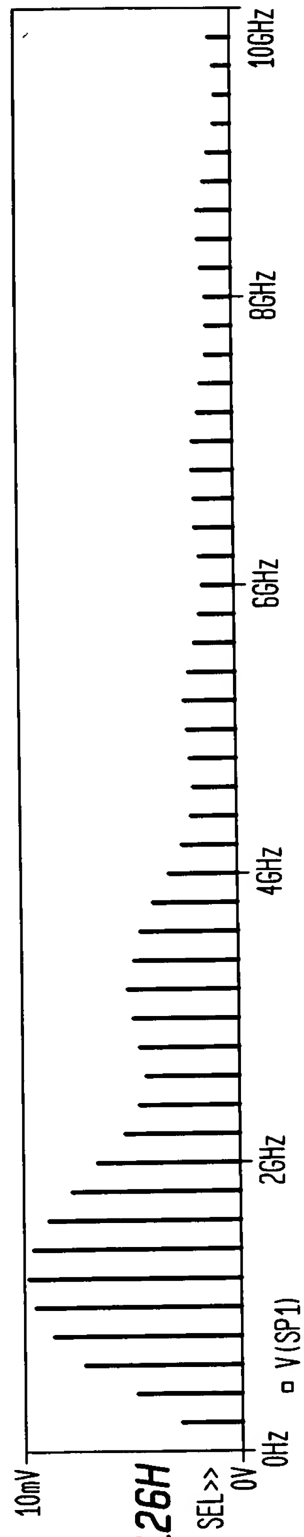


FIG. 126H

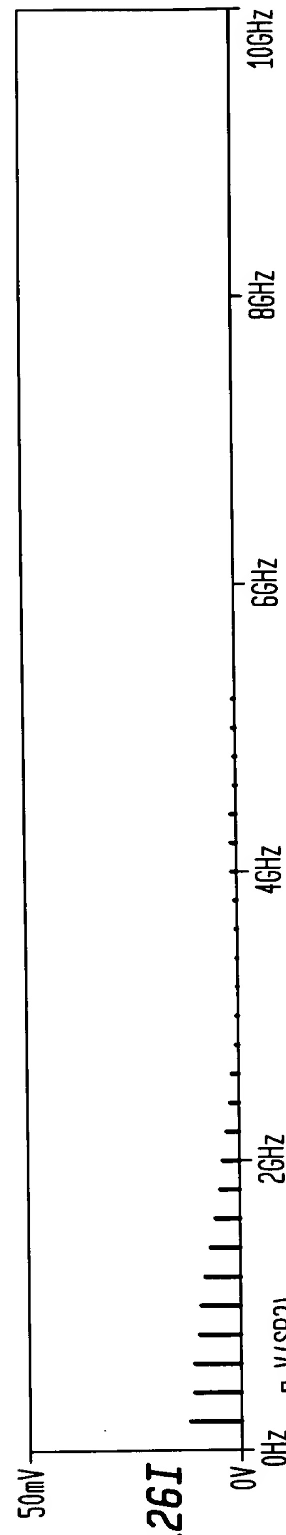


FIG. 126I

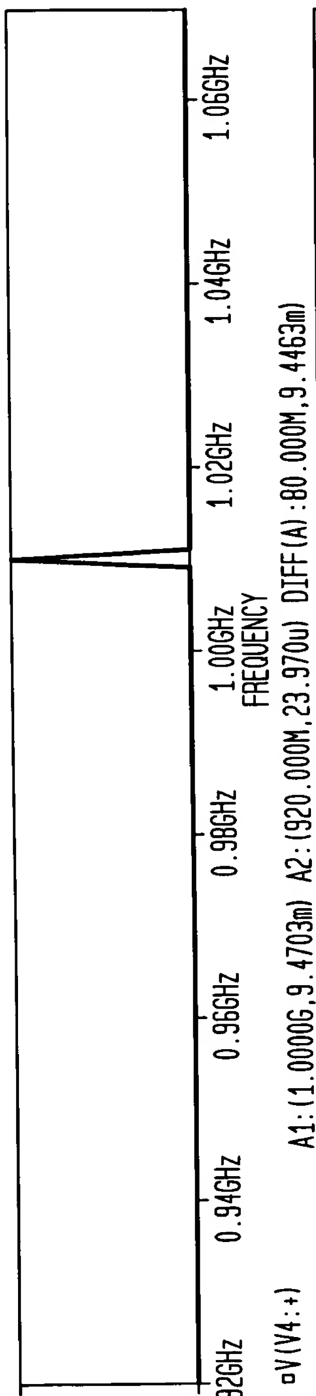


FIG. 126J

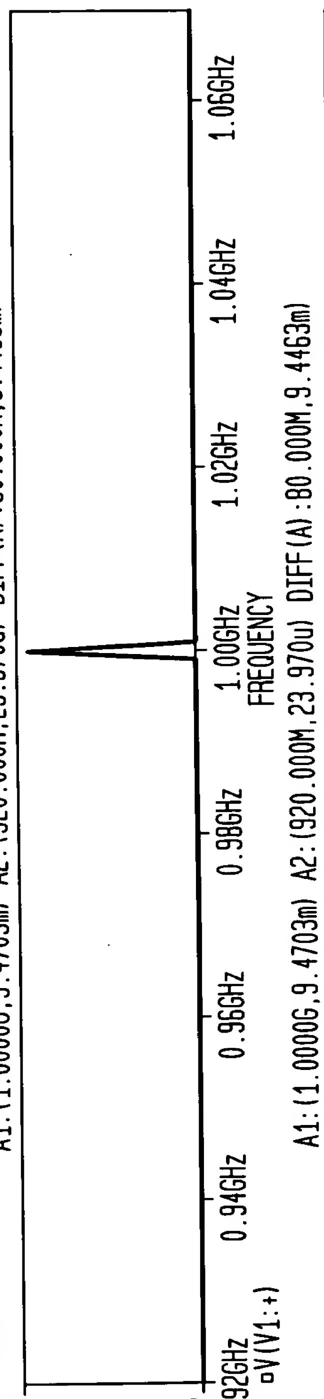


FIG. 126K

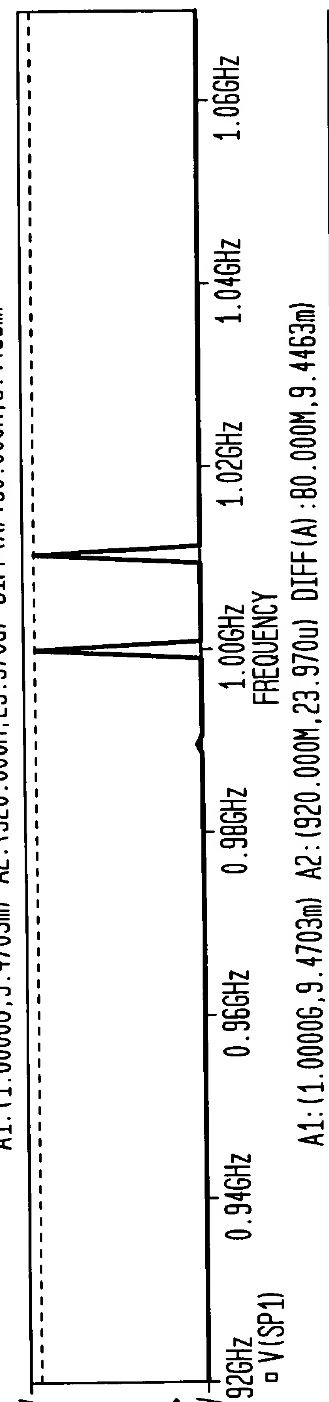


FIG. 126L

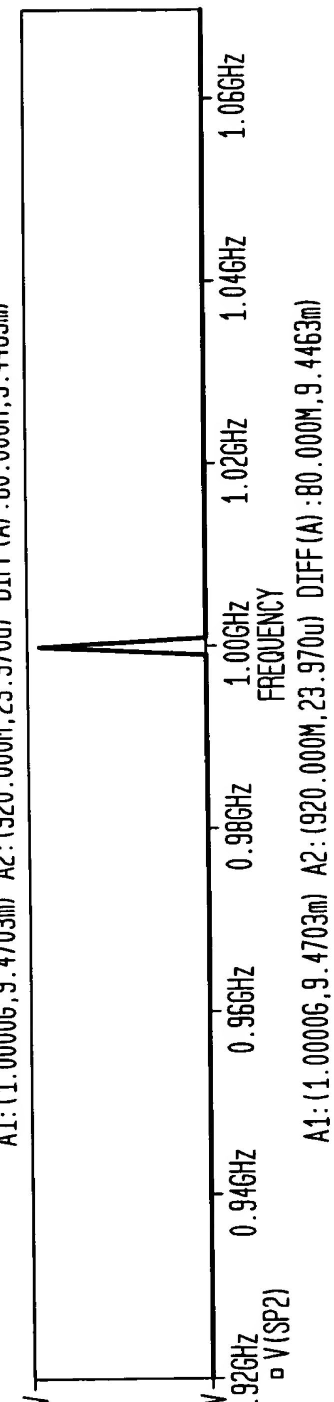


FIG. 126M

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Electromagnetic Signal, and Transforms for Same

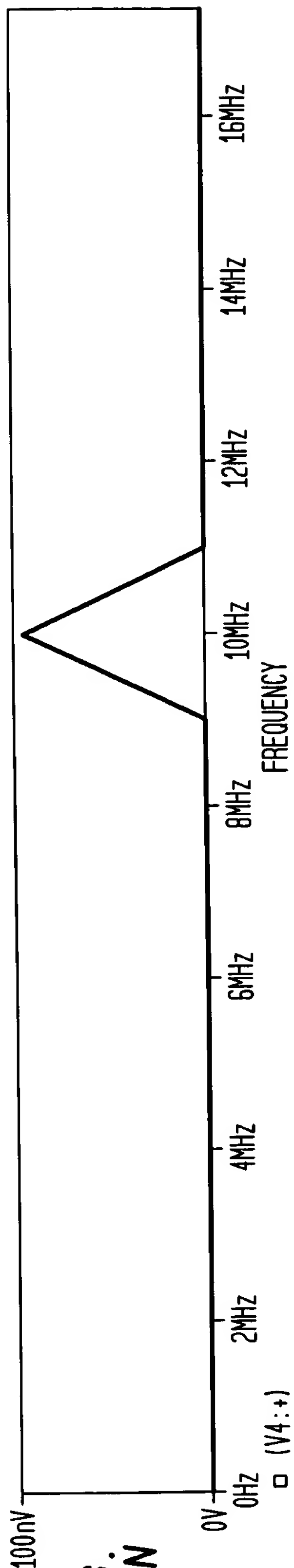

FIG. 126N

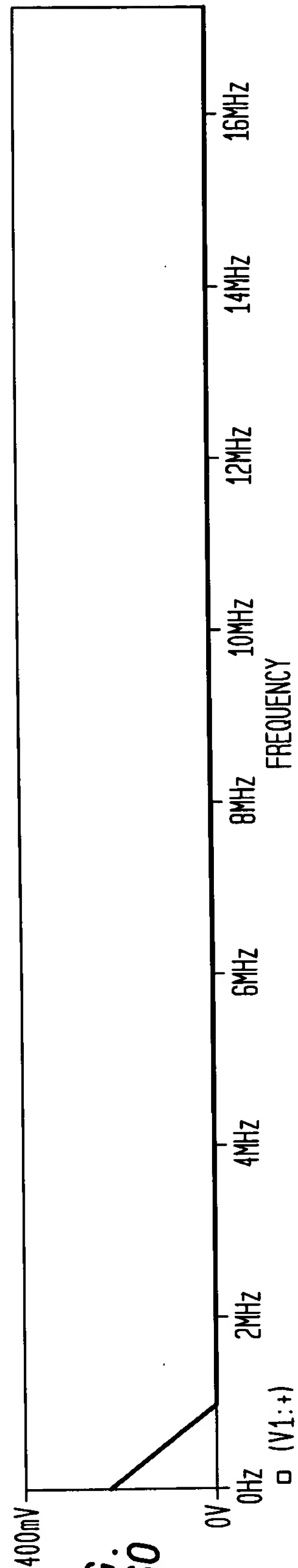

FIG. 126O

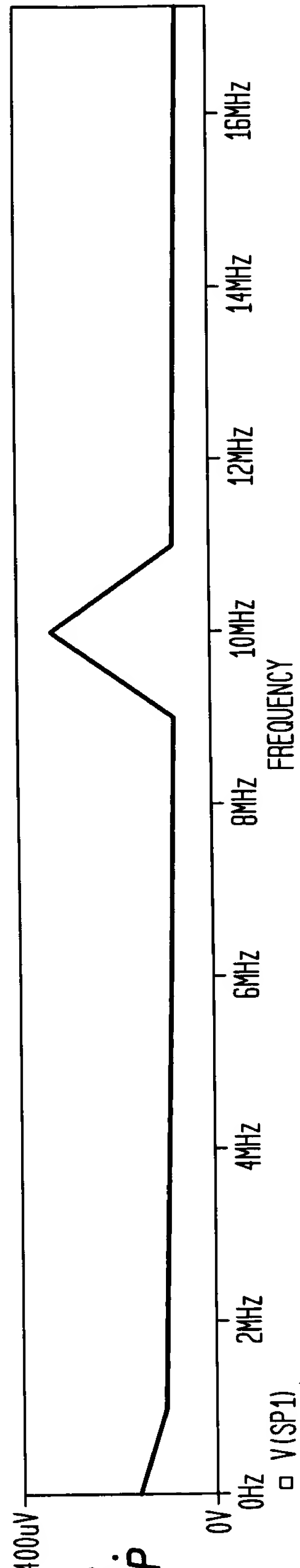

FIG. 126P

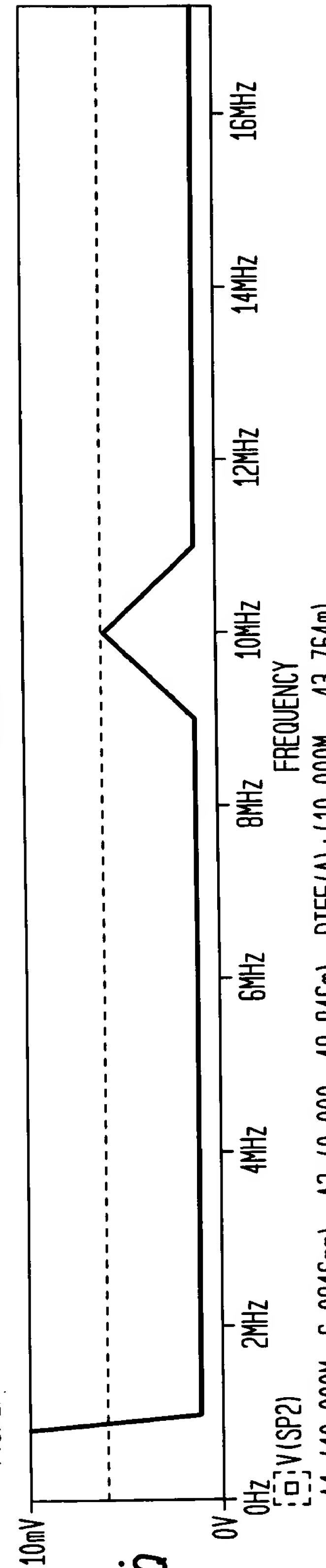

FIG. 126Q

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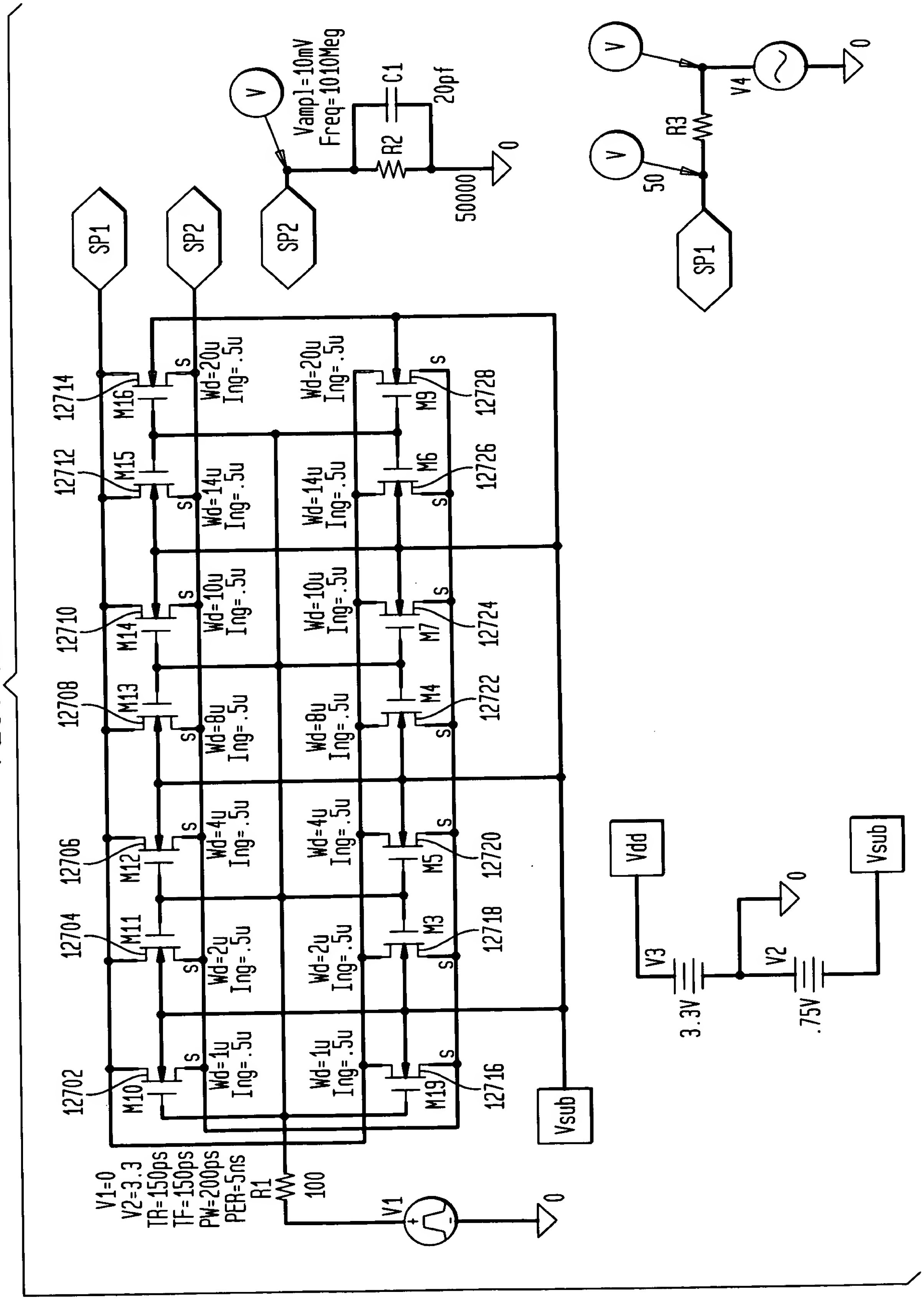
FIG. 127A



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Inventors: SORRELLS et al.
Tel. No.: 202-371-2600
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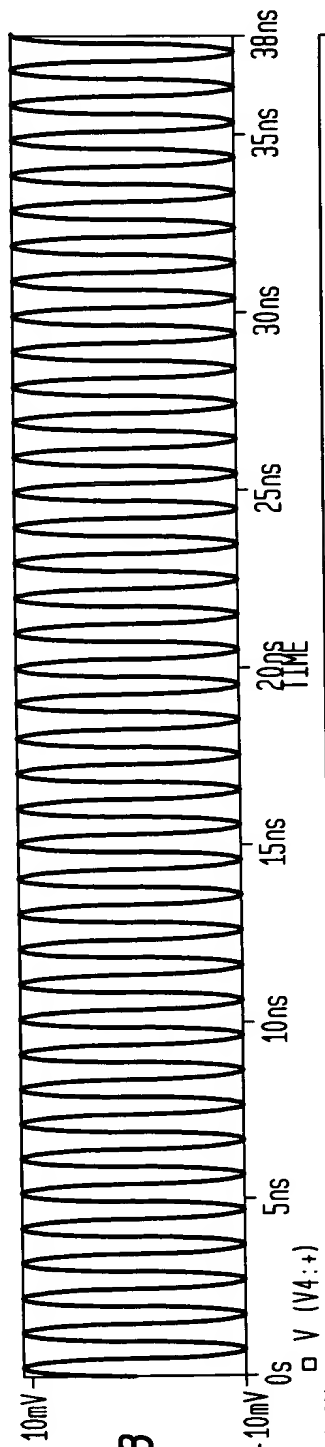

FIG. 127B

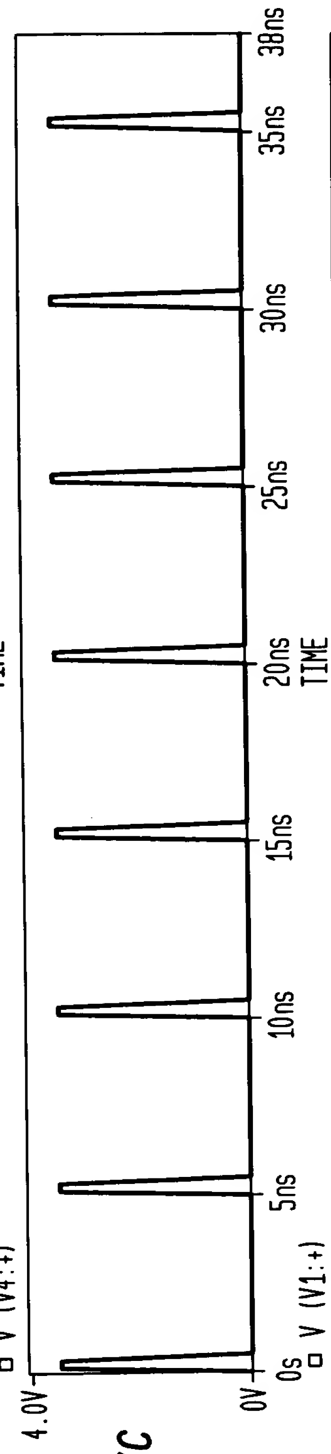

FIG. 127C

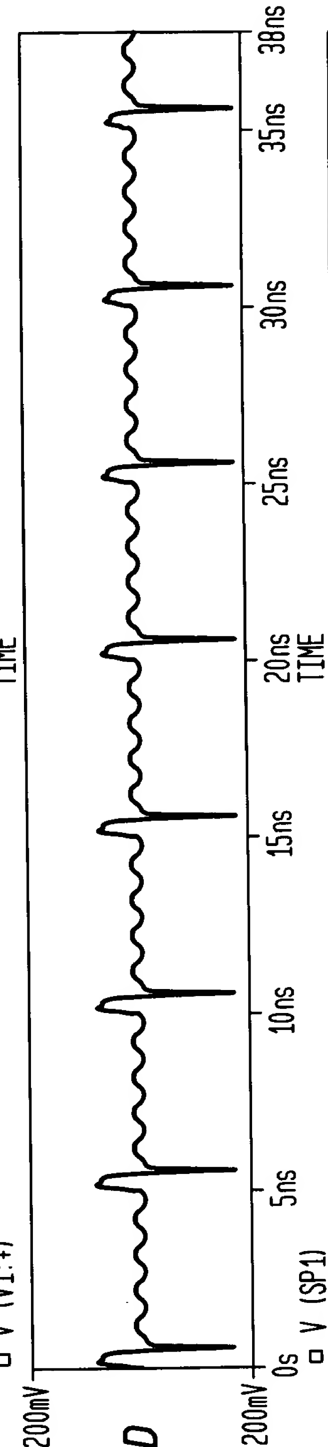

FIG. 127D

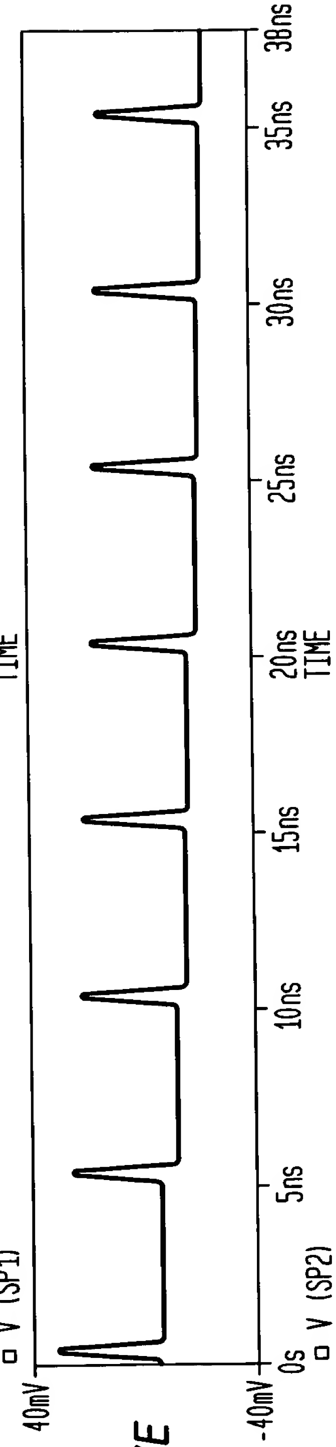

FIG. 127E

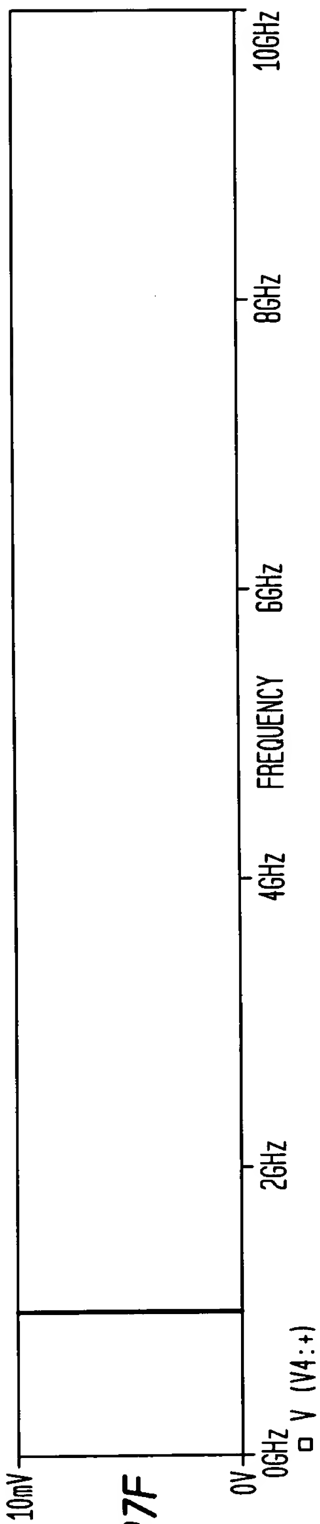

FIG. 127F

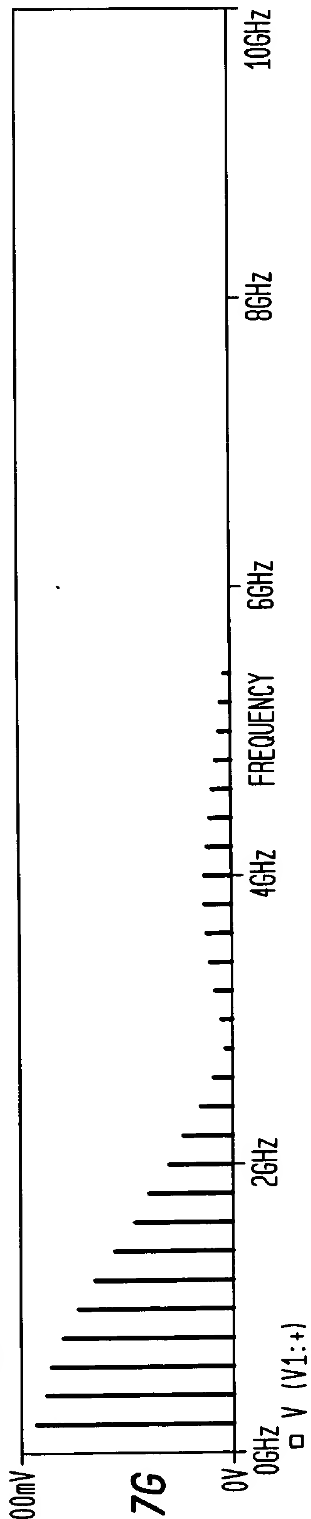

FIG. 127G

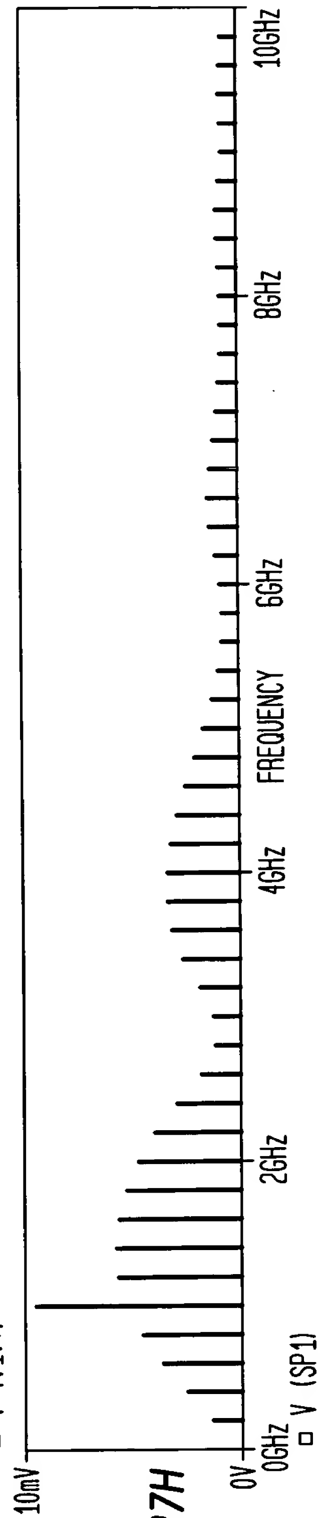

FIG. 127H

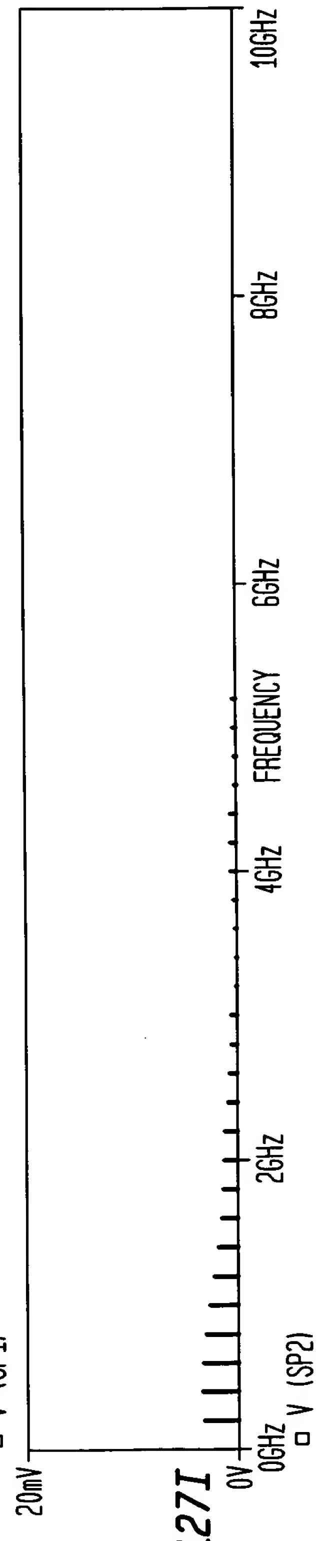

FIG. 127I

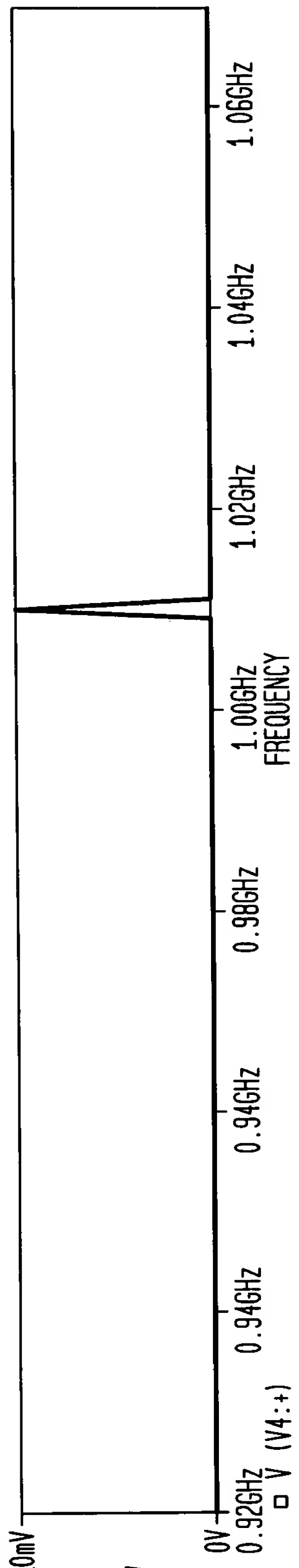

FIG. 127J

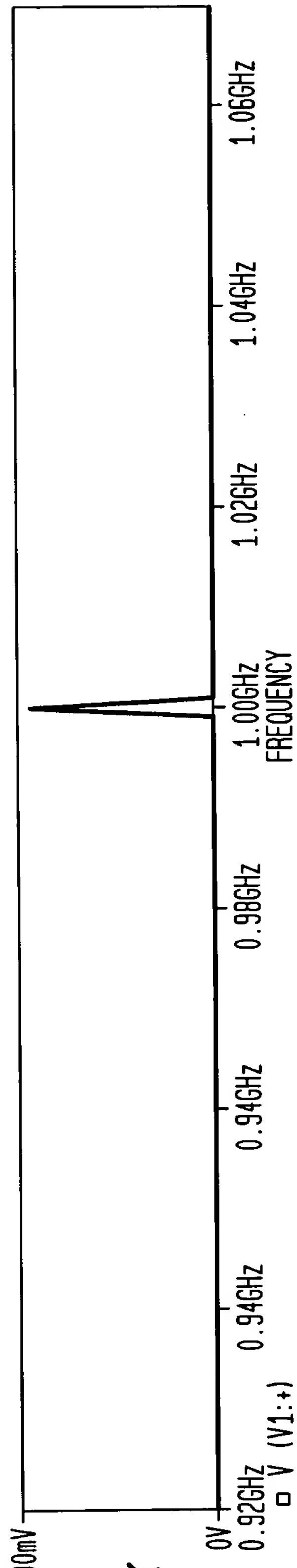

FIG. 127K

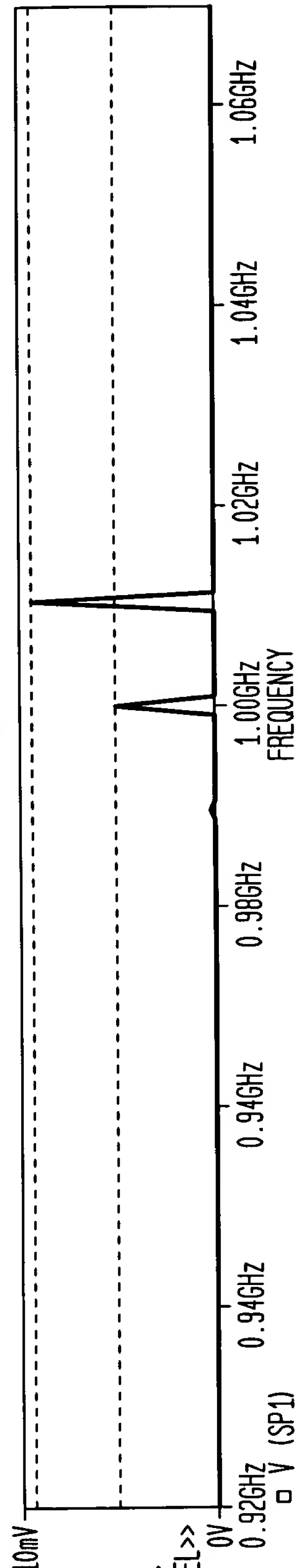

FIG. 127L

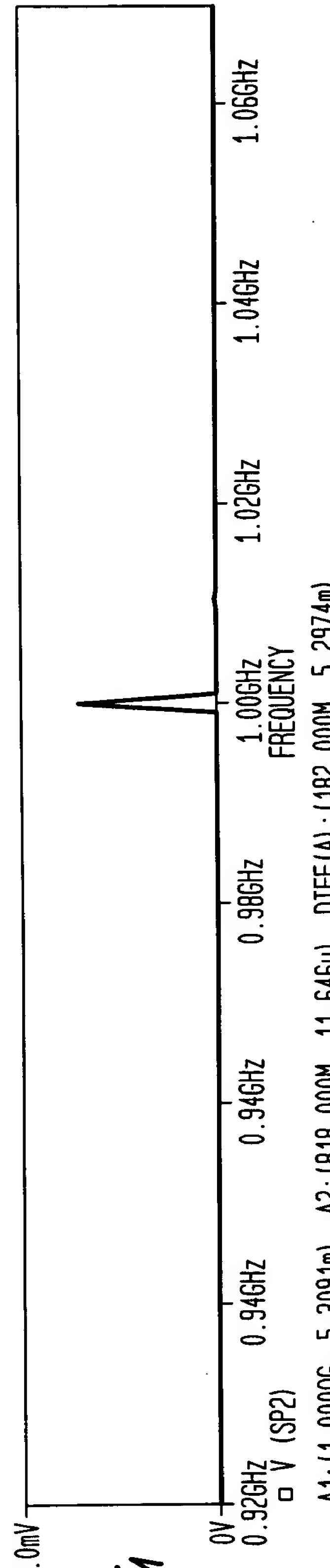

FIG. 127M

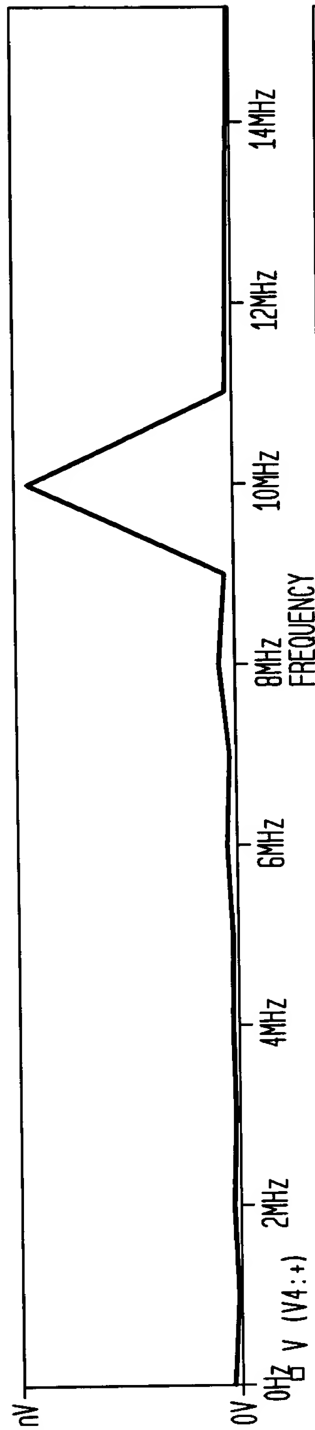

FIG. 127N

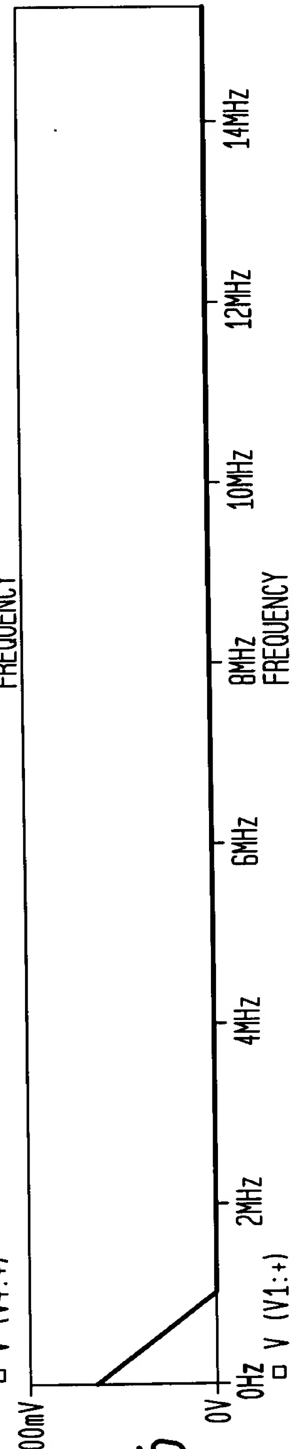

FIG. 127O

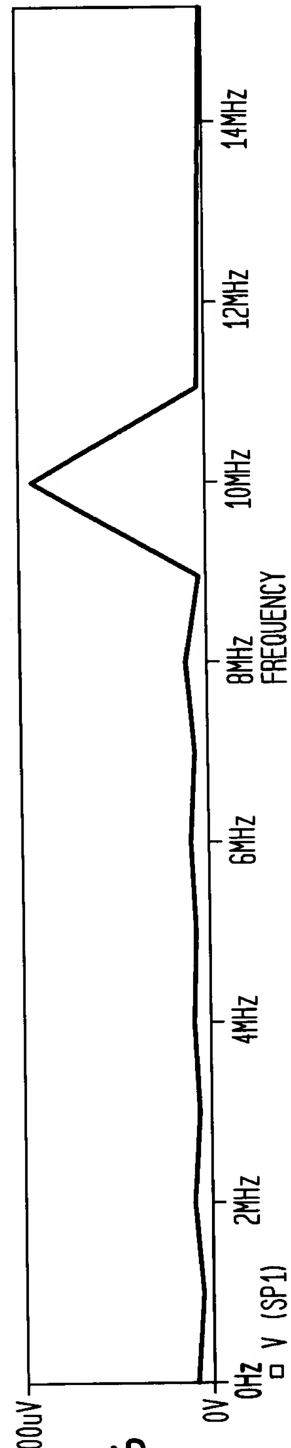

FIG. 127P

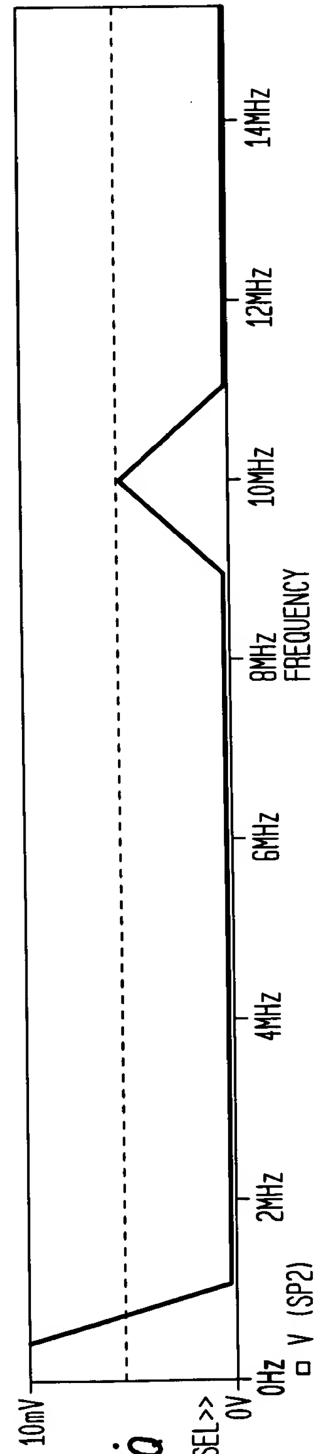

FIG. 127Q

FIG. 128A

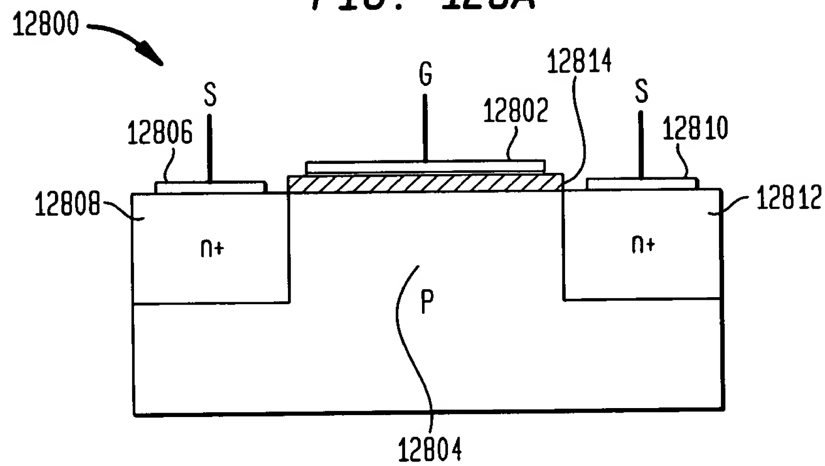

FIG. 128B

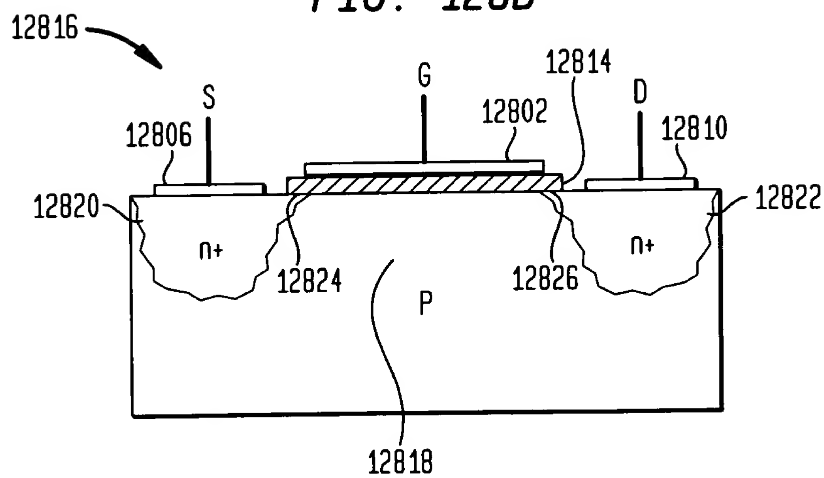

FIG. 128C

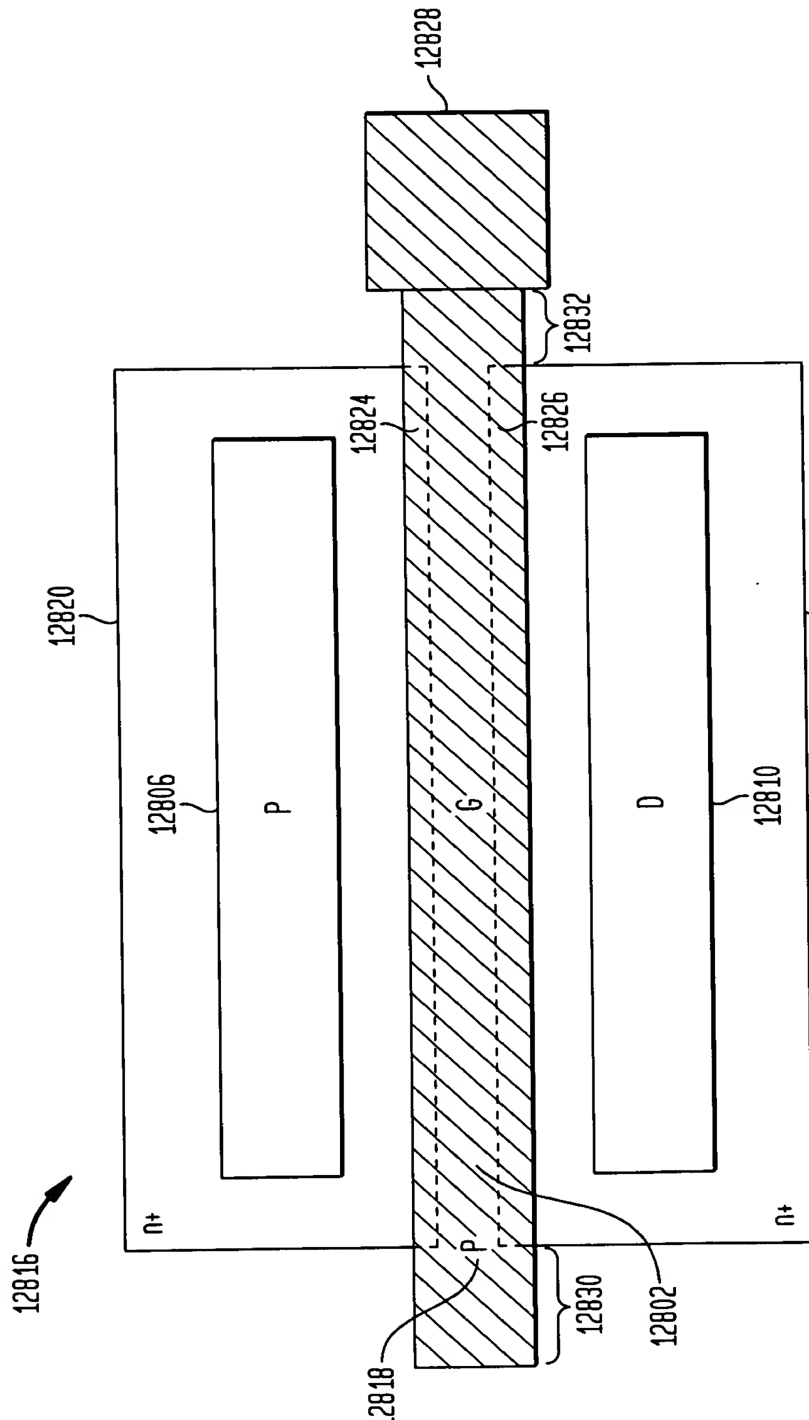
12828
12832
12824
12826
12820
12822
12806
P
G
D
12810
n+
n+
12816
P
12818
12830
12802

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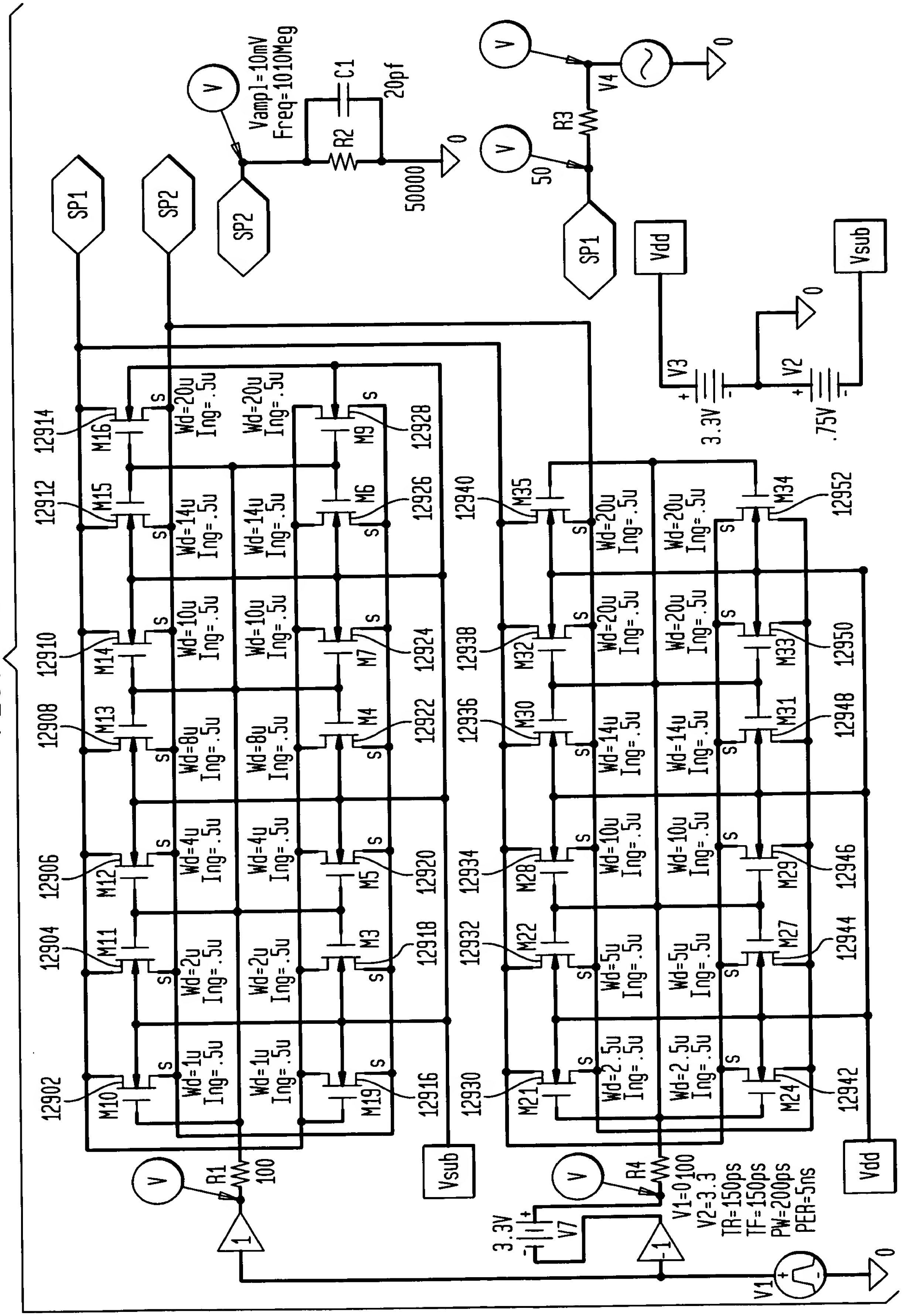
FIG. 129A



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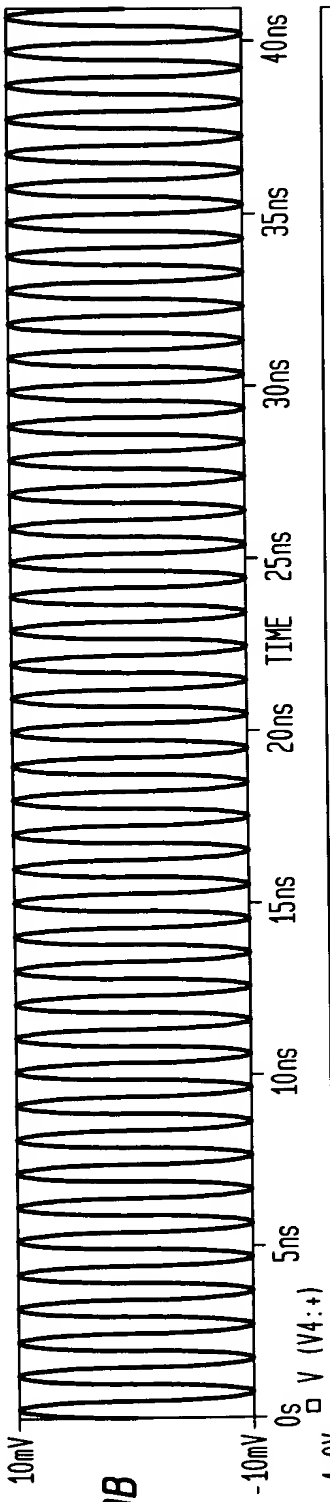

FIG. 129B

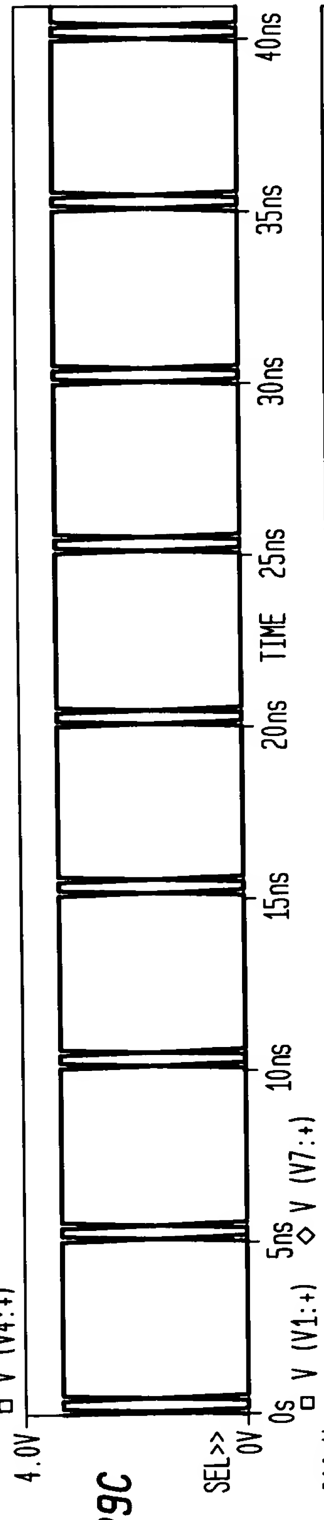

FIG. 129C

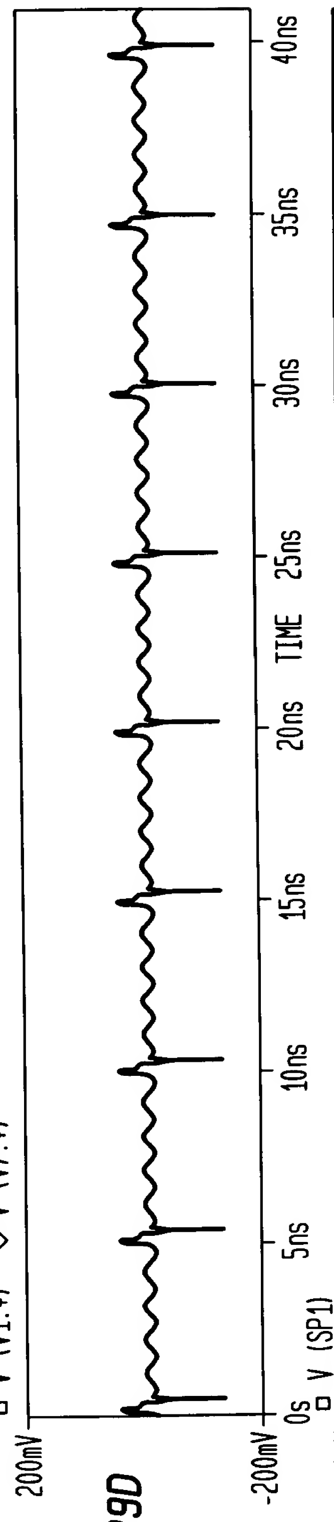

FIG. 129D

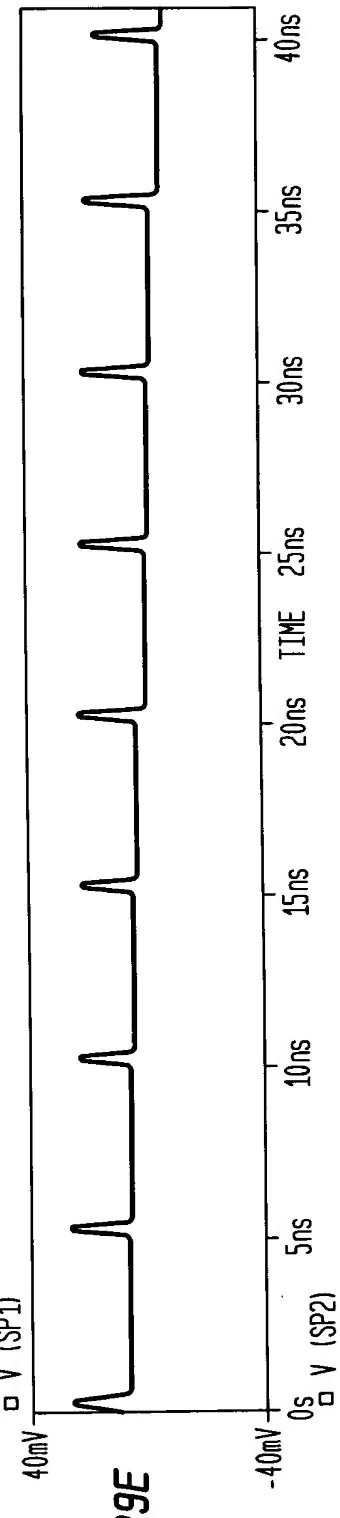

FIG. 129E

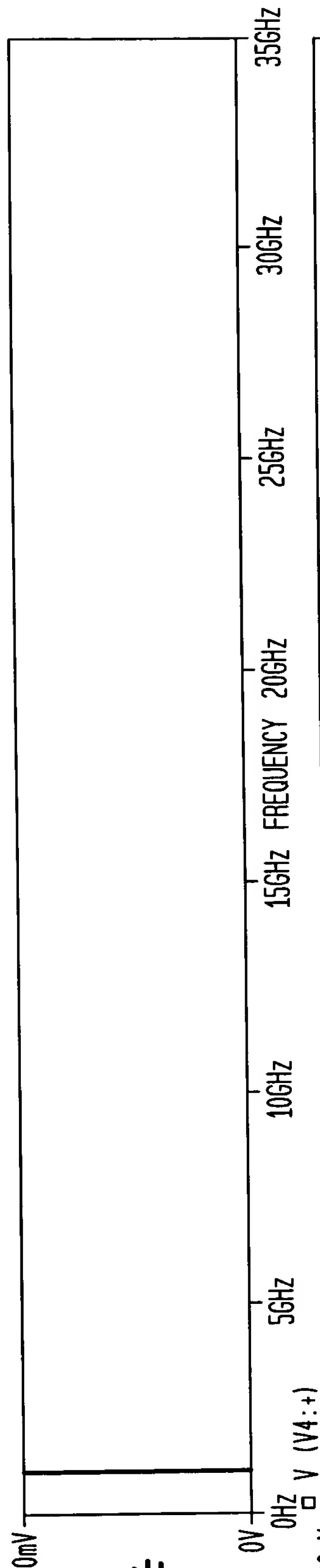

FIG. 129F

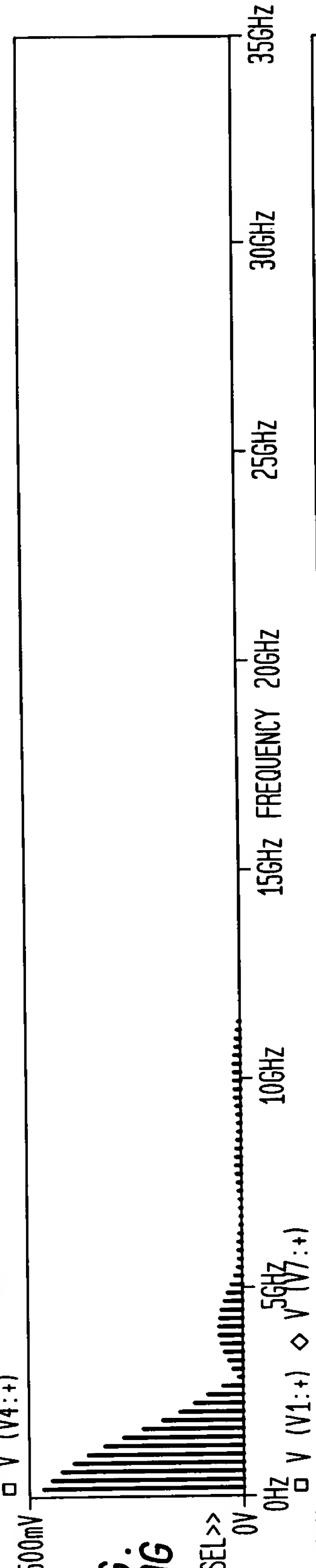

FIG. 129G

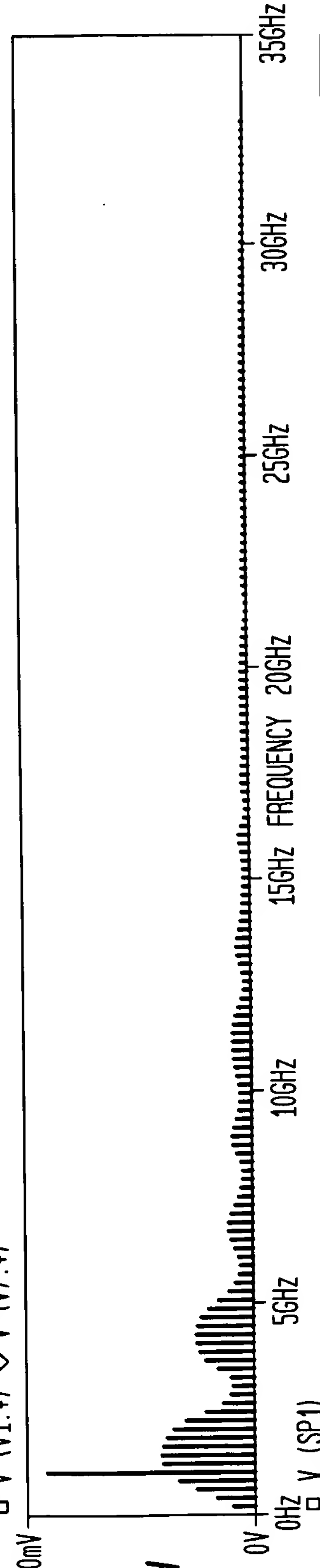

FIG. 129H

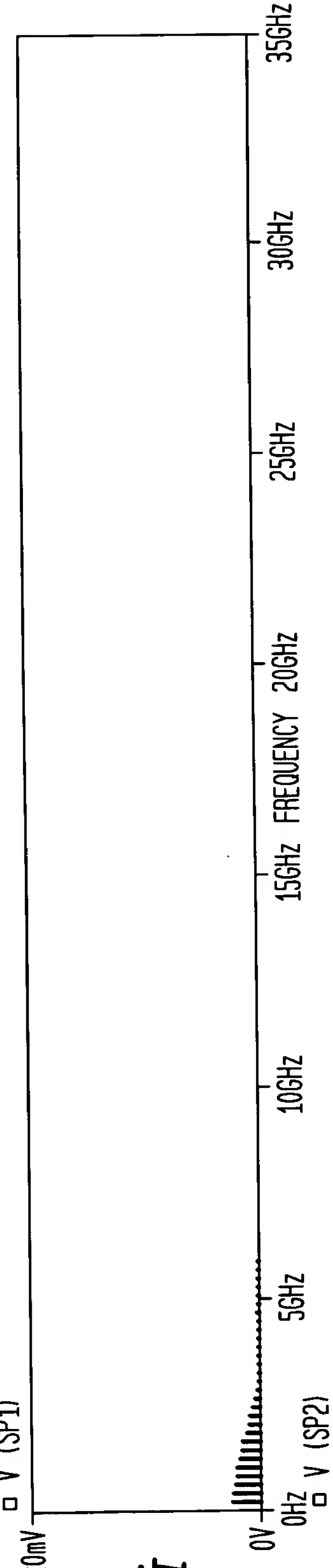

FIG. 129I

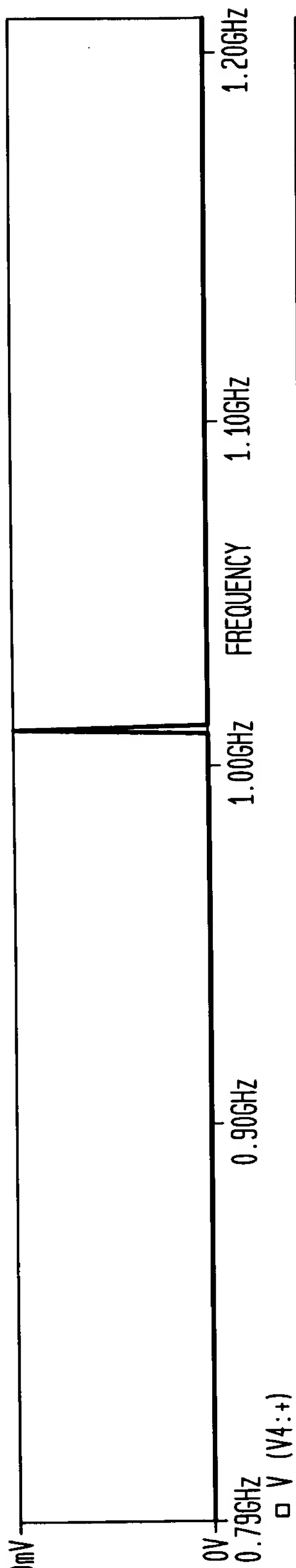

FIG. 129J

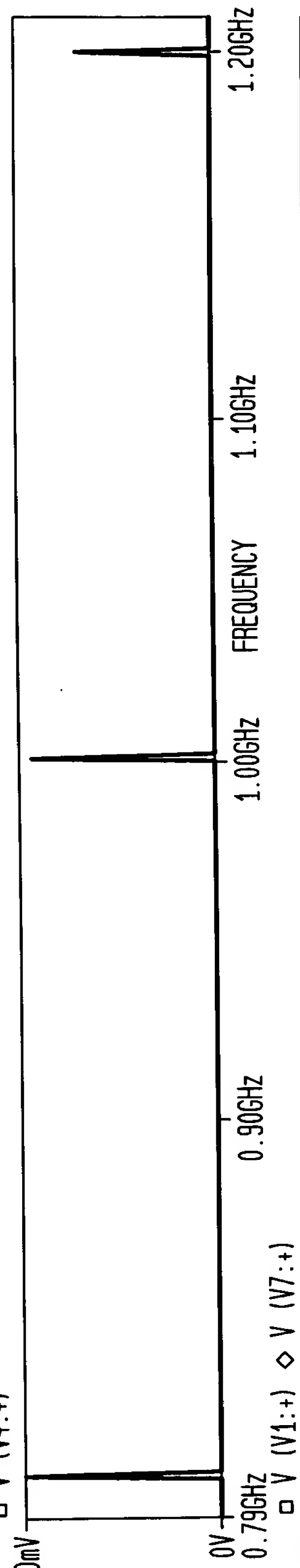

FIG. 129K

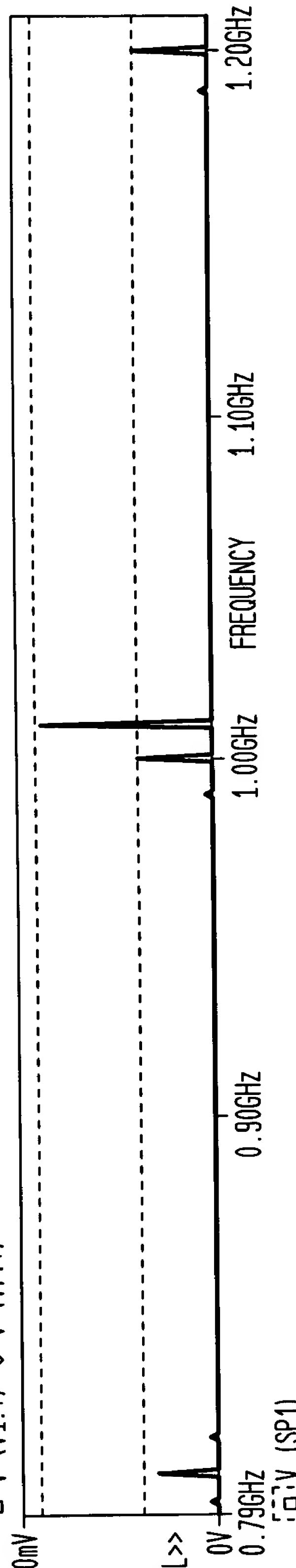

FIG. 129L

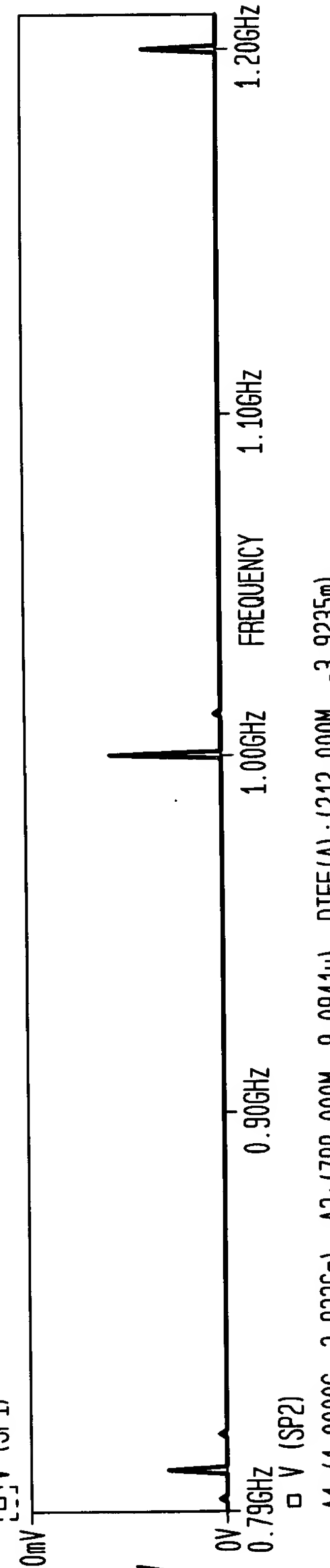

FIG. 129M

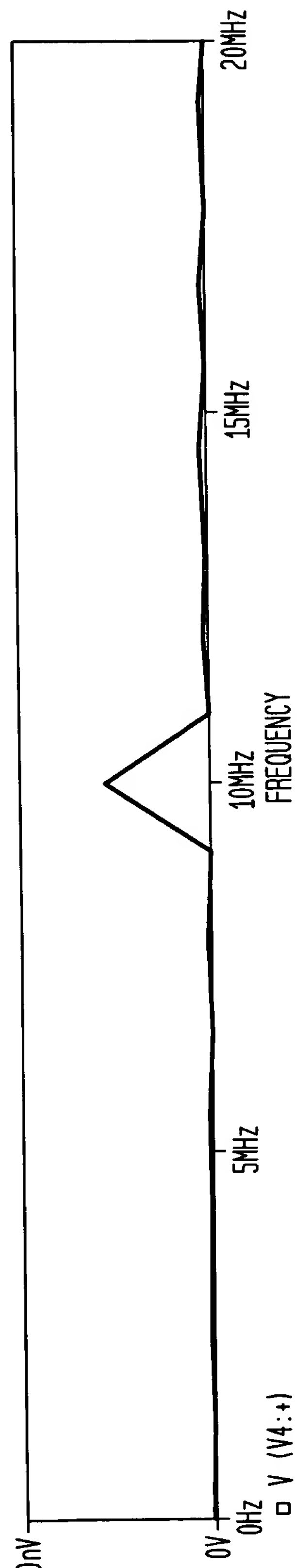

FIG. 129N

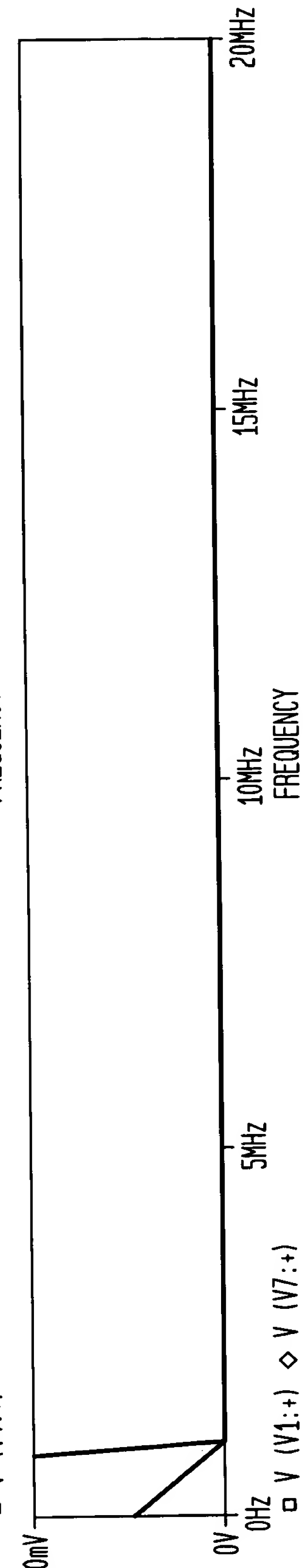

FIG. 129O

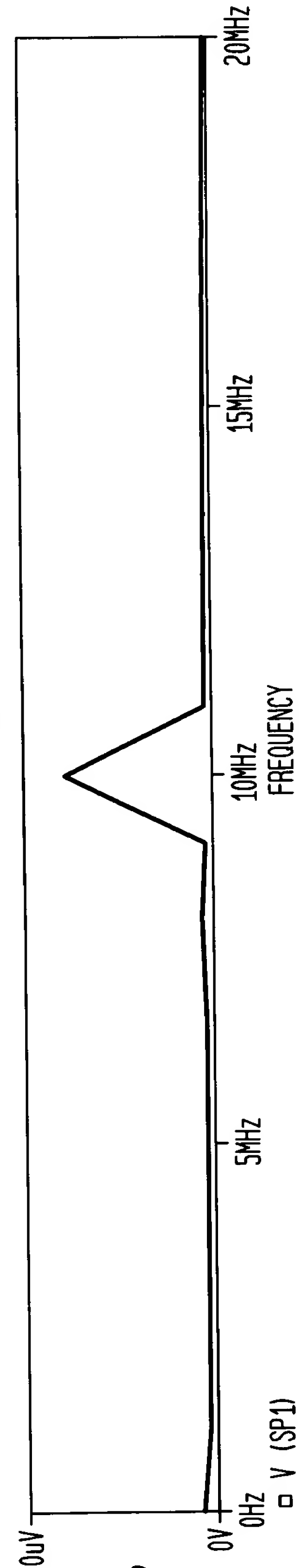

FIG. 129P

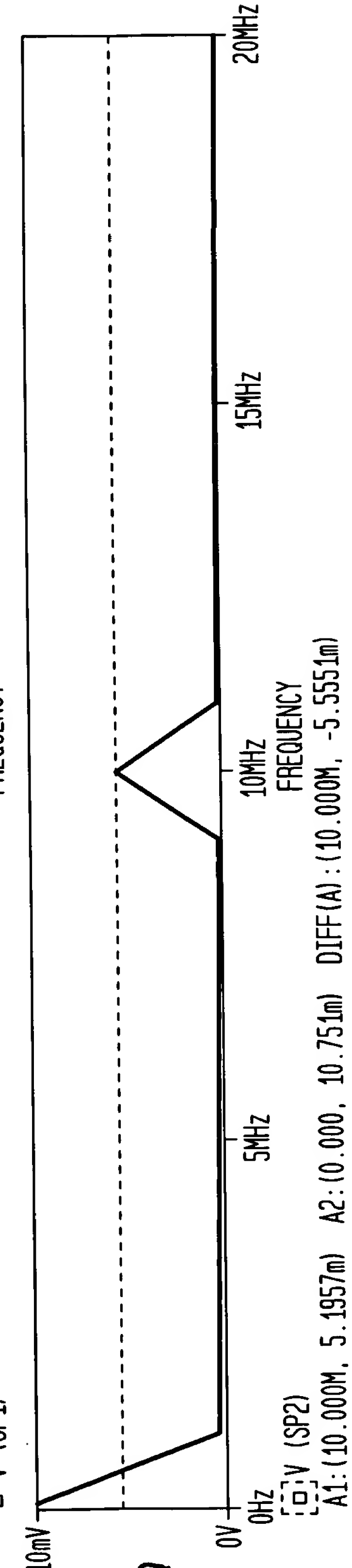

FIG. 129Q

FIG. 130

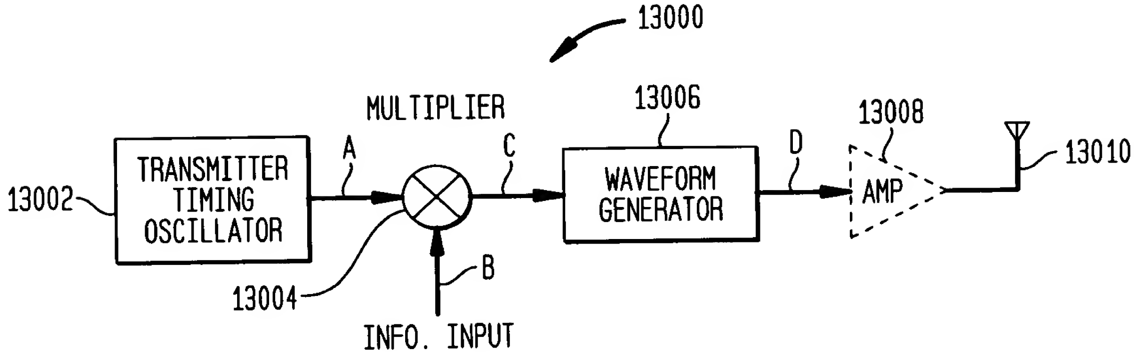
13000
MULTIPLIER
13006
13008
13010
13002
TRANSMITTER
TIMING
OSCILLATOR
A
C
WAVEFORM
GENERATOR
D
AMP
13004
B
INFO. INPUT

FIG. 131

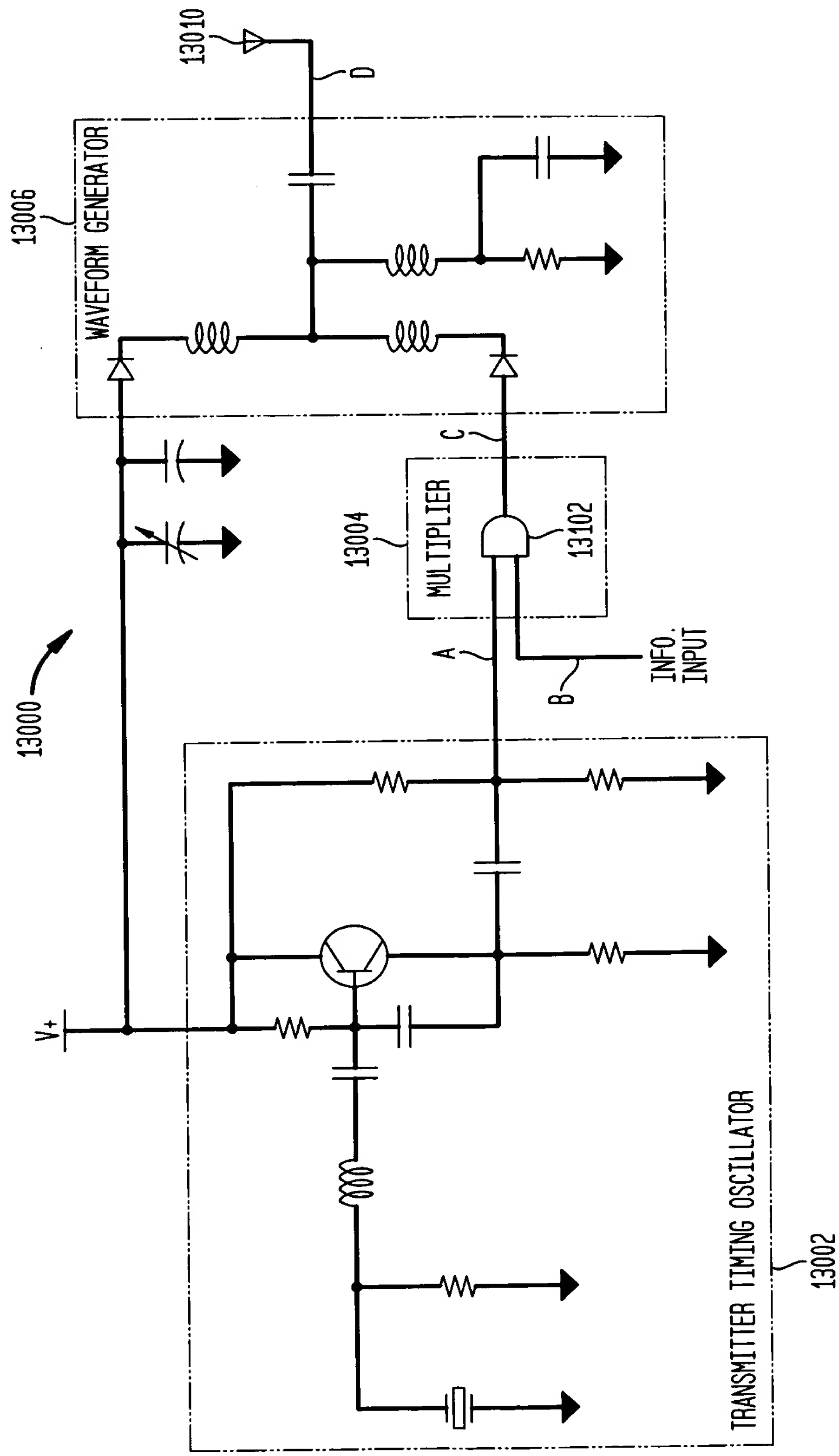
13000
13010
D
WAVEFORM GENERATOR
13006
C
MULTIPLIER
13004
13102
A
B
INFO.
INPUT
V+
TRANSMITTER TIMING OSCILLATOR
13002

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FIG. 132A

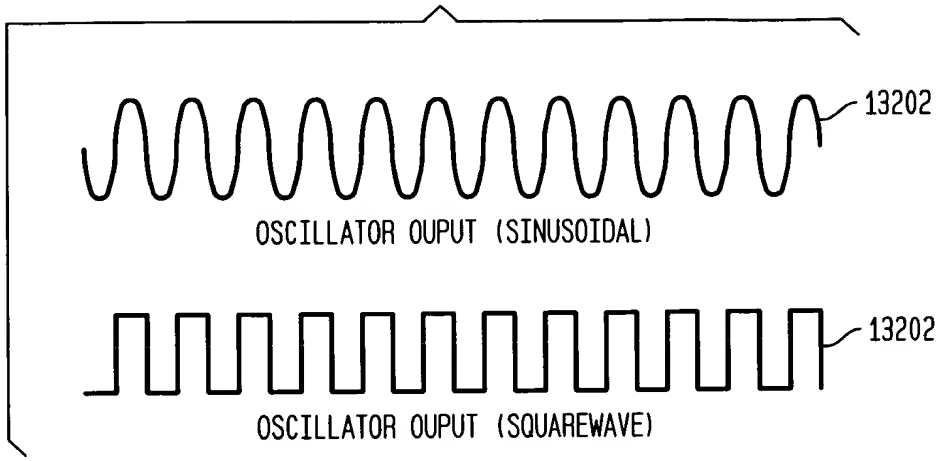

FIG. 132B

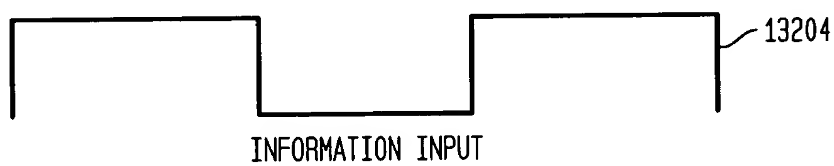

FIG. 132C

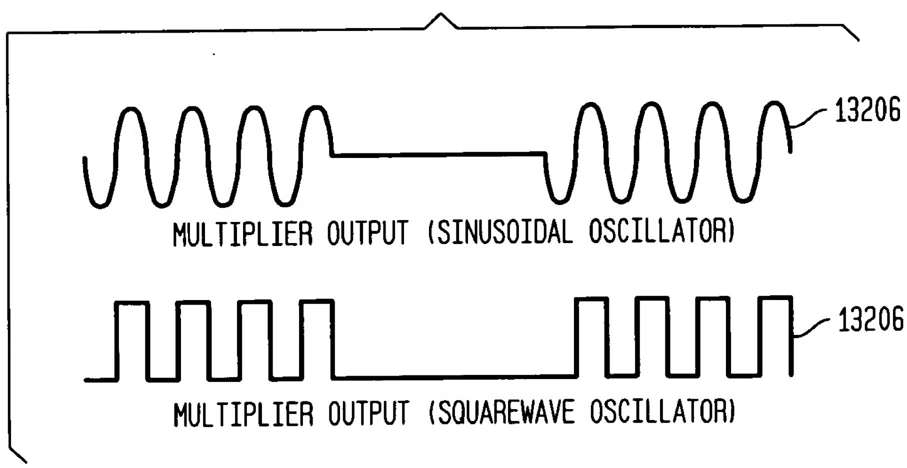

FIG. 132D

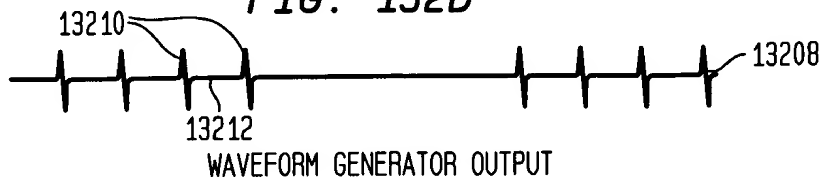

FIG. 133

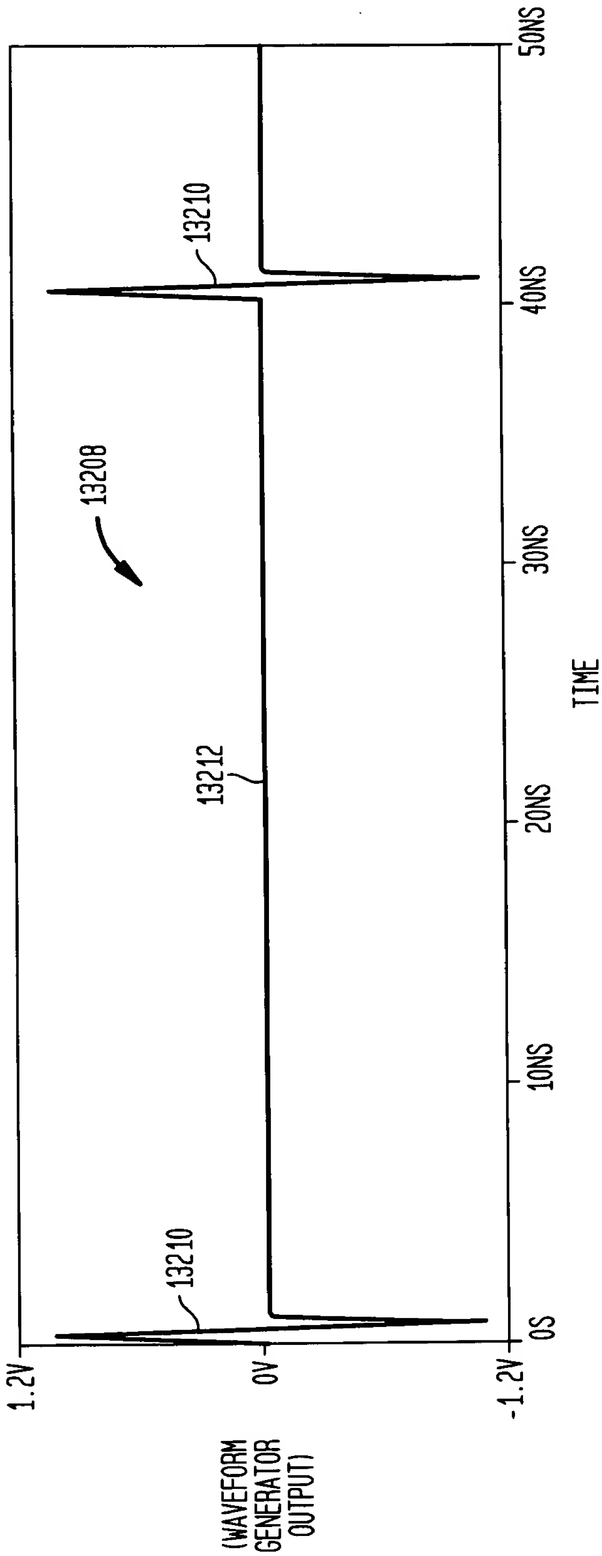
13208
13210
13210
13212
1.2V
0V
-1.2V
(WAVEFORM GENERATOR OUTPUT)
0S
10NS
20NS
30NS
40NS
50NS
TIME

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FIG. 134

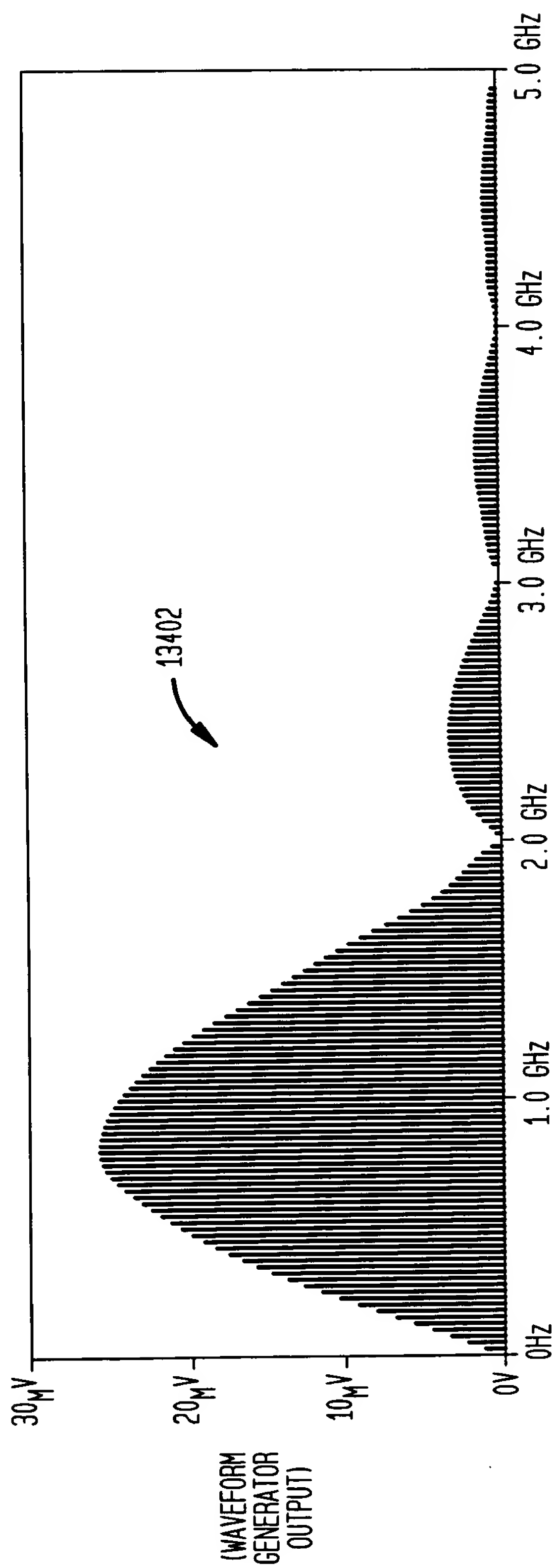

FIG. 135

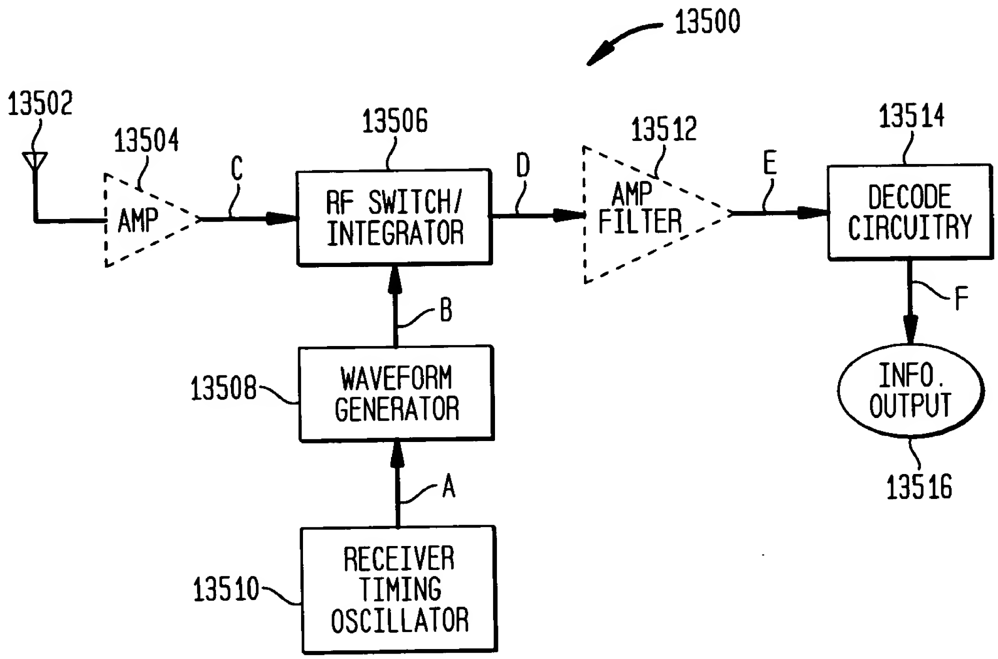
13500
13502
13504
AMP
C
13506
RF SWITCH/
INTEGRATOR
D
13512
AMP
FILTER
E
13514
DECODE
CIRCUITRY
F
INFO.
OUTPUT
13516
B
13508
WAVEFORM
GENERATOR
A
13510
RECEIVER
TIMING
OSCILLATOR

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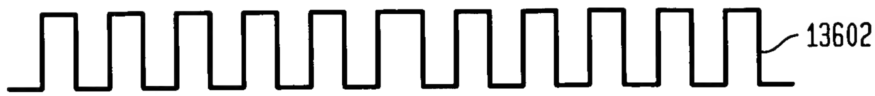
FIG. 136A



RECEIVER TIMING OSCILLATOR OUTPUT

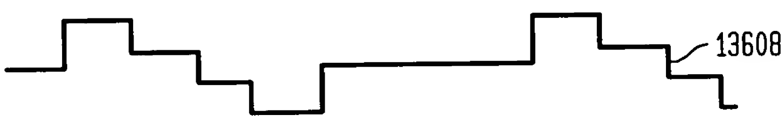
FIG. 136B

WAVEFORM GENERATOR OUTPUT

FIG. 136C

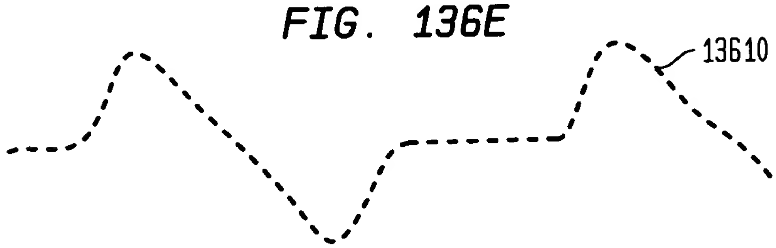
RF INPUT

FIG. 136D



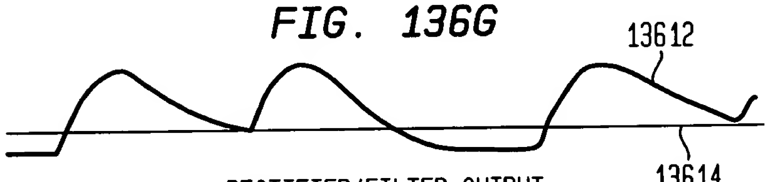
RF SWITCH/INTEGRATOR OUTPUT

FIG. 136E



OPTIONAL AMPLIFIER/FILTER OUTPUT

FIG. 136G



RECTIFIER/FILTER OUTPUT
VARIABLE THRESHOLD GENERATOR OUTPUT

FIG. 136F

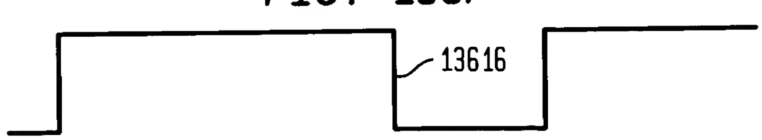


FIG. 137

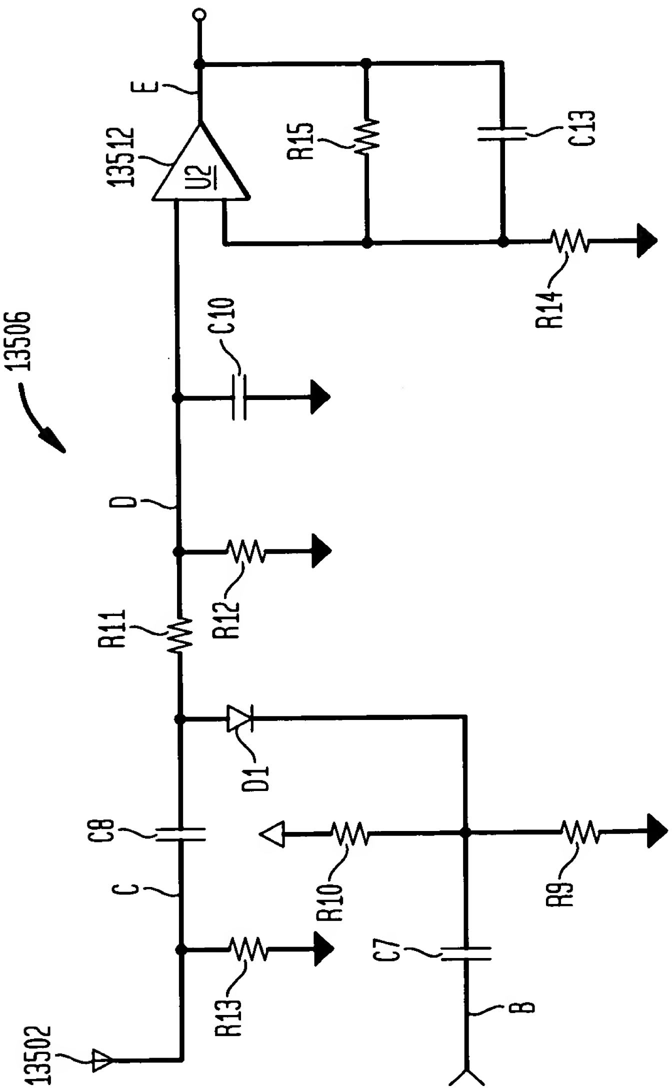

13506
13502
R13
C
C8
D1
R11
R12
D
C10
13512
U2
E
R15
C13
R14
R10
R9
C7
B

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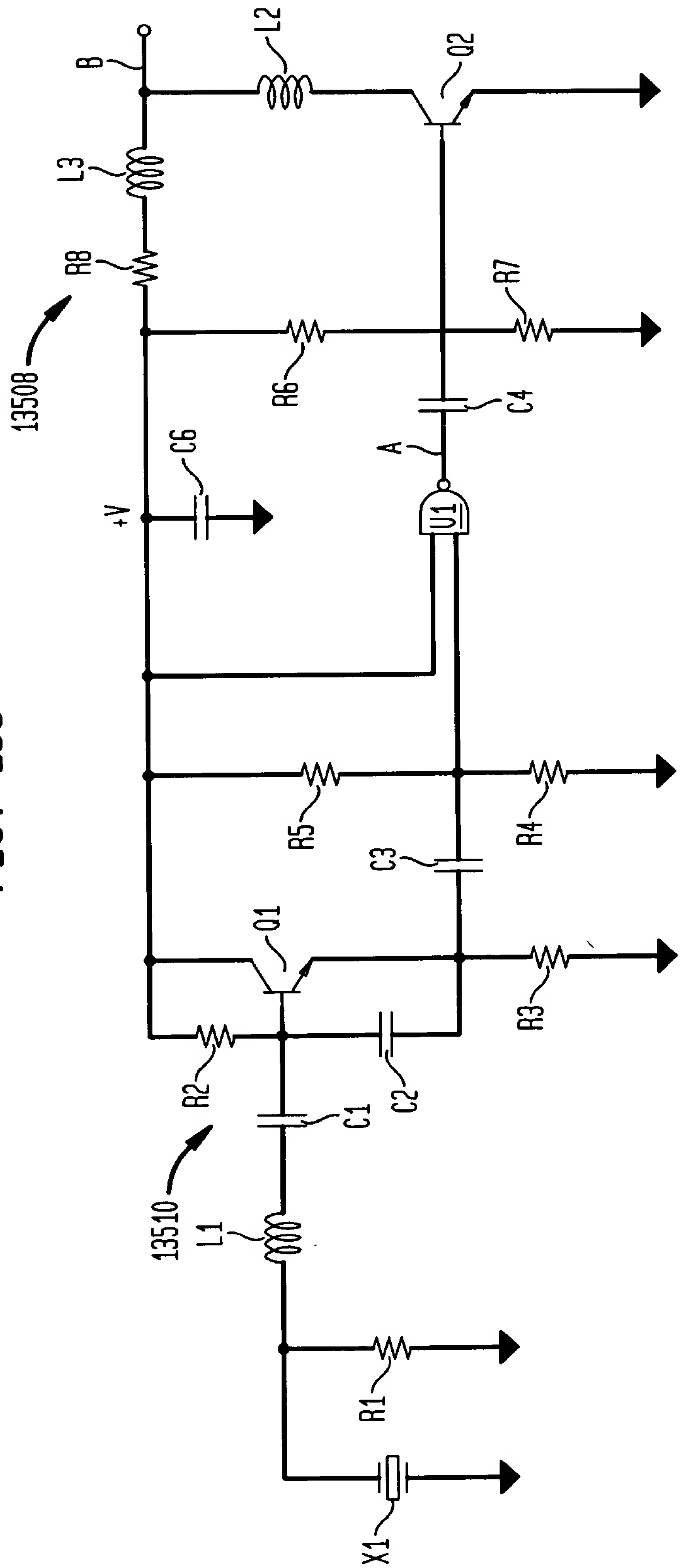
FIG. 138



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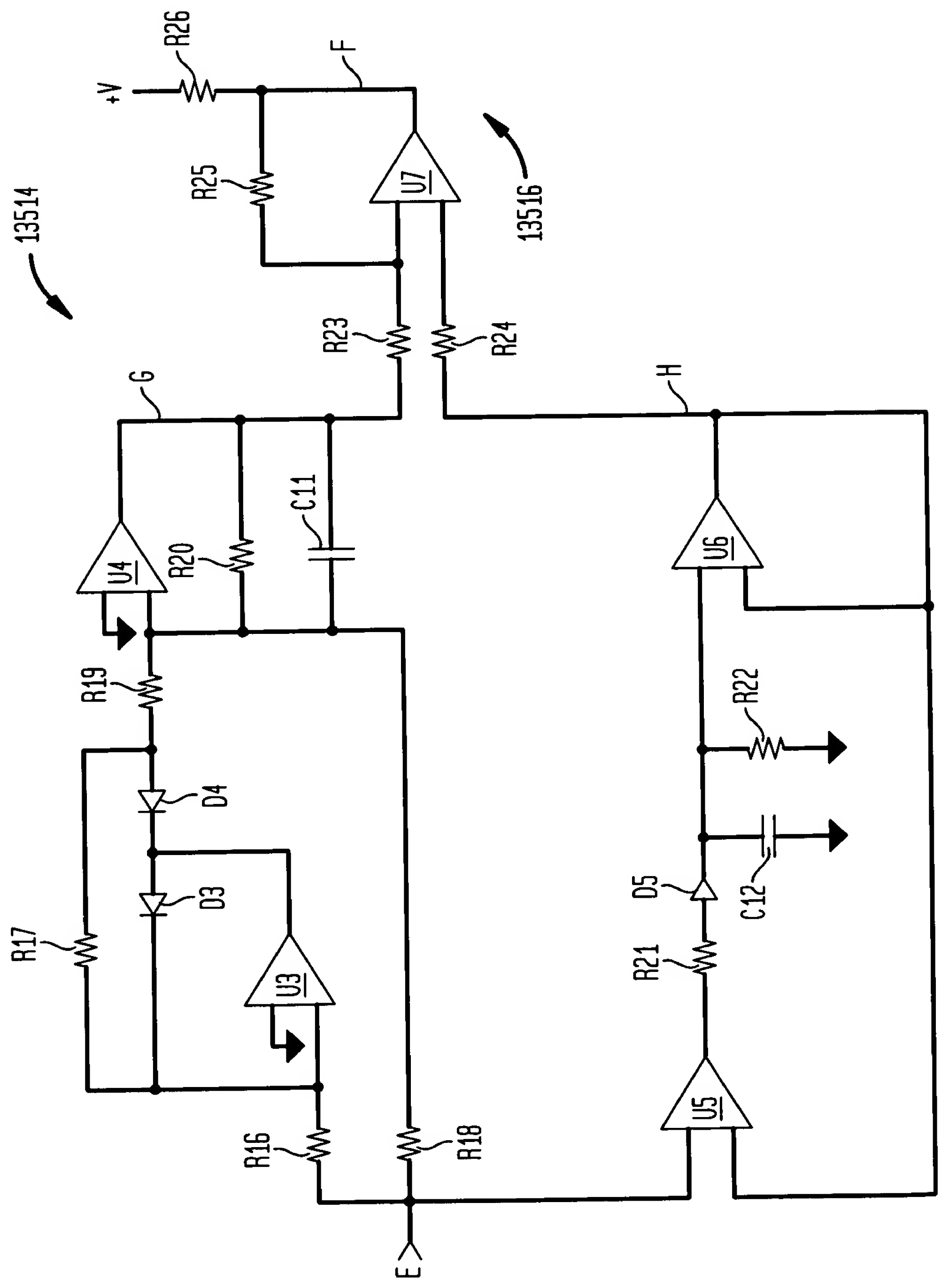

FIG. 139

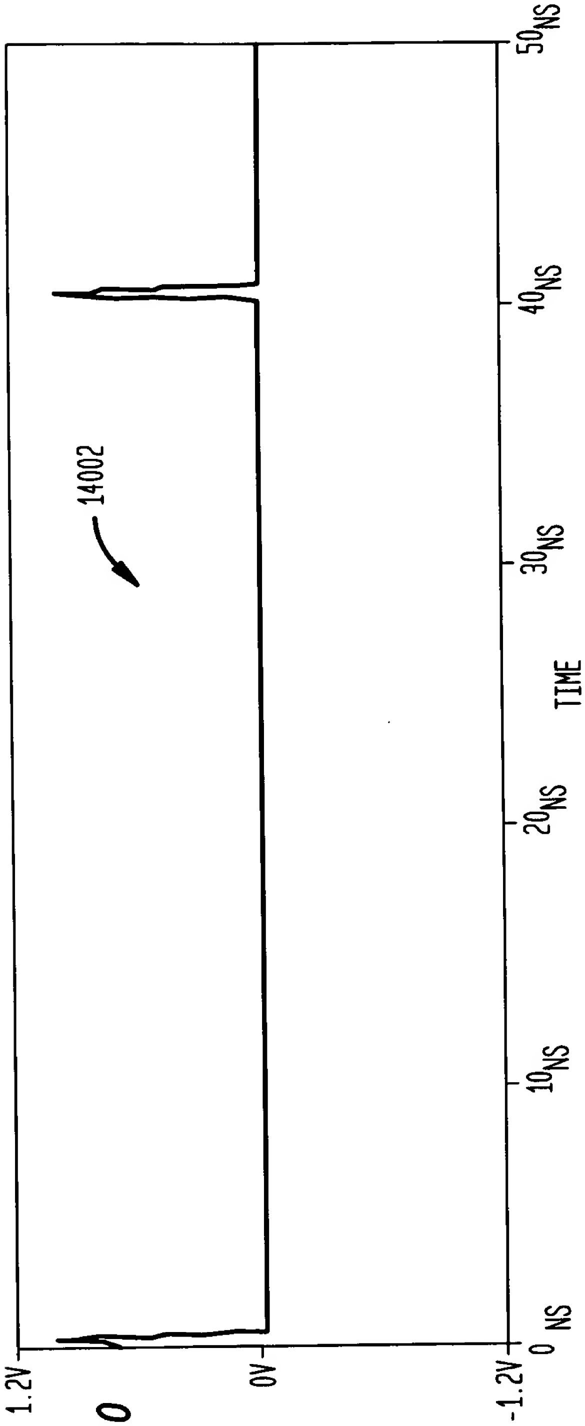

FIG. 140

(WAVEFORM GENERATOR OUTPUT)

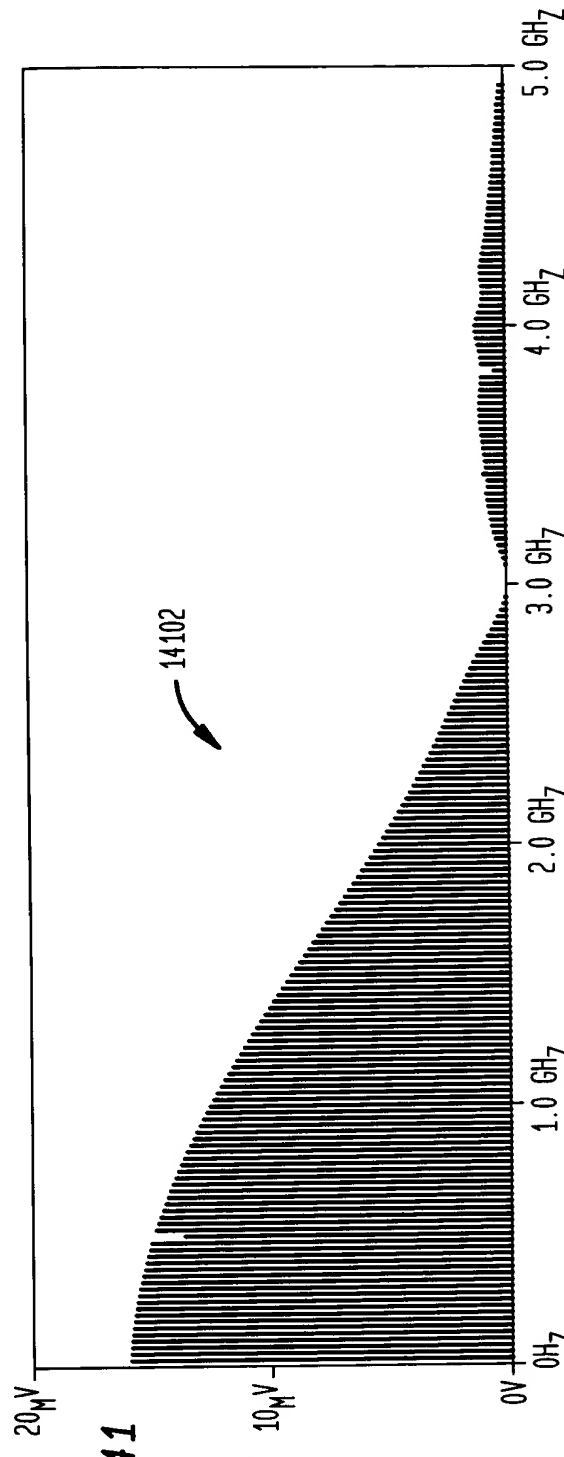

FIG. 141

(WAVEFORM GENERATOR OUTPUT)

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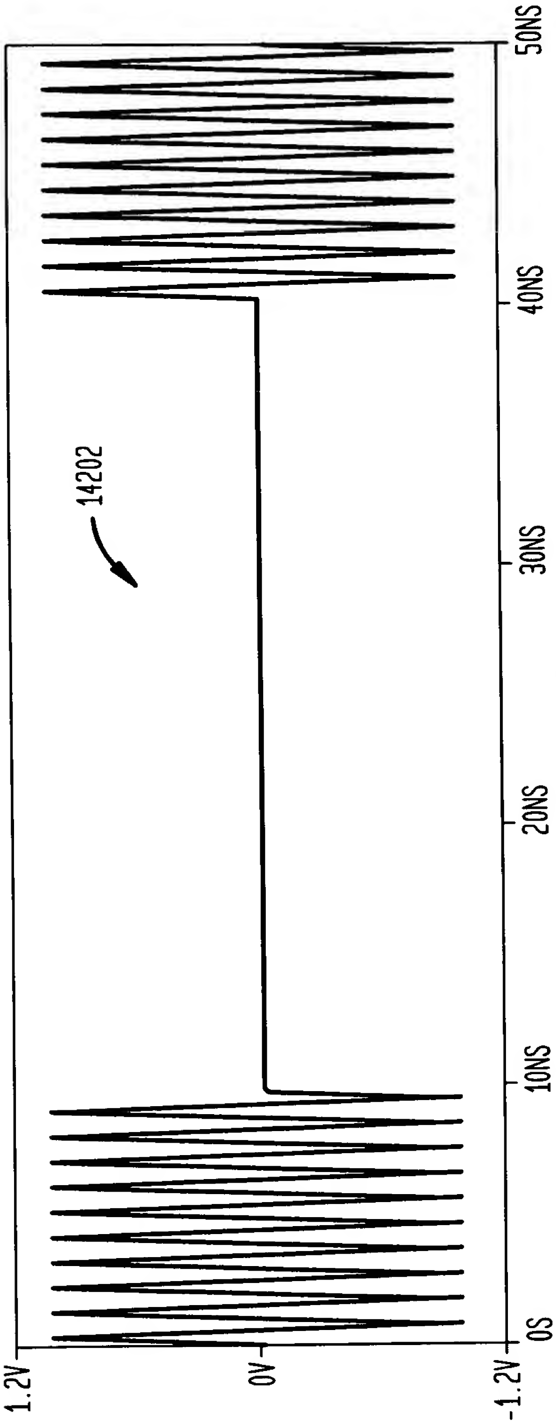

FIG. 142

(WAVEFORM GENERATOR OUTPUT)

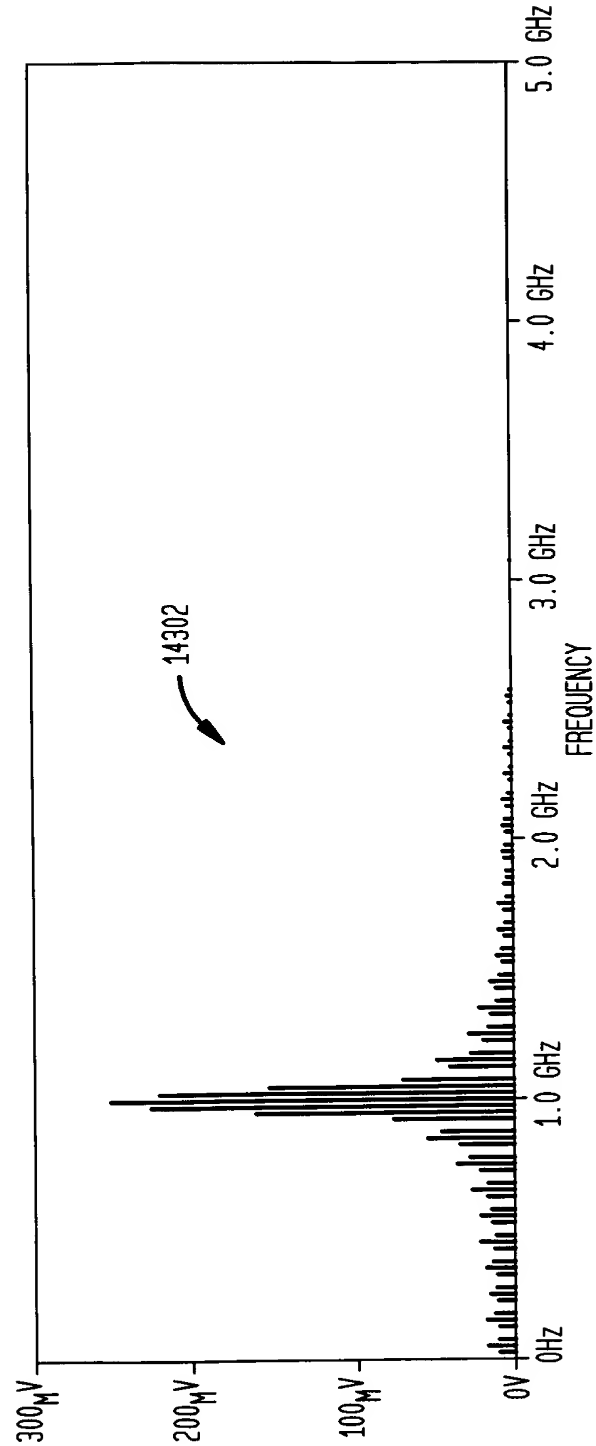

FIG. 143

(WAVEFORM GENERATOR OUTPUT)

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FIG. 144

RF DIFFERENTIAL RECEIVER

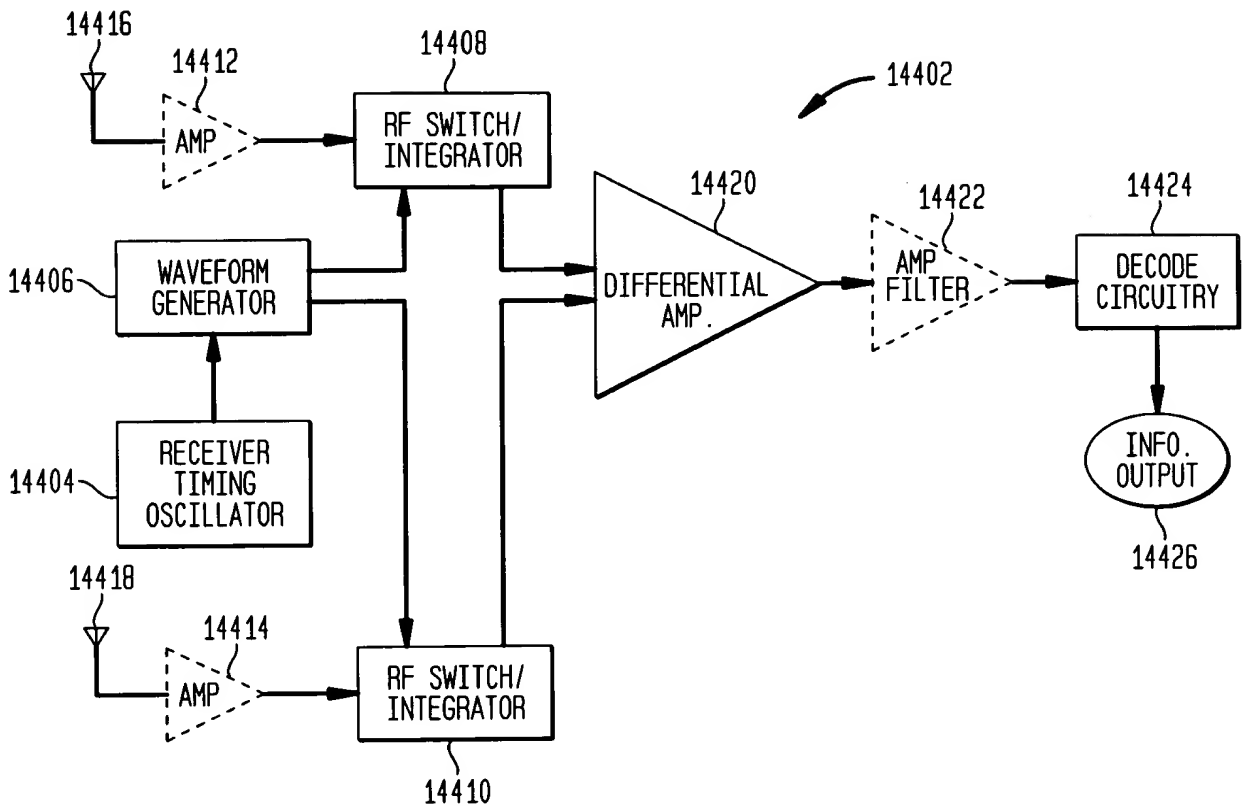
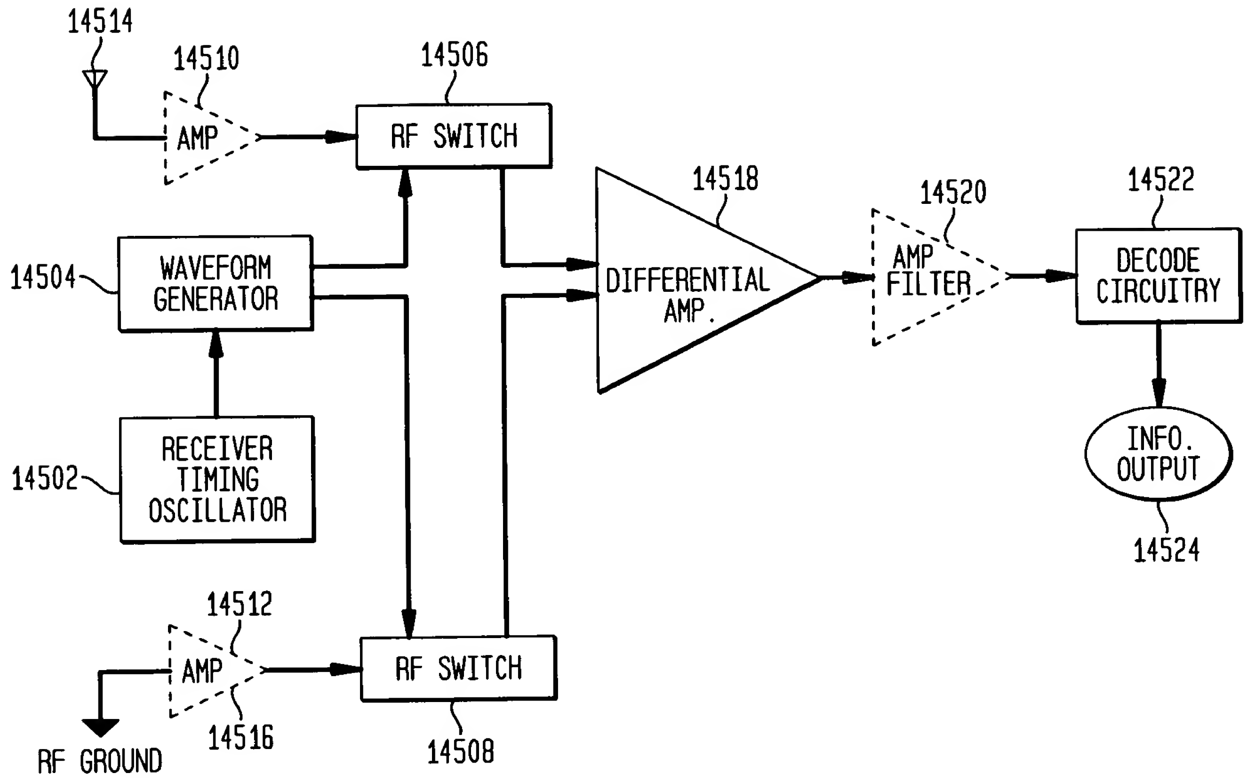


FIG. 145

PSEUDO DIFFERENTIAL RECEIVER



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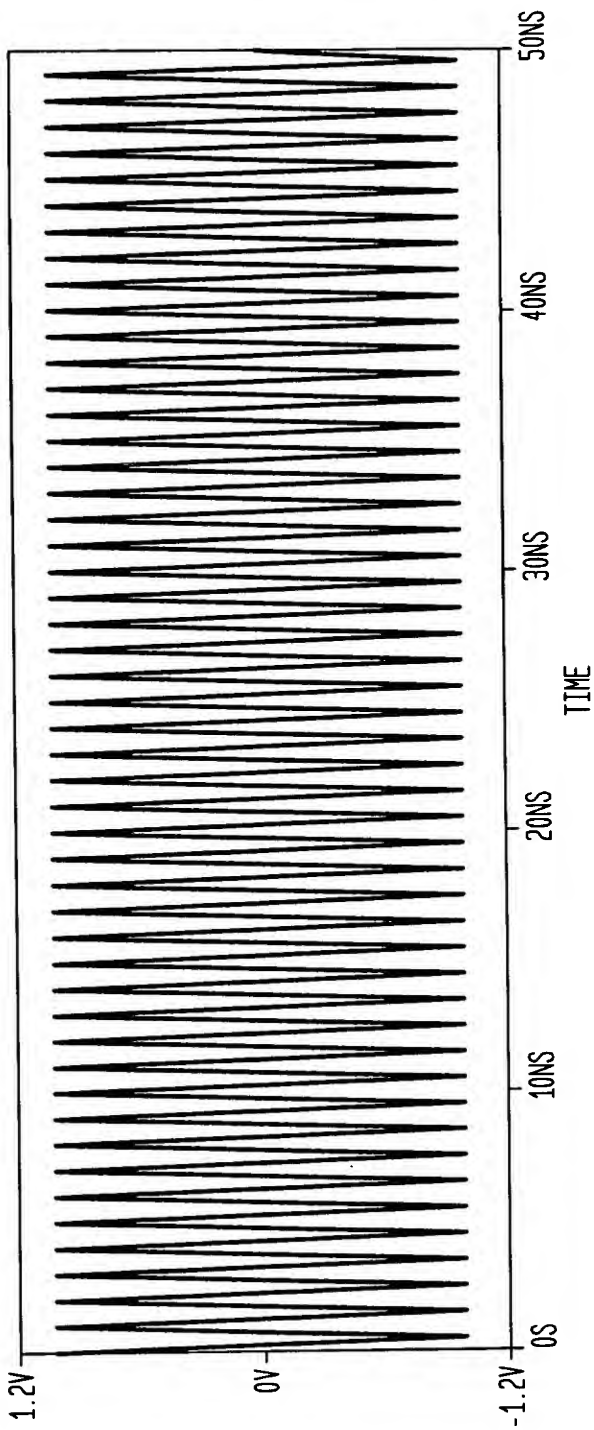

FIG. 146

(WAVEFORM GENERATOR OUTPUT)

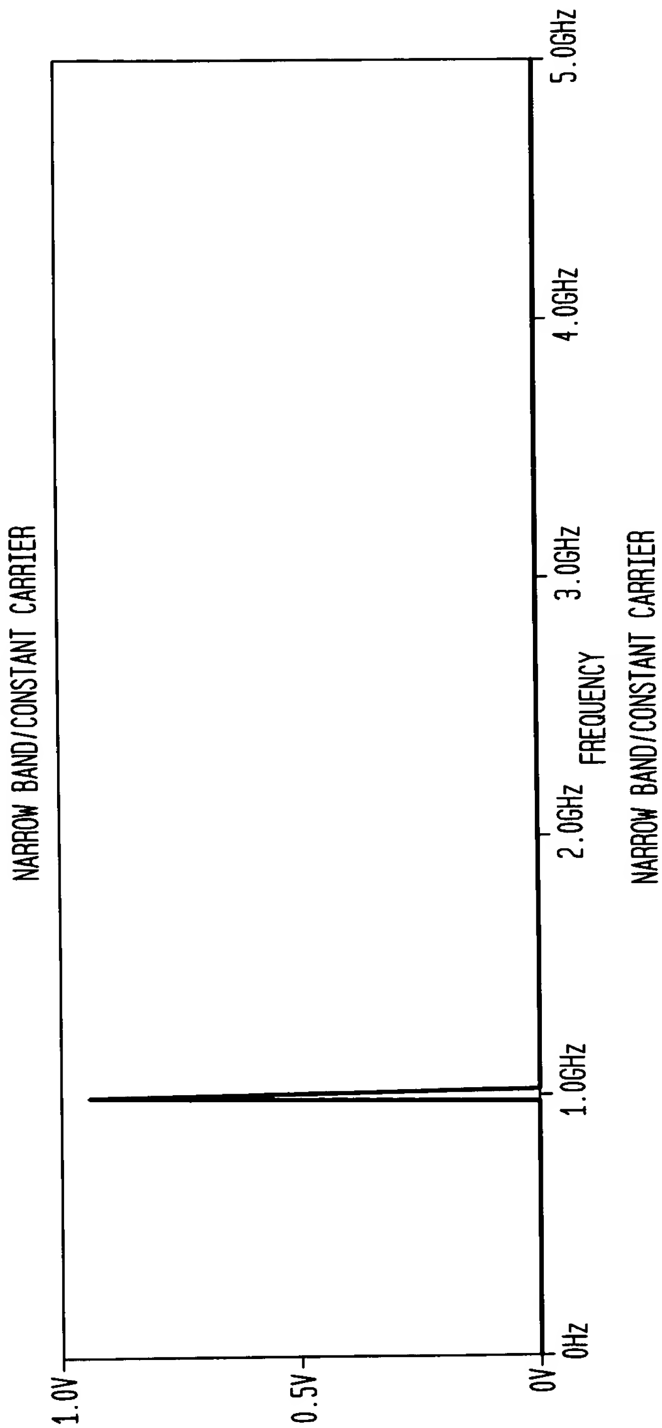

FIG. 147

(WAVEFORM GENERATOR OUTPUT)

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FIG. 148

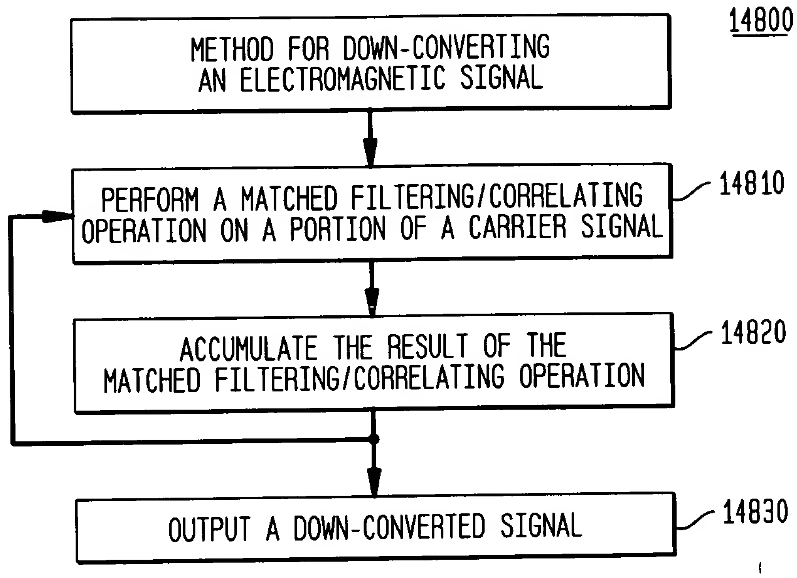

FIG. 149

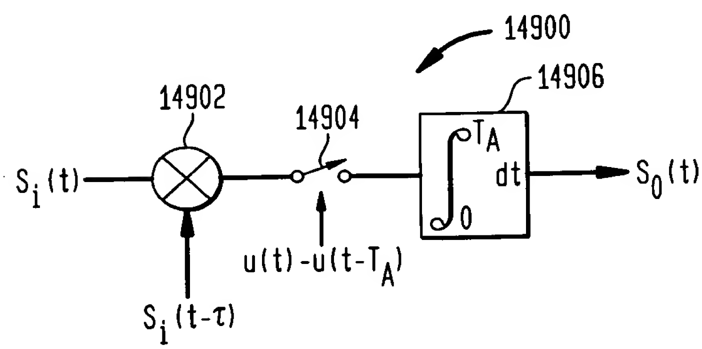

FIG. 150

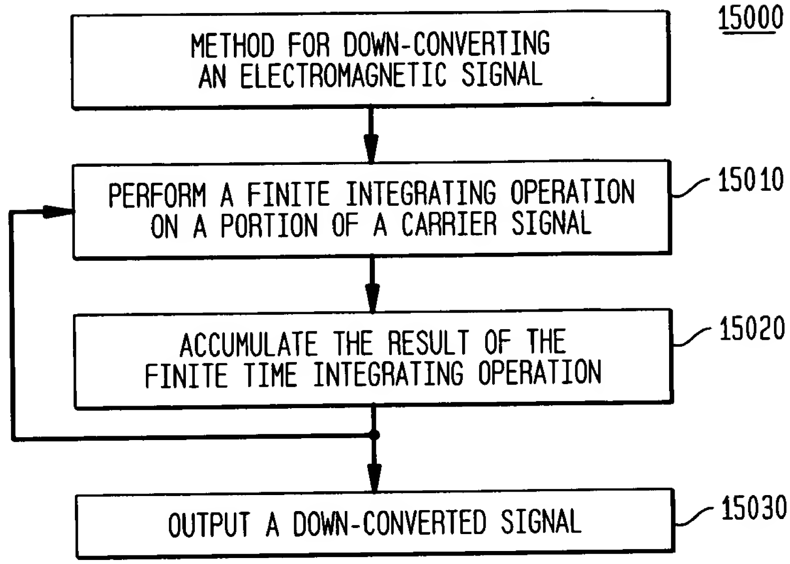

FIG. 151

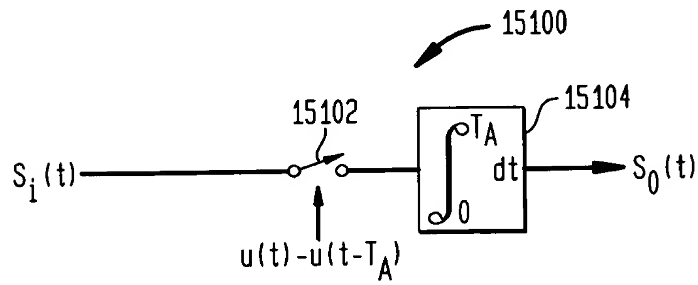

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FIG. 152

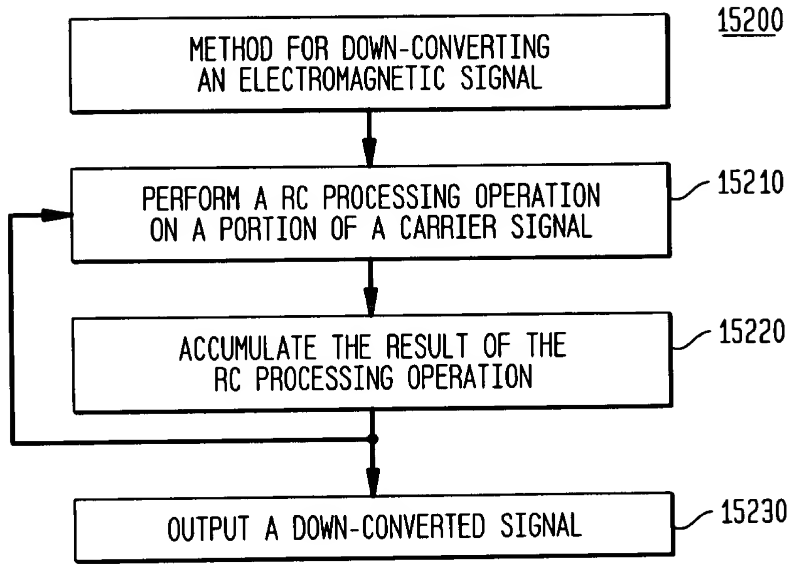

FIG. 153

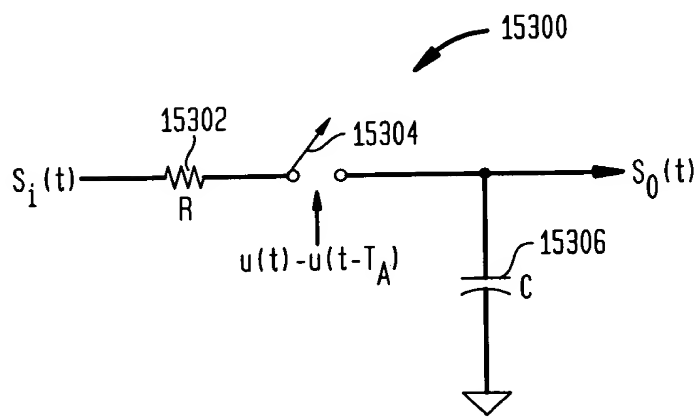

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FIG. 154

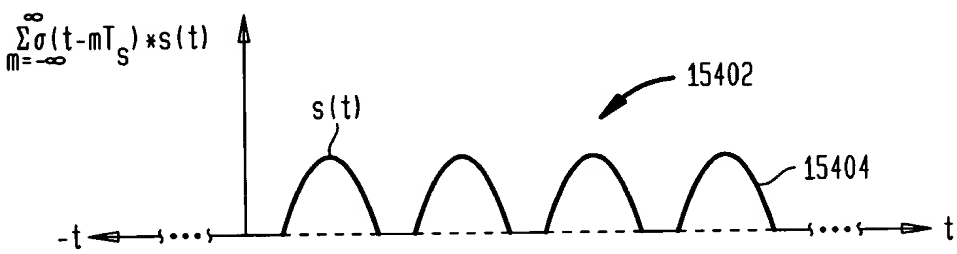


FIG. 155

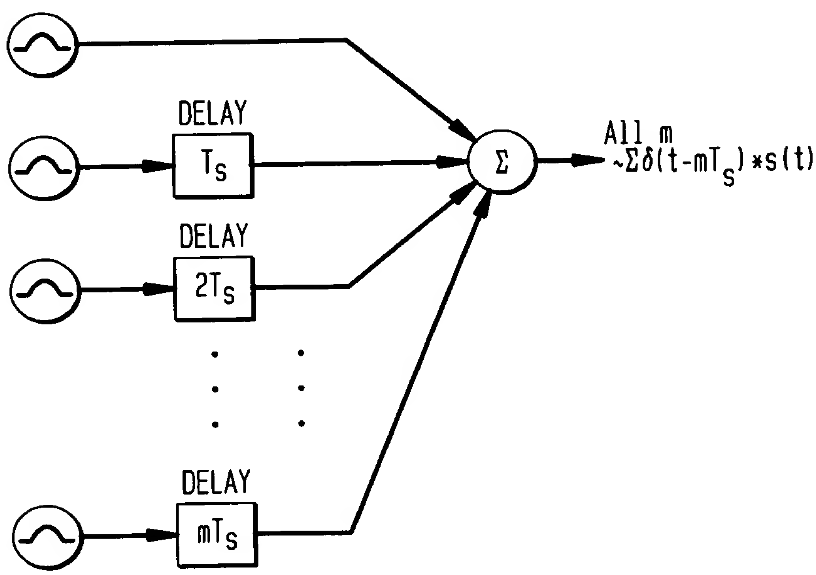


FIG. 156

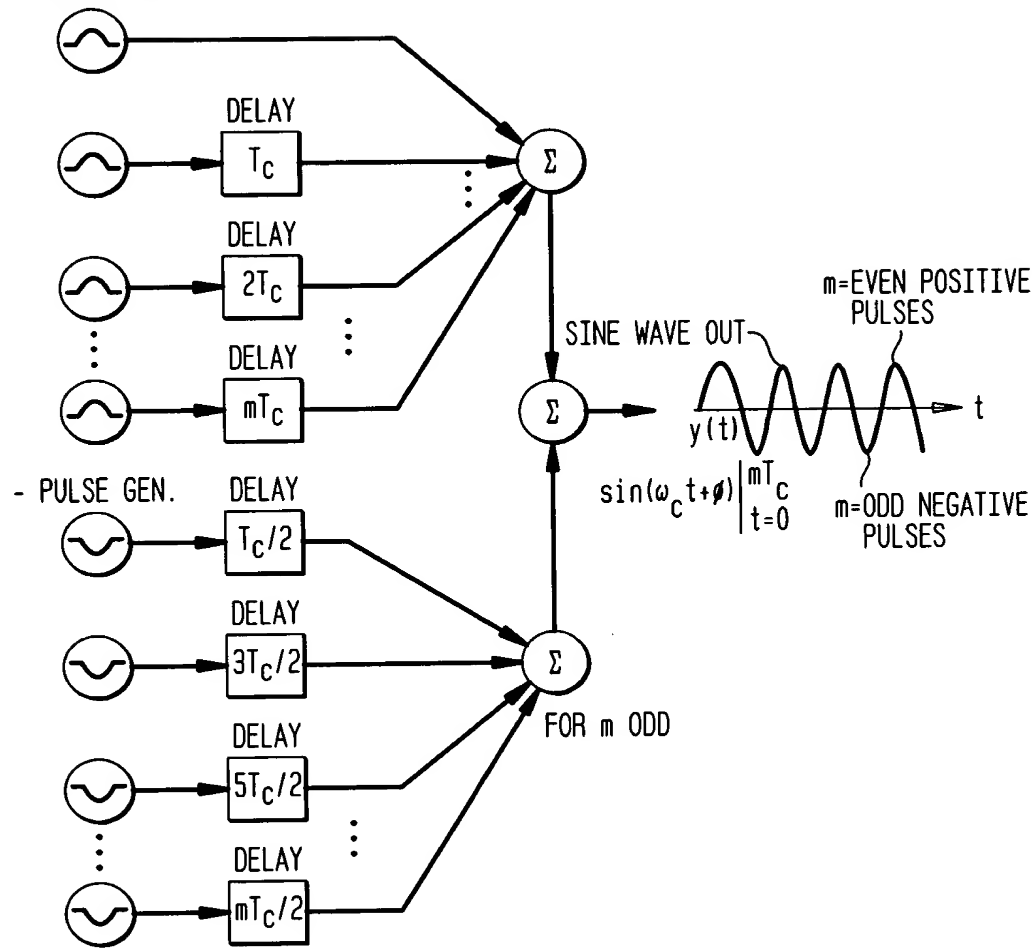
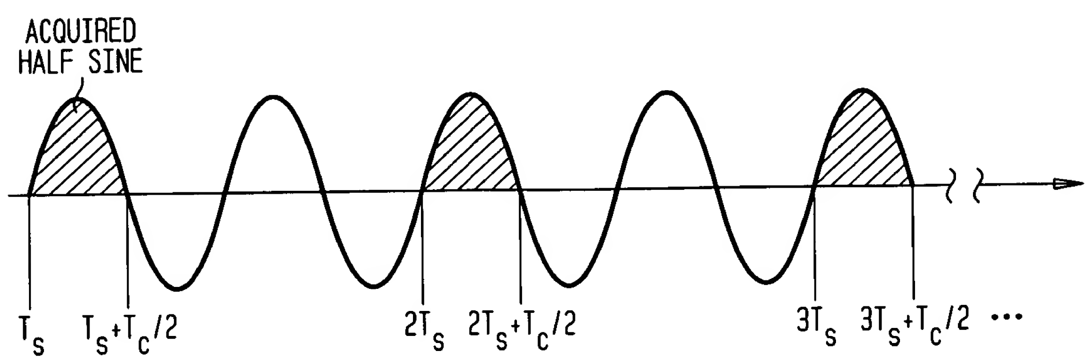


FIG. 157



CARRIER PROCESSED BY 3RD HARMONIC UFT PROCESSOR

FIG. 158

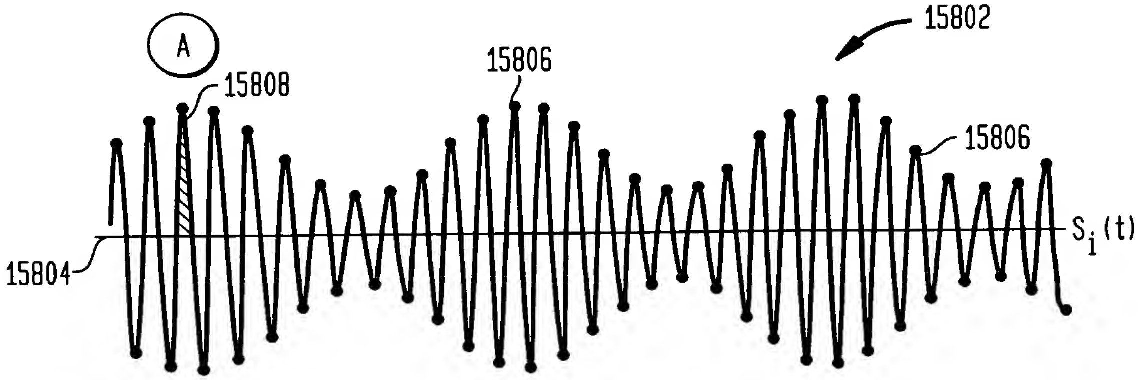


FIG. 159

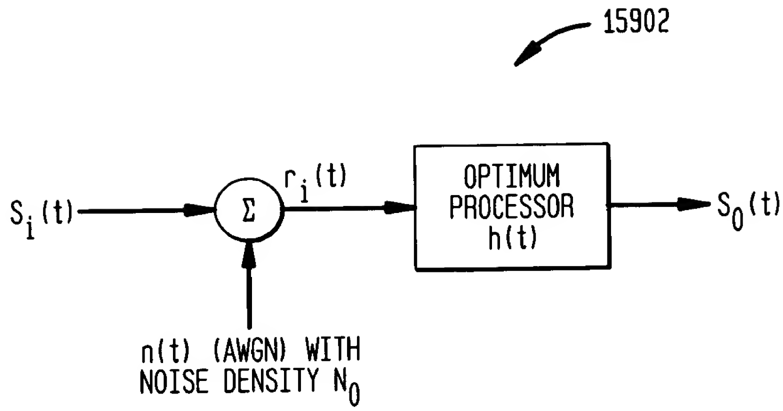
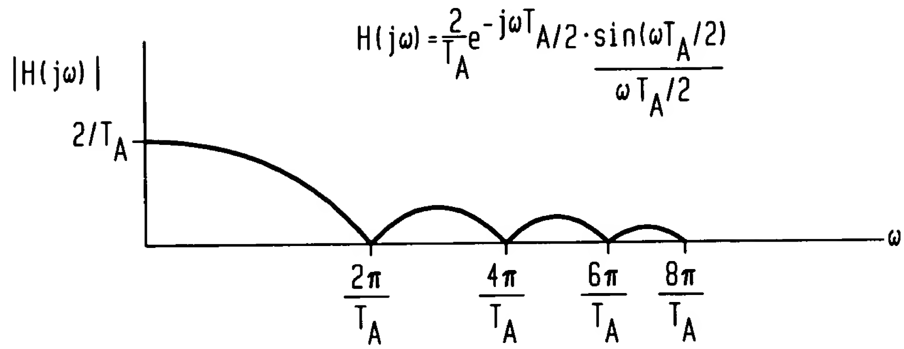
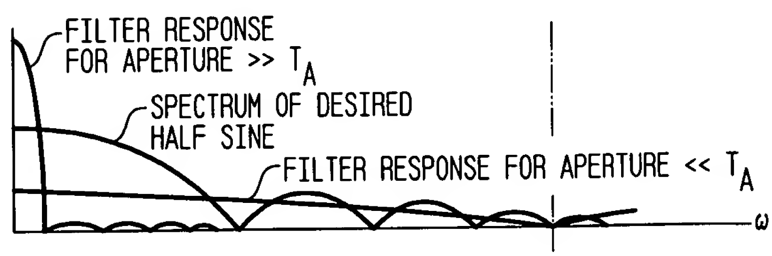


FIG. 160



MAG FREQUENCY RESPONSE OF SAMPLING APERTURE WAVEFORM

FIG. 161



APERTURE FREQUENCY DOMAIN REPRESENTATION

FIG. 162

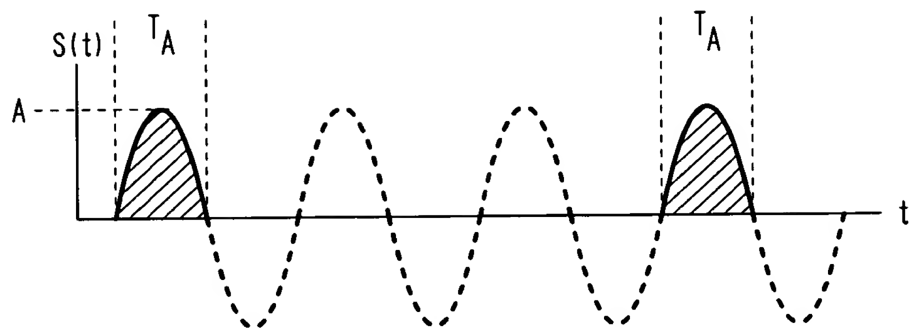


FIG. 163

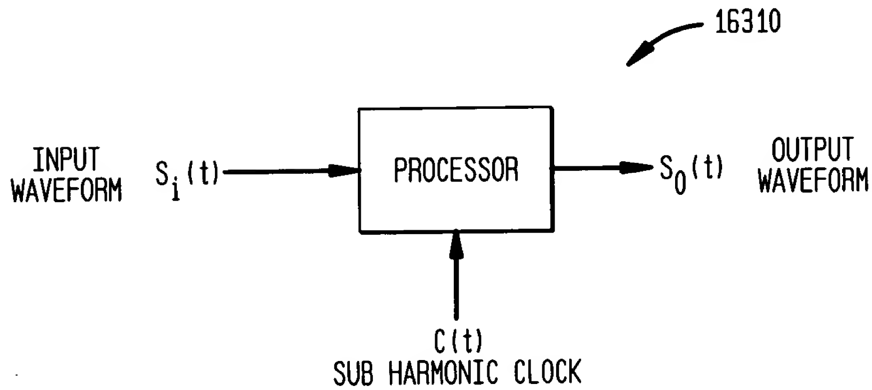


FIG. 164A

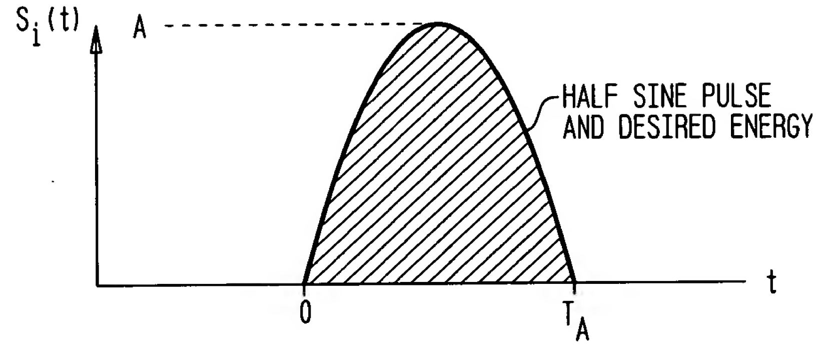


FIG. 164B

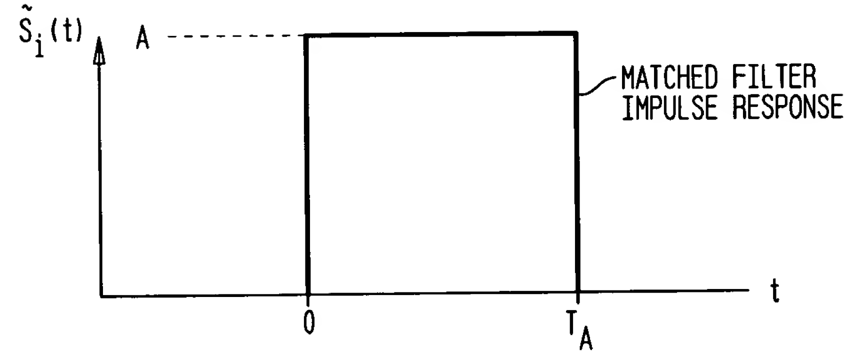


FIG. 164C

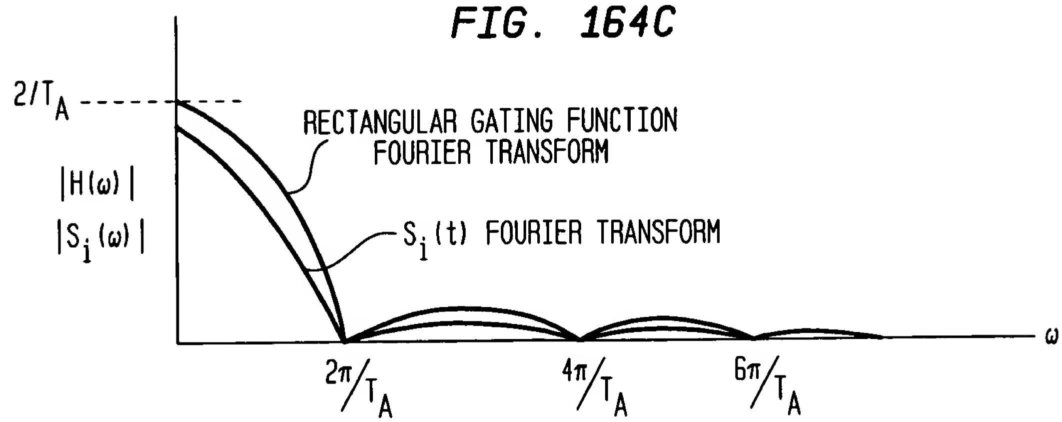


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FIG. 165

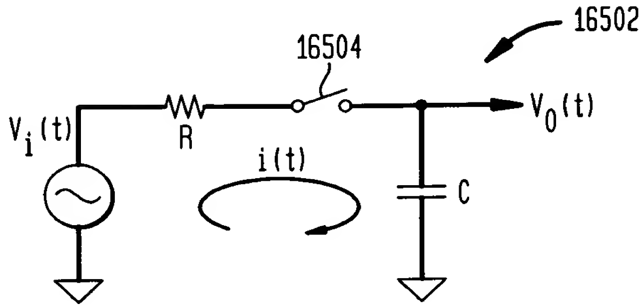

FIG. 166

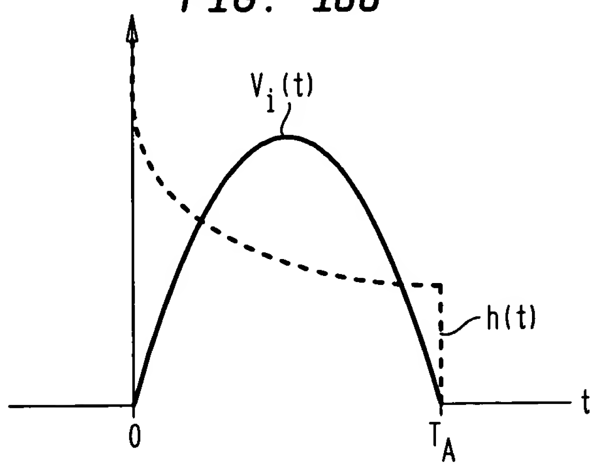

FIG. 167

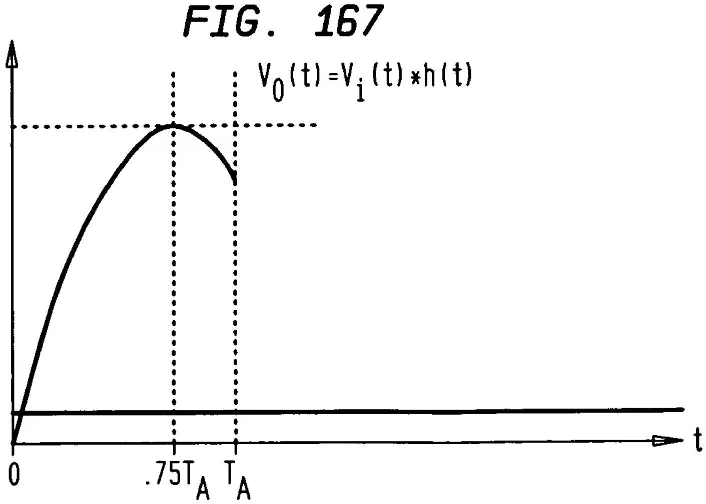

FIG. 168

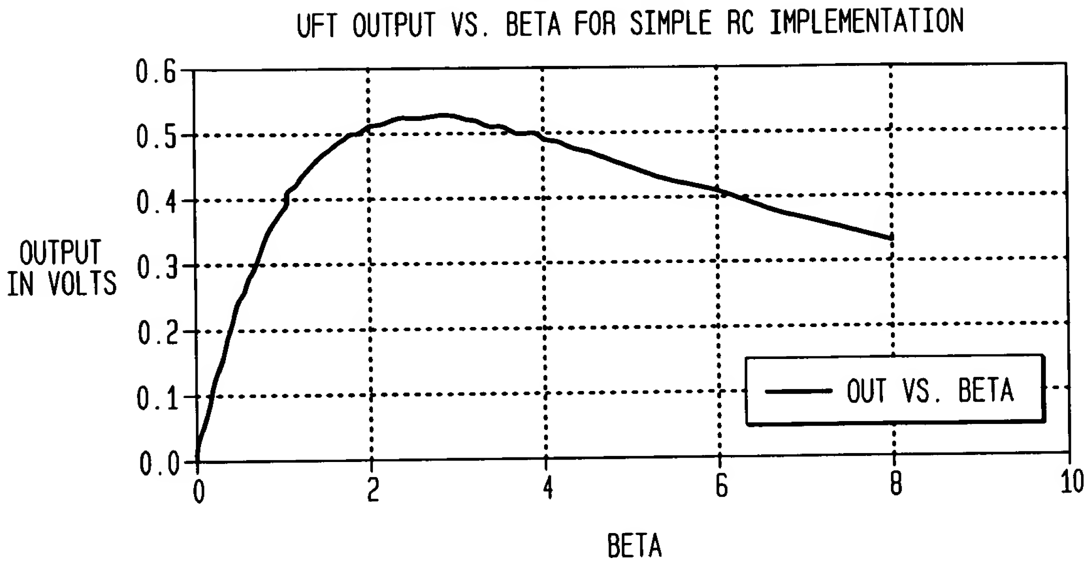

FIG. 169

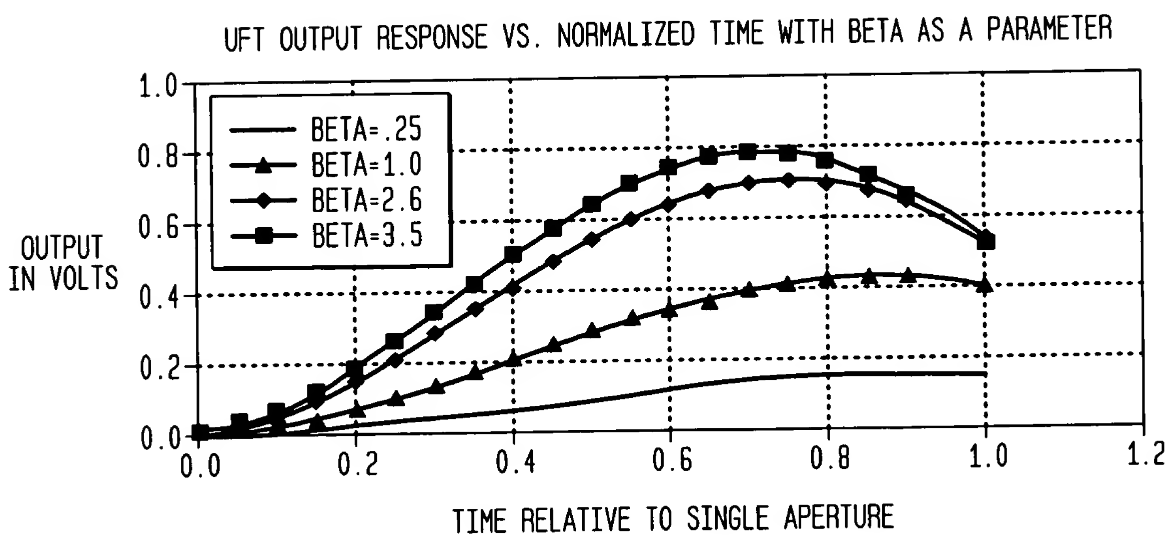

FIG. 170

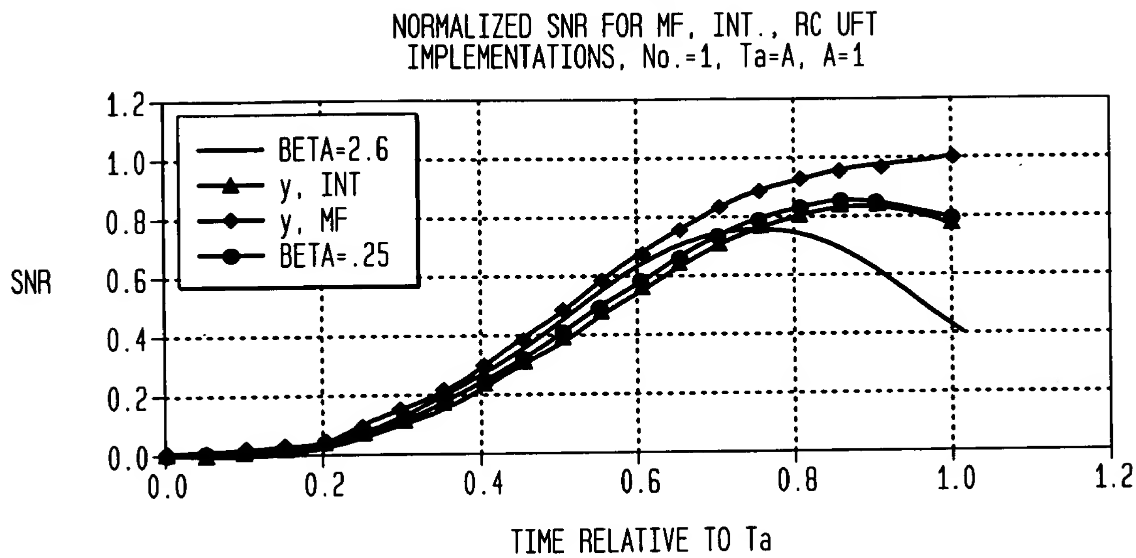

FIG. 171

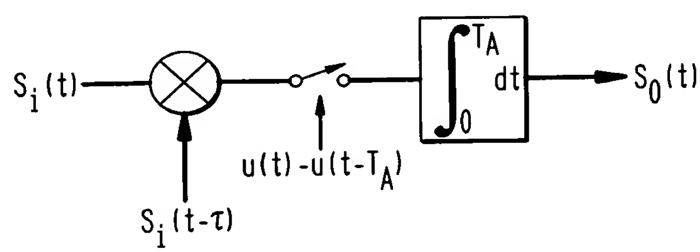

FIG. 172

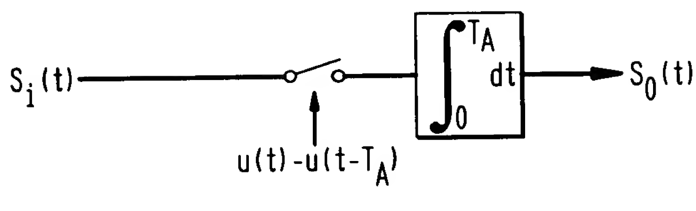

FIG. 173

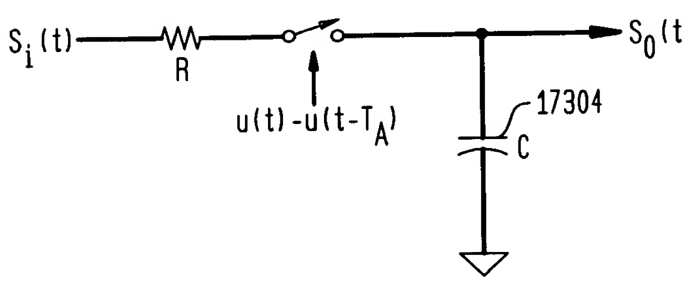

FIG. 174

UFT OUTPUT CHARGE TRANSFER

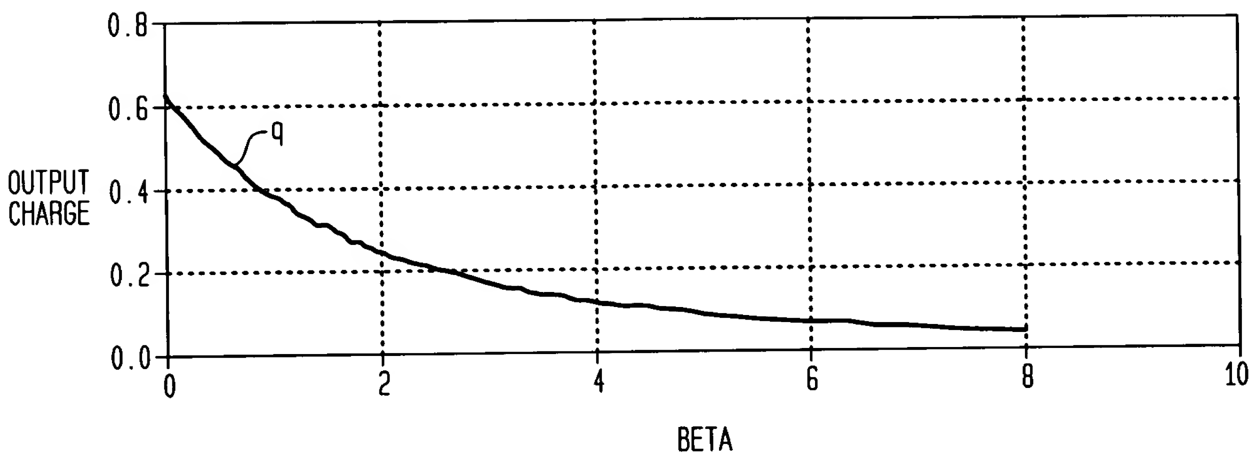

FIG. 175A

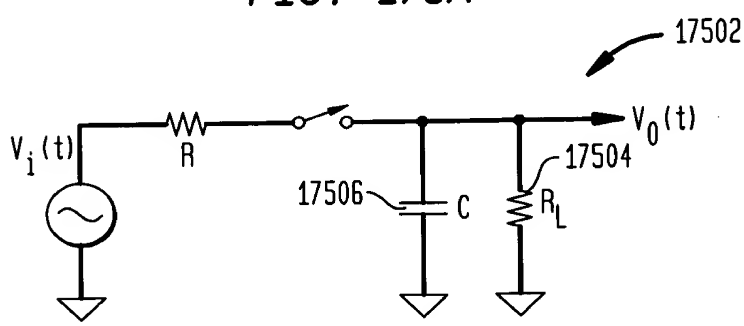

FIG. 175B

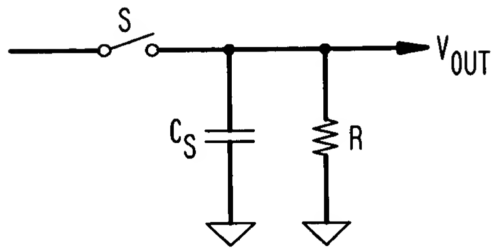

FIG. 175C

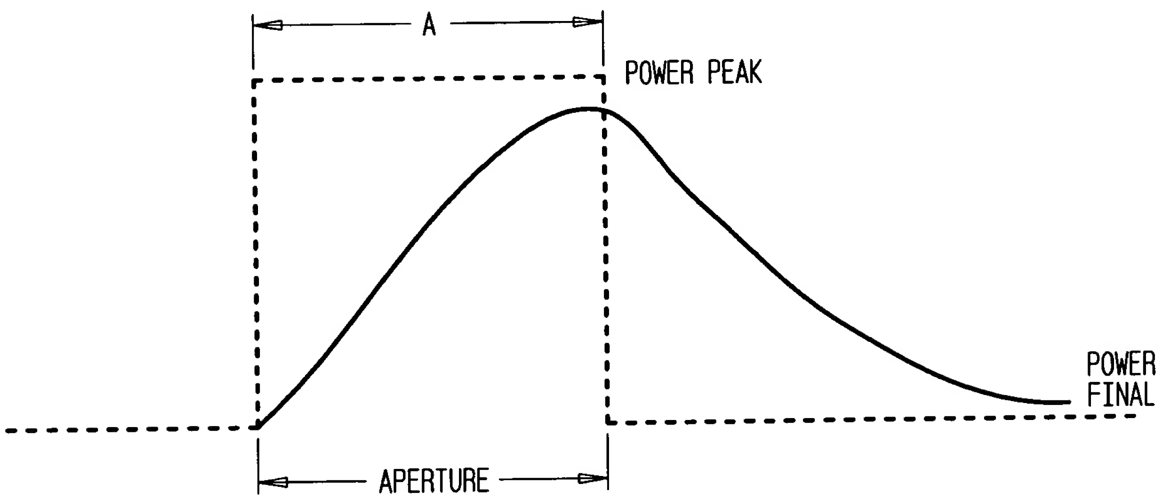

FIG. 175D

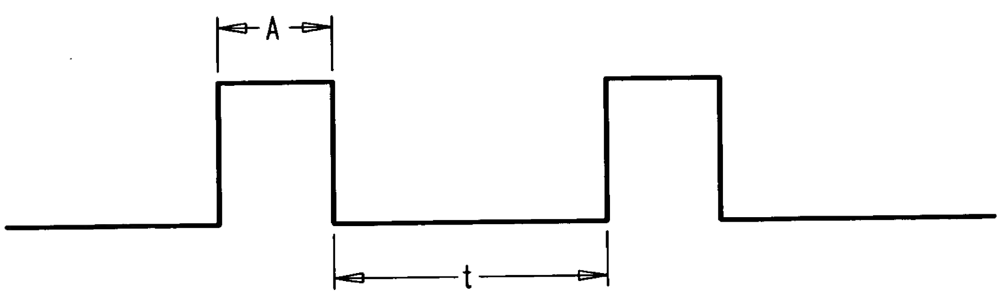

FIG. 176

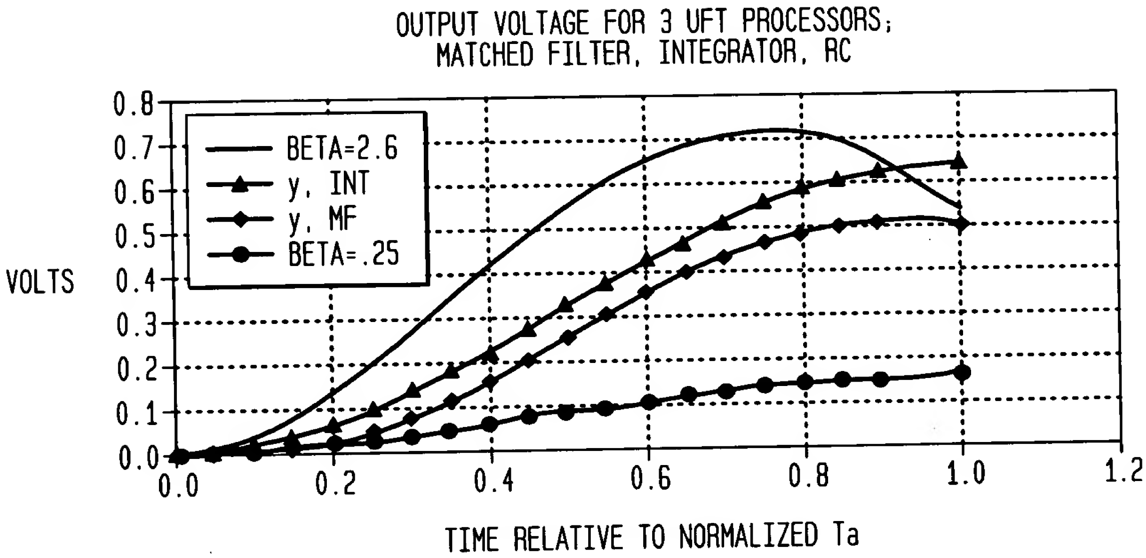
OUTPUT VOLTAGE FOR 3 UFT PROCESSORS;
MATCHED FILTER, INTEGRATOR, RC
BETA=2.6
y, INT
y, MF
BETA=.25
VOLTS
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.0
0.2
0.4
0.6
0.8
1.0
1.2
TIME RELATIVE TO NORMALIZED Ta

FIG. 177A

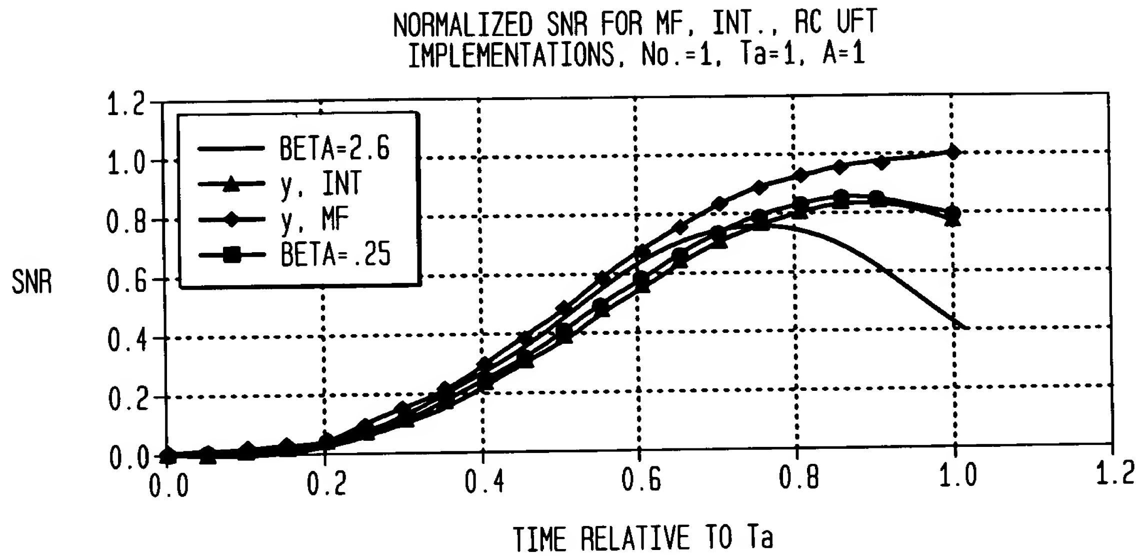
NORMALIZED SNR FOR MF, INT., RC UFT
IMPLEMENTATIONS, No.=1, Ta=1, A=1
BETA=2.6
y, INT
y, MF
BETA=.25
SNR
1.2
1.0
0.8
0.6
0.4
0.2
0.0
0.0
0.2
0.4
0.6
0.8
1.0
1.2
TIME RELATIVE TO Ta

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FIG. 177B

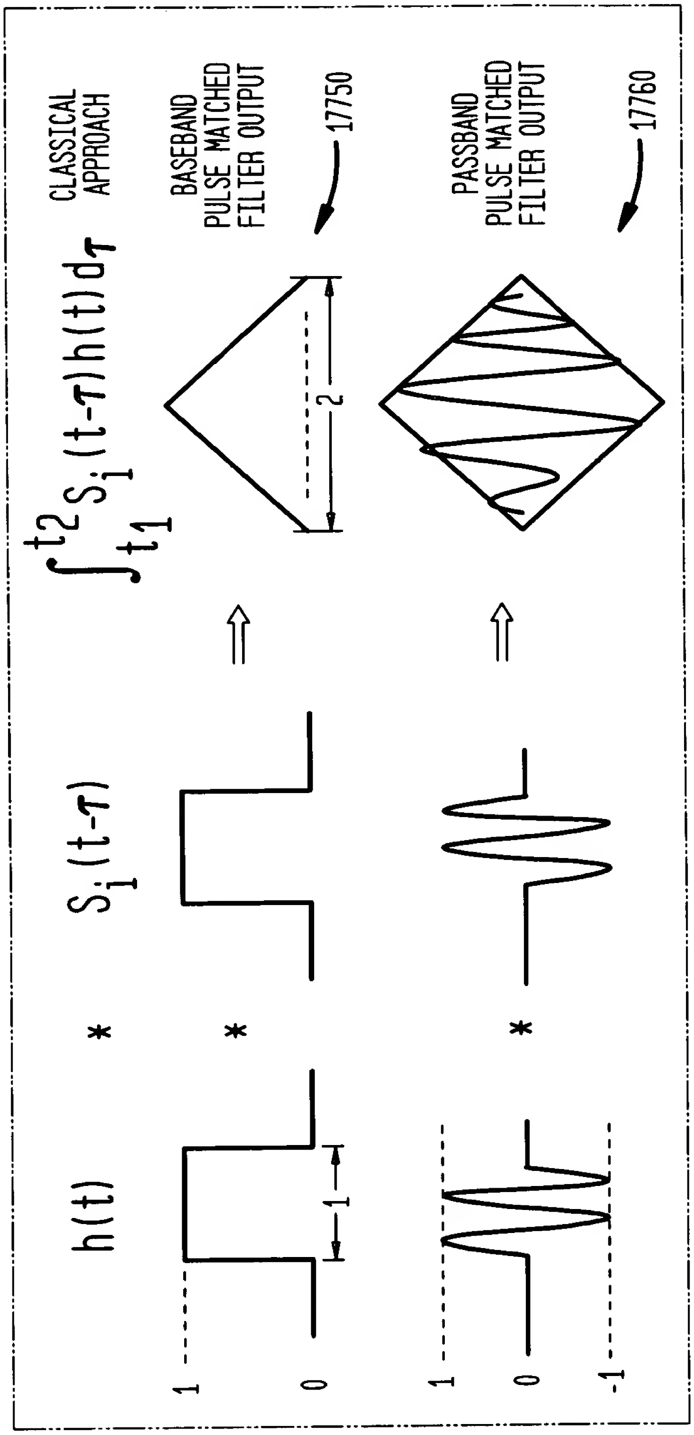


FIG. 177C

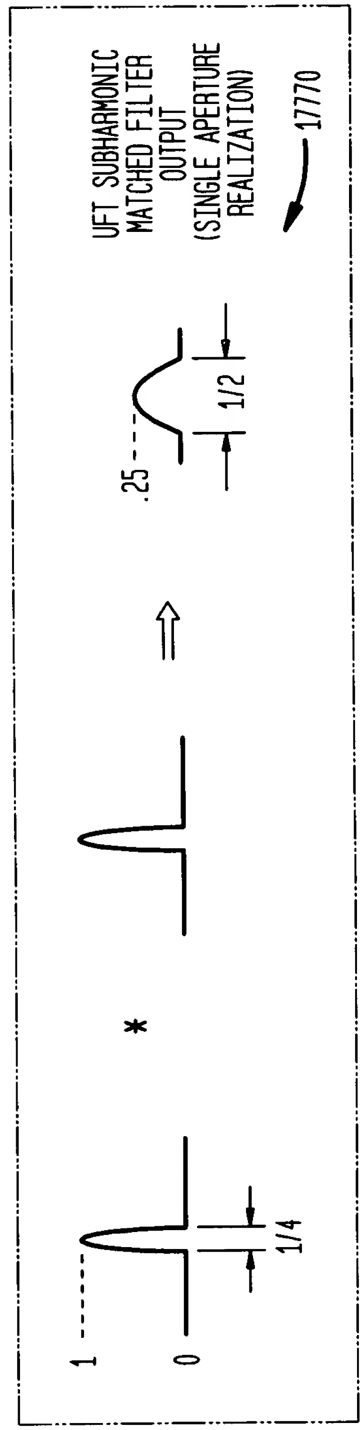


FIG. 177D

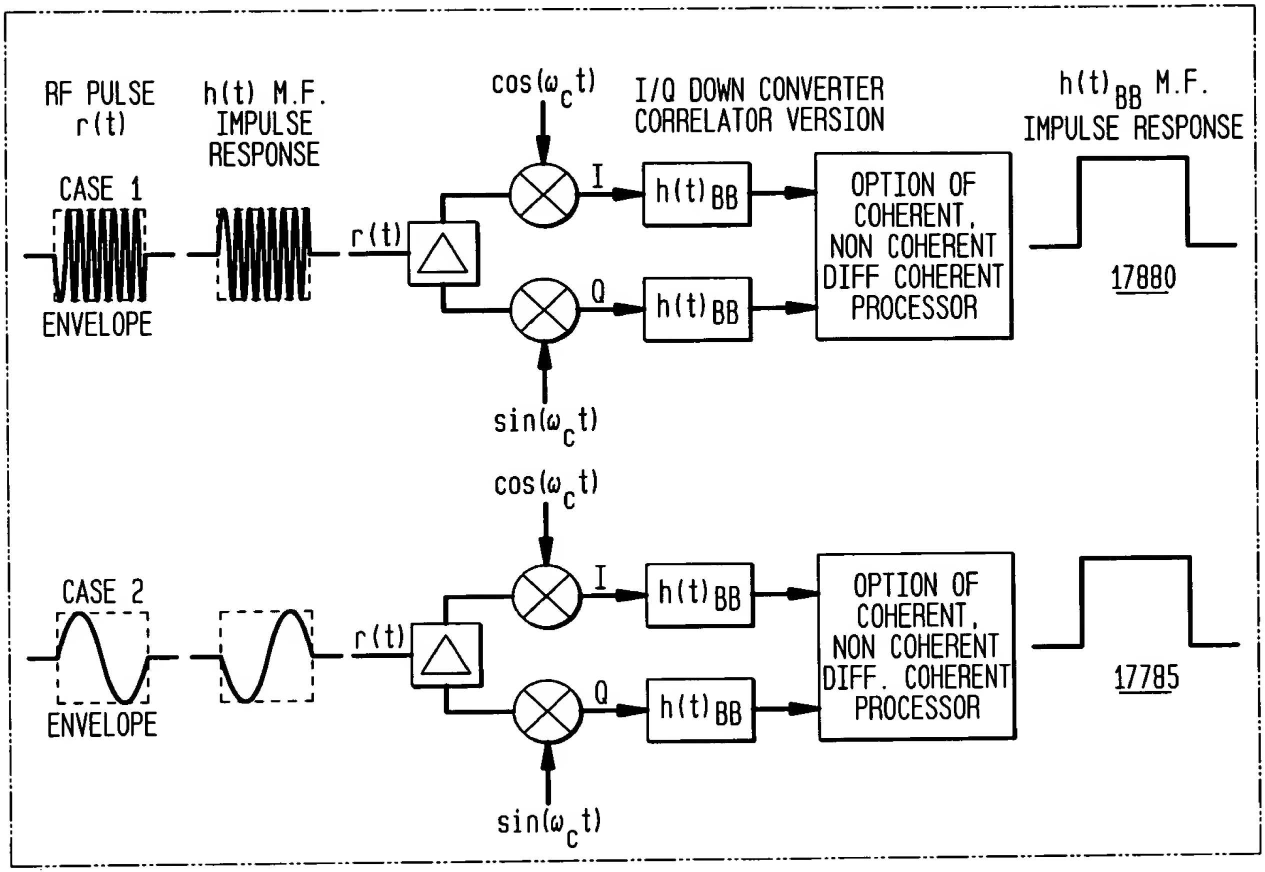


FIG. 177E

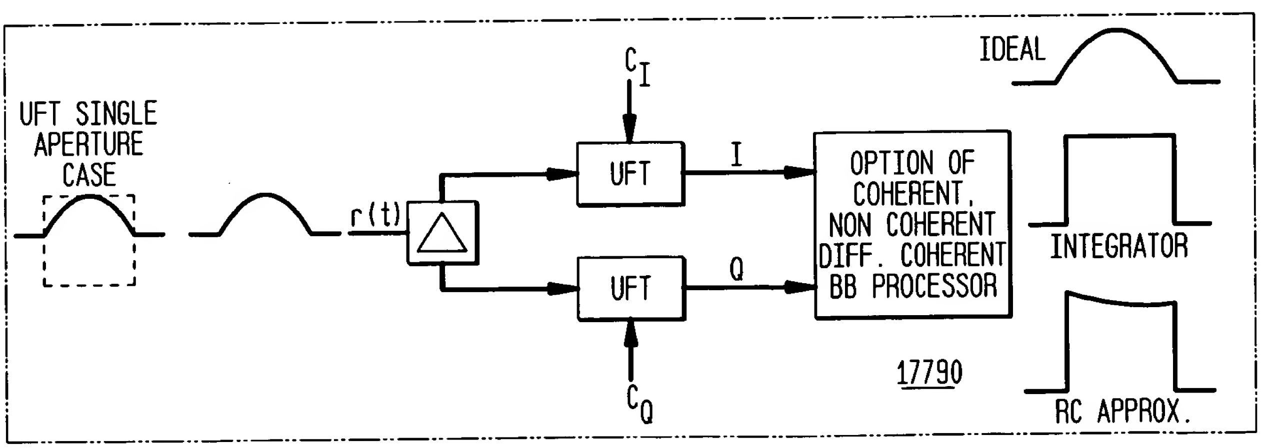
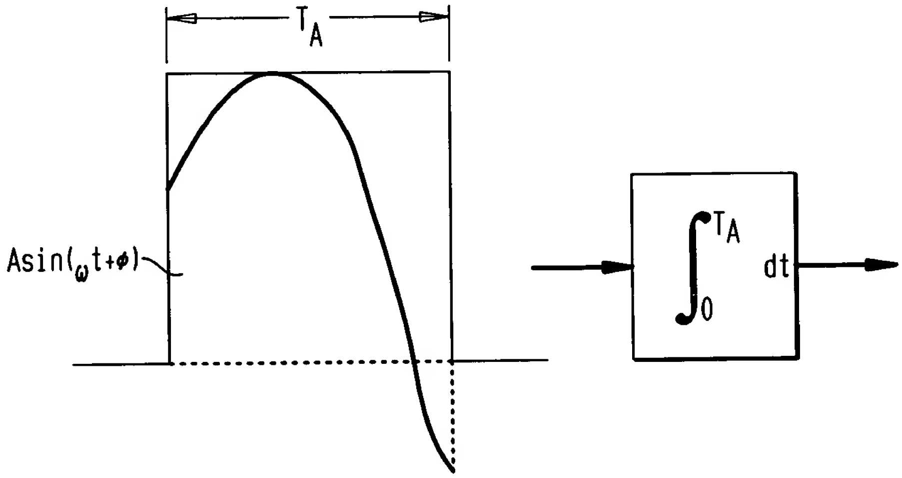


FIG. 177F



$$\int_0^{T_A} Au(t-T_A)\sin(\omega t+\phi)\,dt=\int_0^{T_A} A\left(u(t-T_A)\cos\phi\sin(\omega t)+u(t-T_A)\sin\phi\cos(\omega t)\right)dt$$

$$=\underbrace{A\cos(\phi)}_{\text{CONSTANT}}\underbrace{\int_0^{T_A} u(t-T_A)\sin(\omega t)\,dt}_{\text{UFT CORRELATOR KERNEL}}+\underbrace{A\sin(\phi)}_{\text{CONSTANT}}\underbrace{\int_0^{T_A} u(t-T_A)\cos(\omega t)\,dt}_{=0}$$

$$=A\cos(\phi)\int_0^{T_A} u(t-T_A)\sin(\omega t)\,dt$$

- A IS CONSTANT ON A SINE TO SINE BASIS
- ϕ IS CONSTANT ON A SINE TO SINE BASIS
- i.e., THE MODULATION RATE DUE TO INFORMATION FOR PHASE AND AMPLITUDE IS VERY SLOW COMPARED TO CARRIER FREQUENCY

FIG. 178A

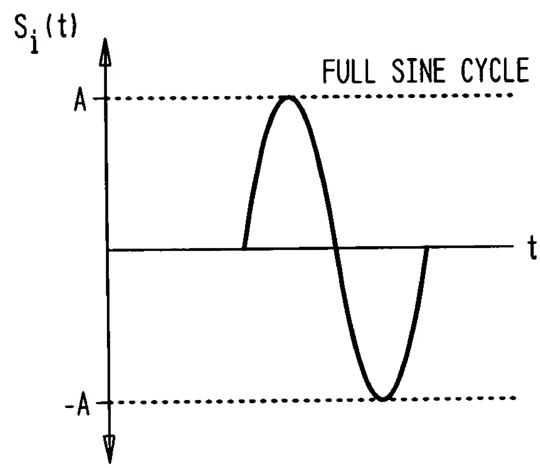


FIG. 178B

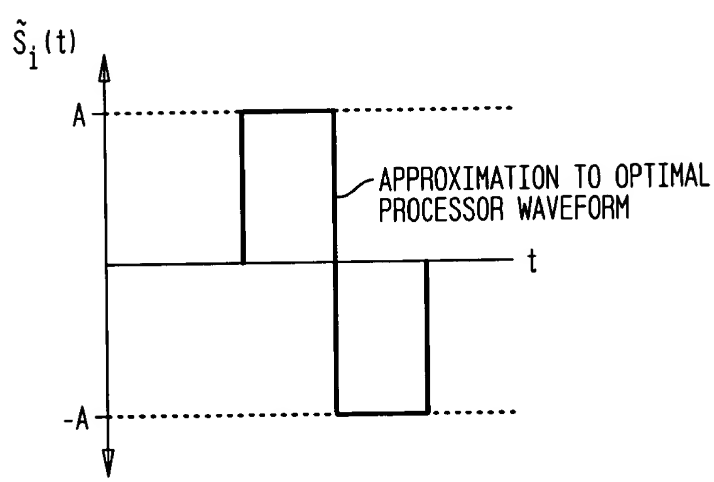


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FIG. 179

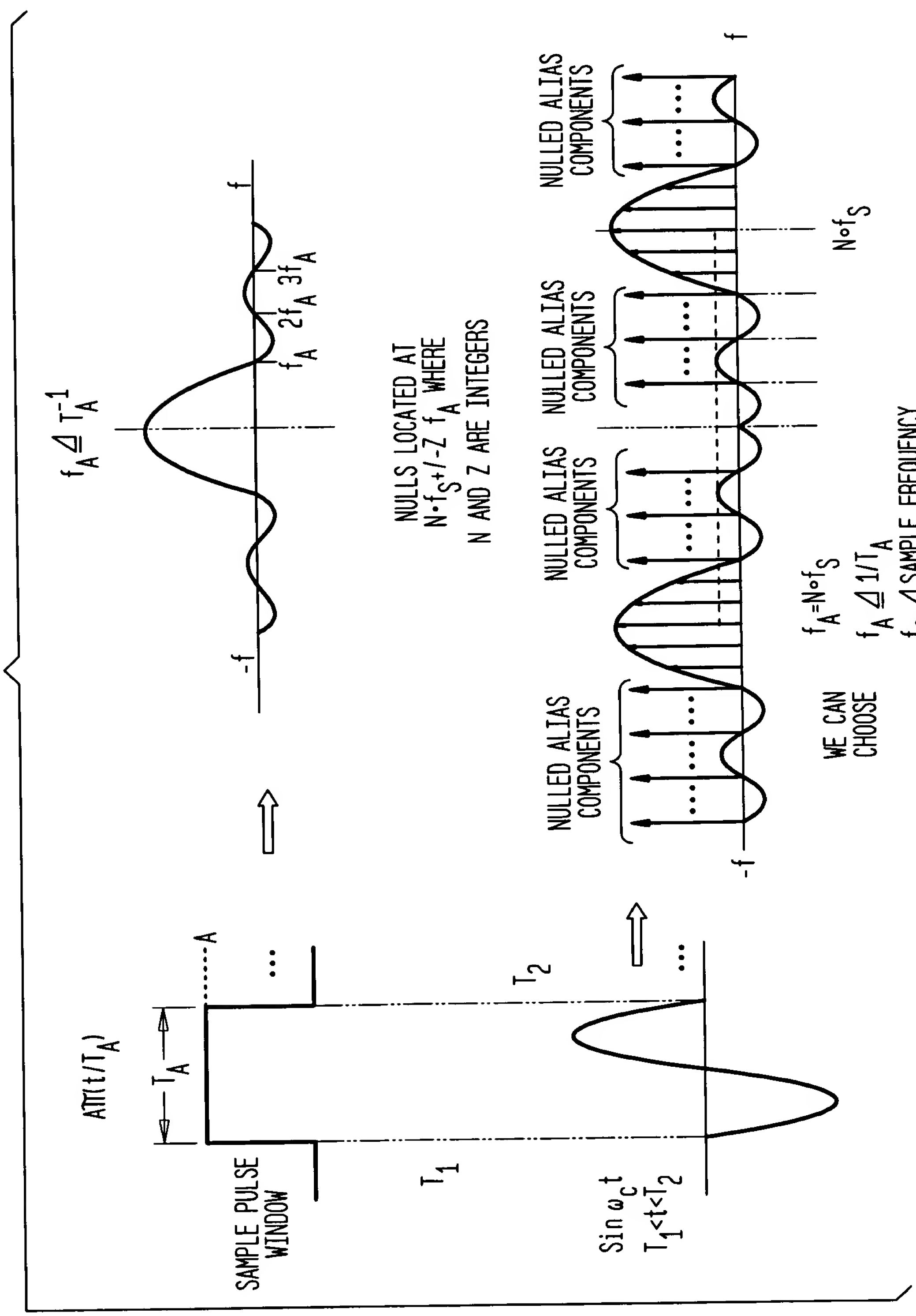

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FIG. 180

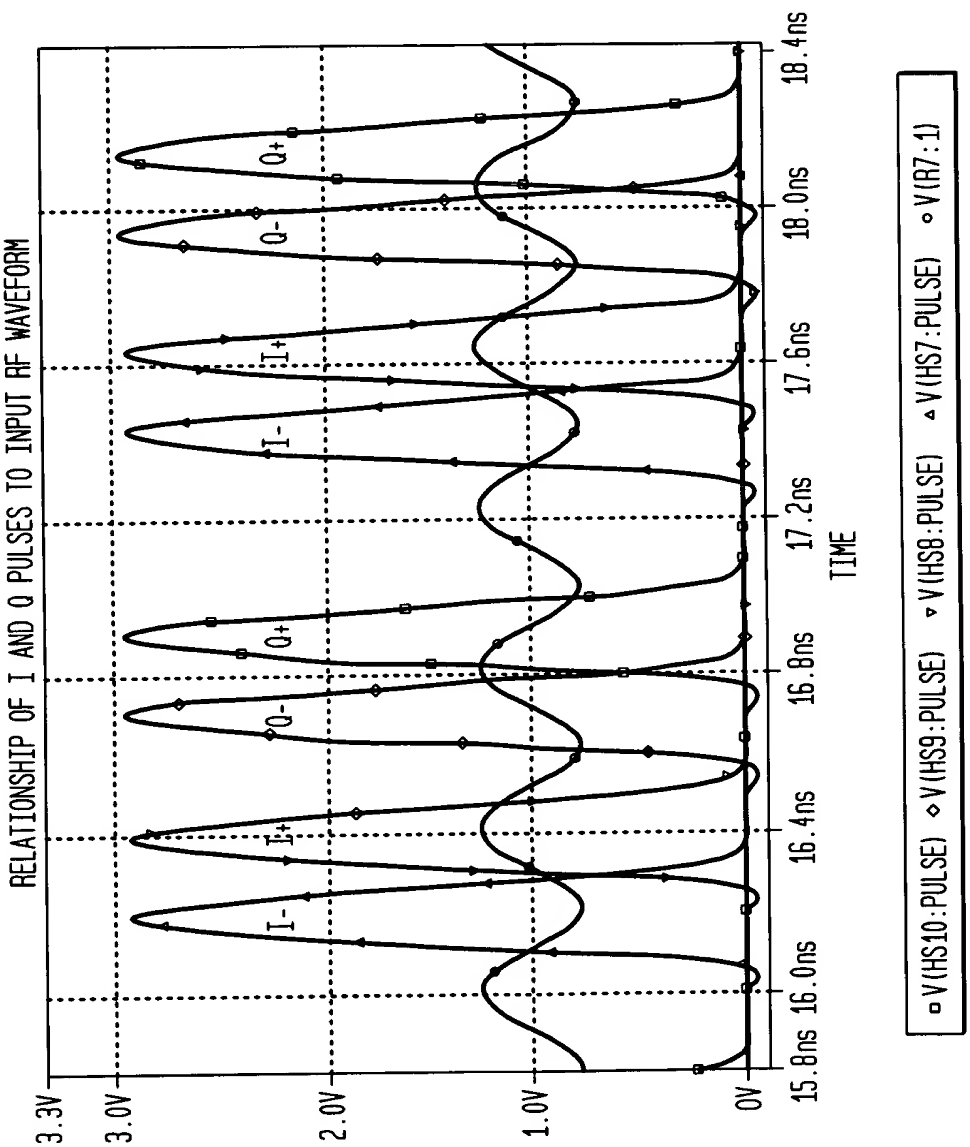

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FIG. 181

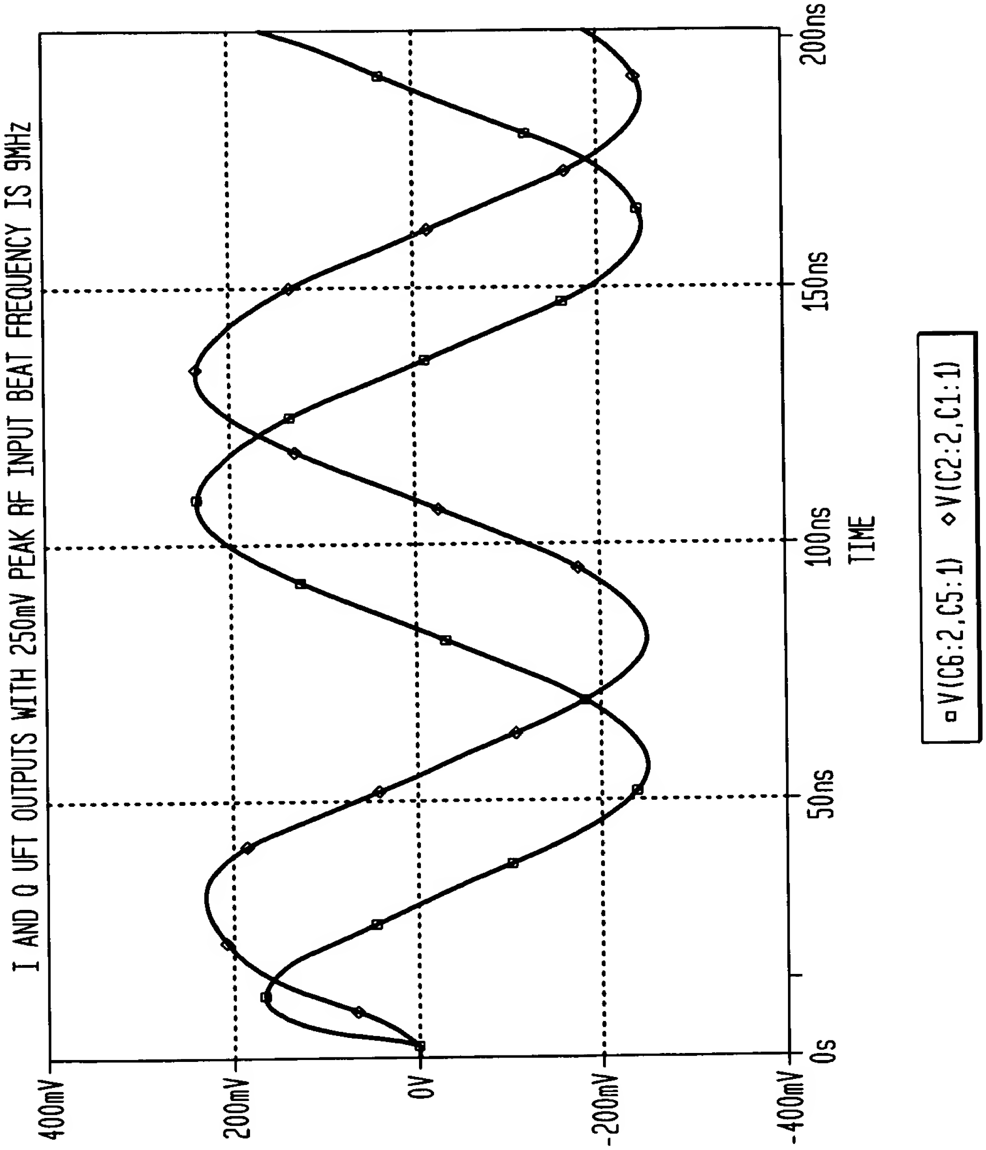

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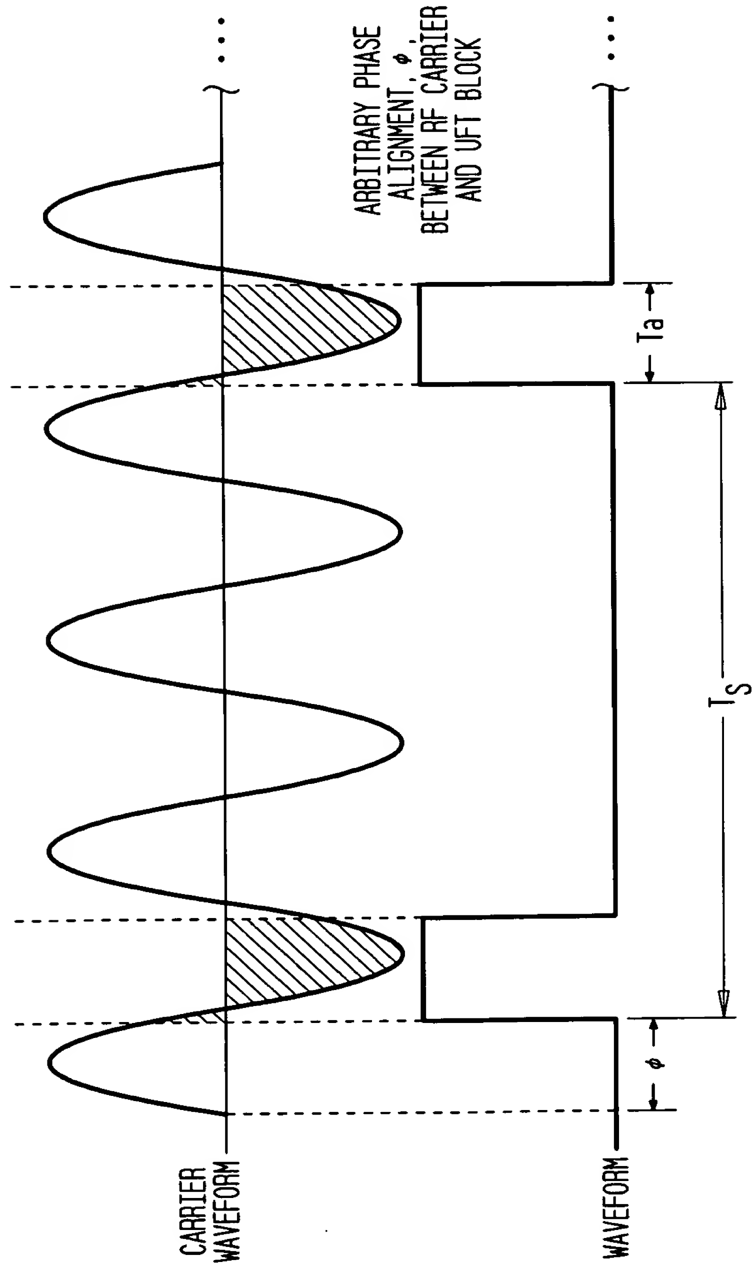
FIG. 182



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Inventors: SORRELLS et al.
Tel. No.: 202-371-2600
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FIG. 183

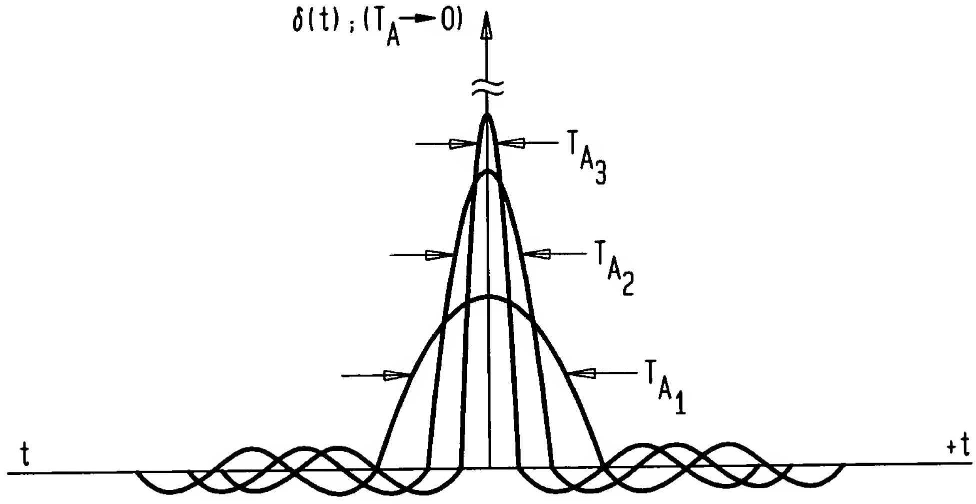

FIG. 184

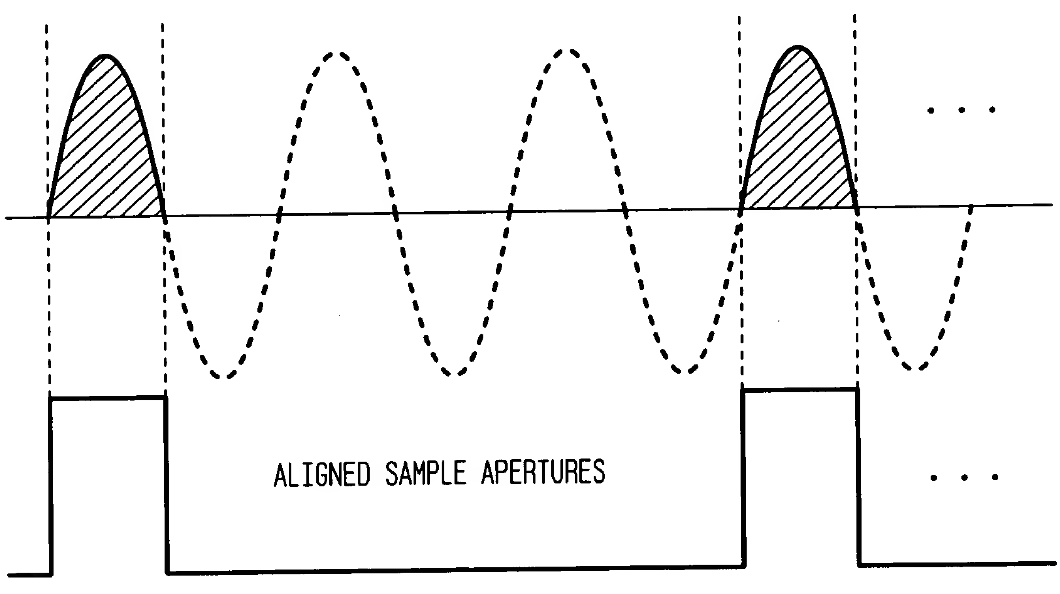

FIG. 185

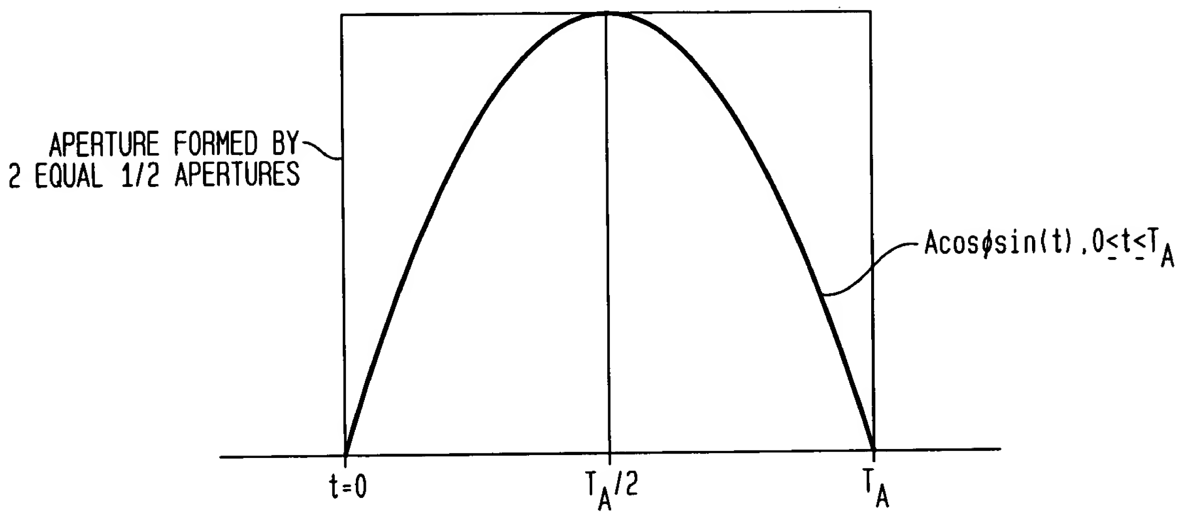

FIG. 186

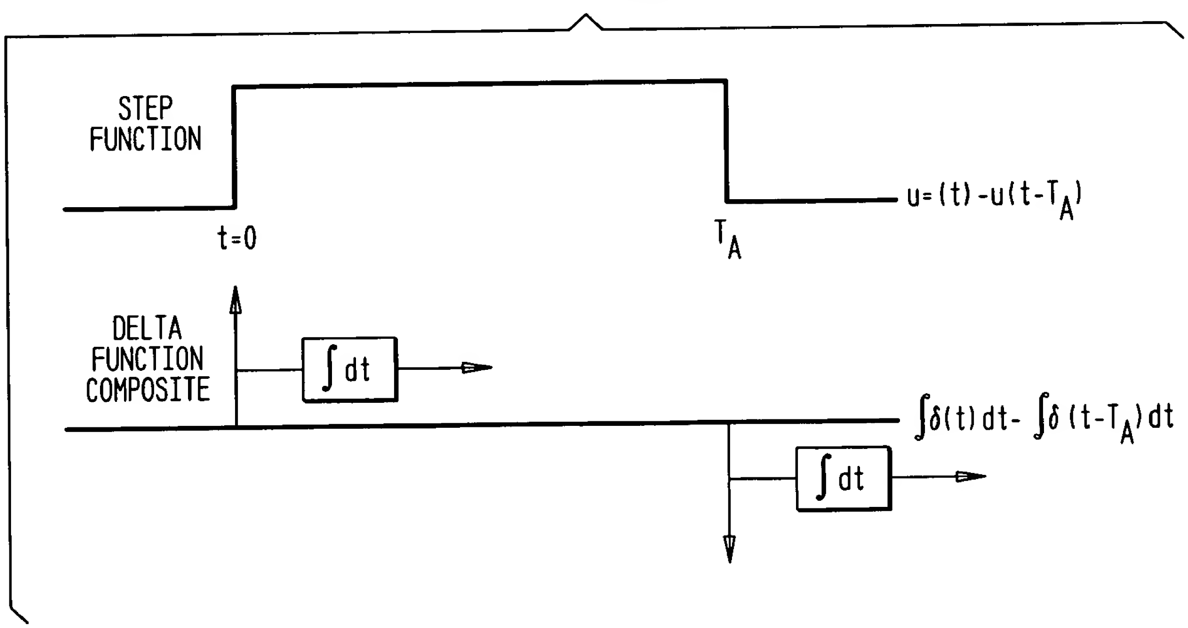

FIG. 187

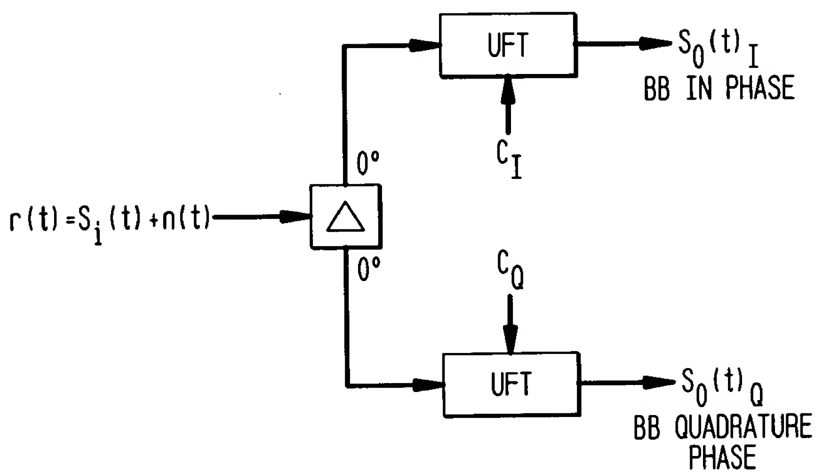

FIG. 188

$$C_I(t)=\sum_{m=-\infty}^{\infty}\delta(t-mT_S)*p_C(t)=\sum_{m=-\infty}^{\infty}p(t-mT_S)$$ 18802

$$C_I(t)=\sum_{m=-\infty}^{\infty}(u(t)-u(t-T_A))*\delta(t-mT_S)$$ 18804

$$C_Q(t)=\sum_{m=-\infty}^{\infty}(u[t-T_A/2]-u[t-3T_A/2])*\delta(t-(mT_S+T_A/2))$$ 18806

FIG. 189

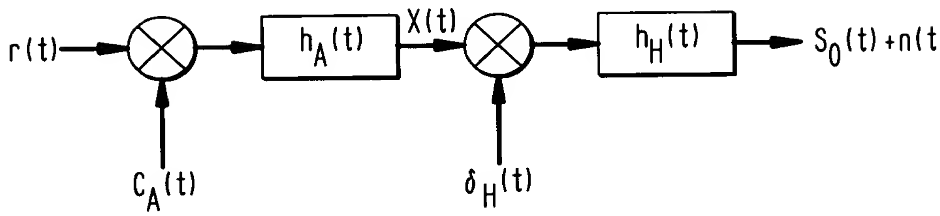

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FIG. 190

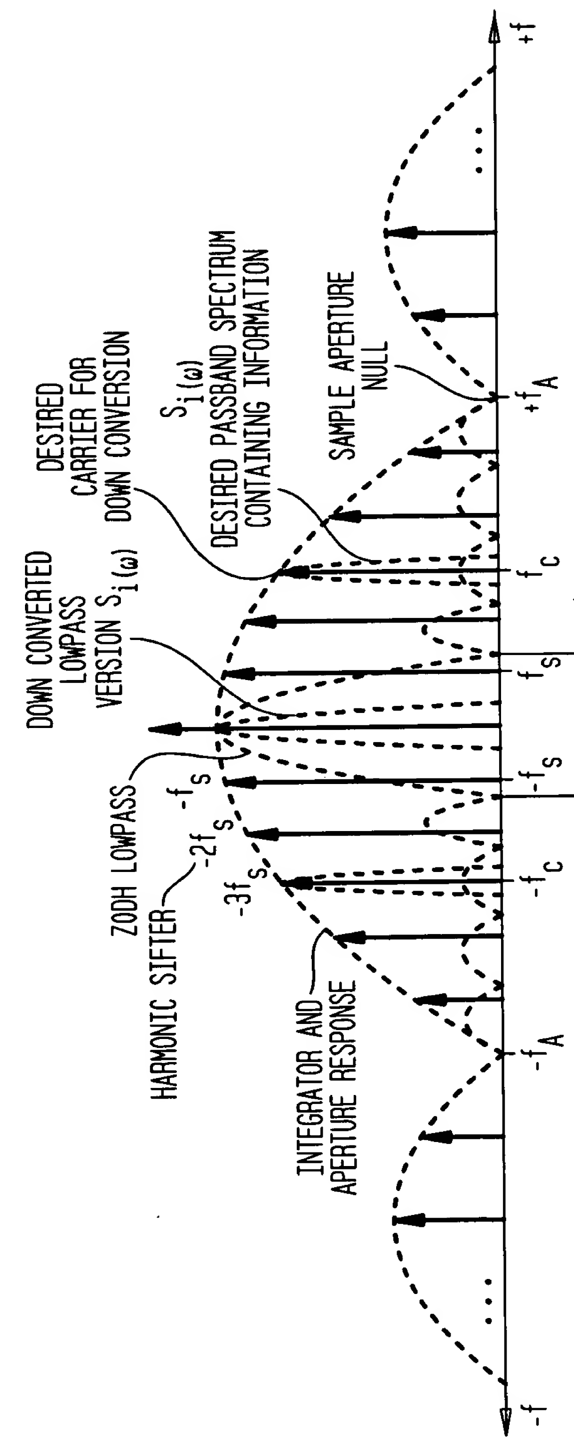

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FIG. 191

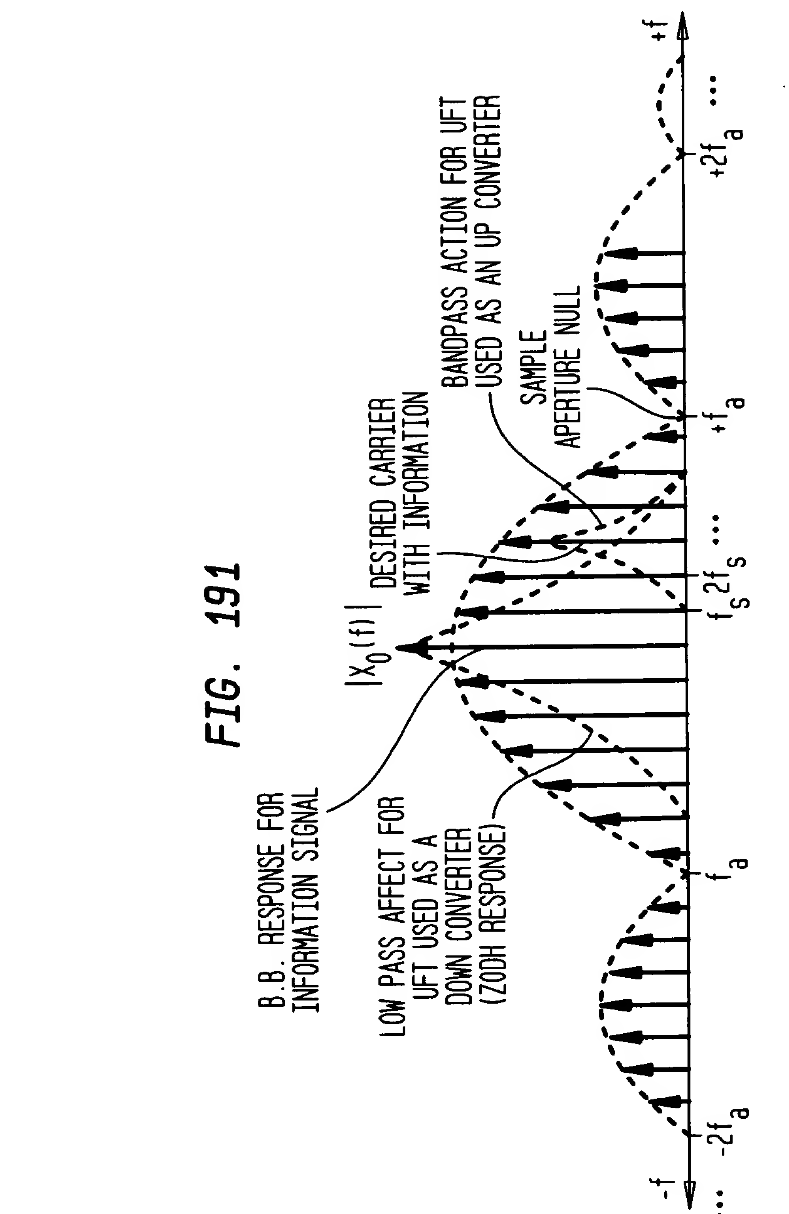

FIG. 192

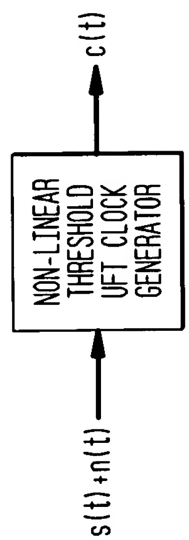

FIG. 193

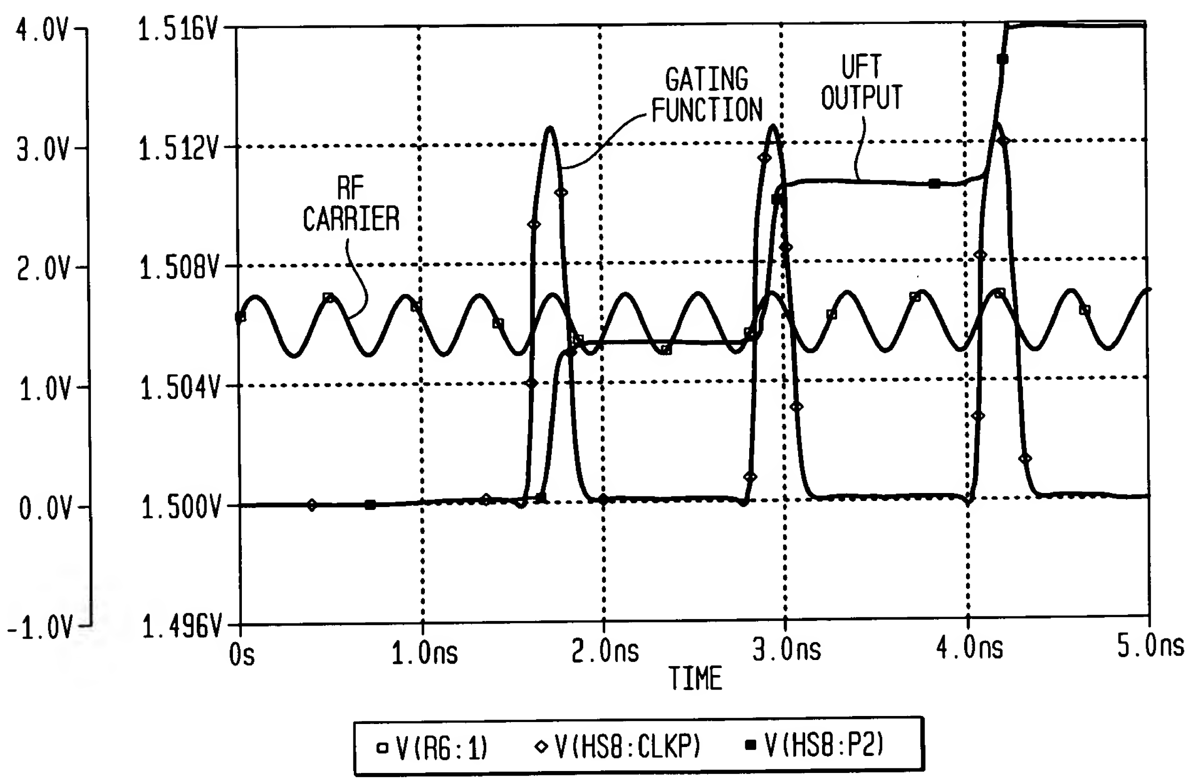
4.0V
3.0V
2.0V
1.0V
0.0V
-1.0V
1.516V
1.512V
1.508V
1.504V
1.500V
1.496V
0s
1.0ns
2.0ns
3.0ns
4.0ns
5.0ns
TIME
GATING FUNCTION
UFT OUTPUT
RF CARRIER
V(R6:1)
V(HS8:CLKP)
V(HS8:P2)

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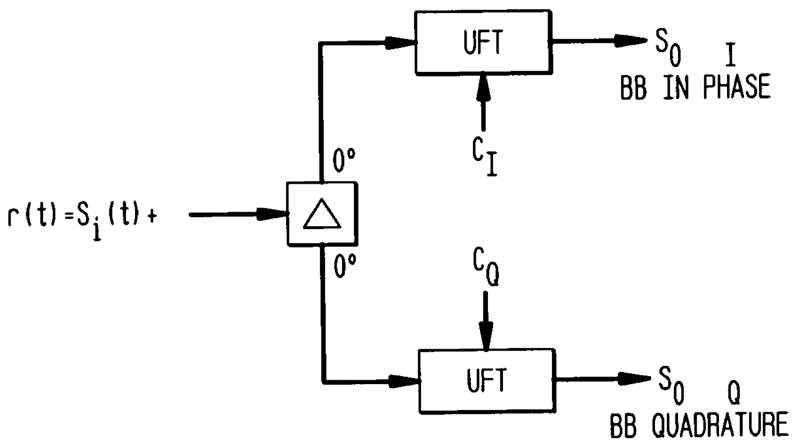
FIG. 194



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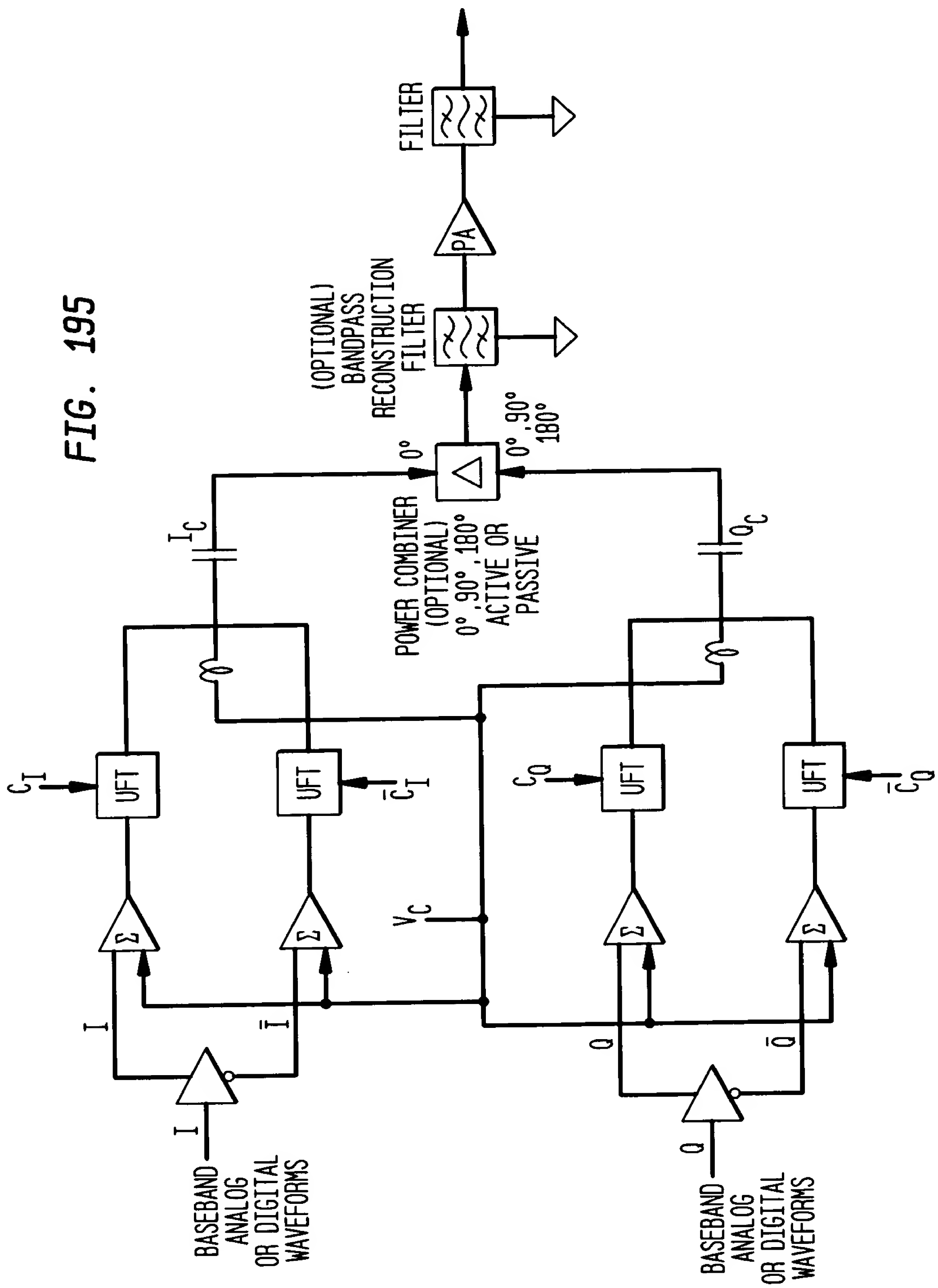

FIG. 195

FIG. 196

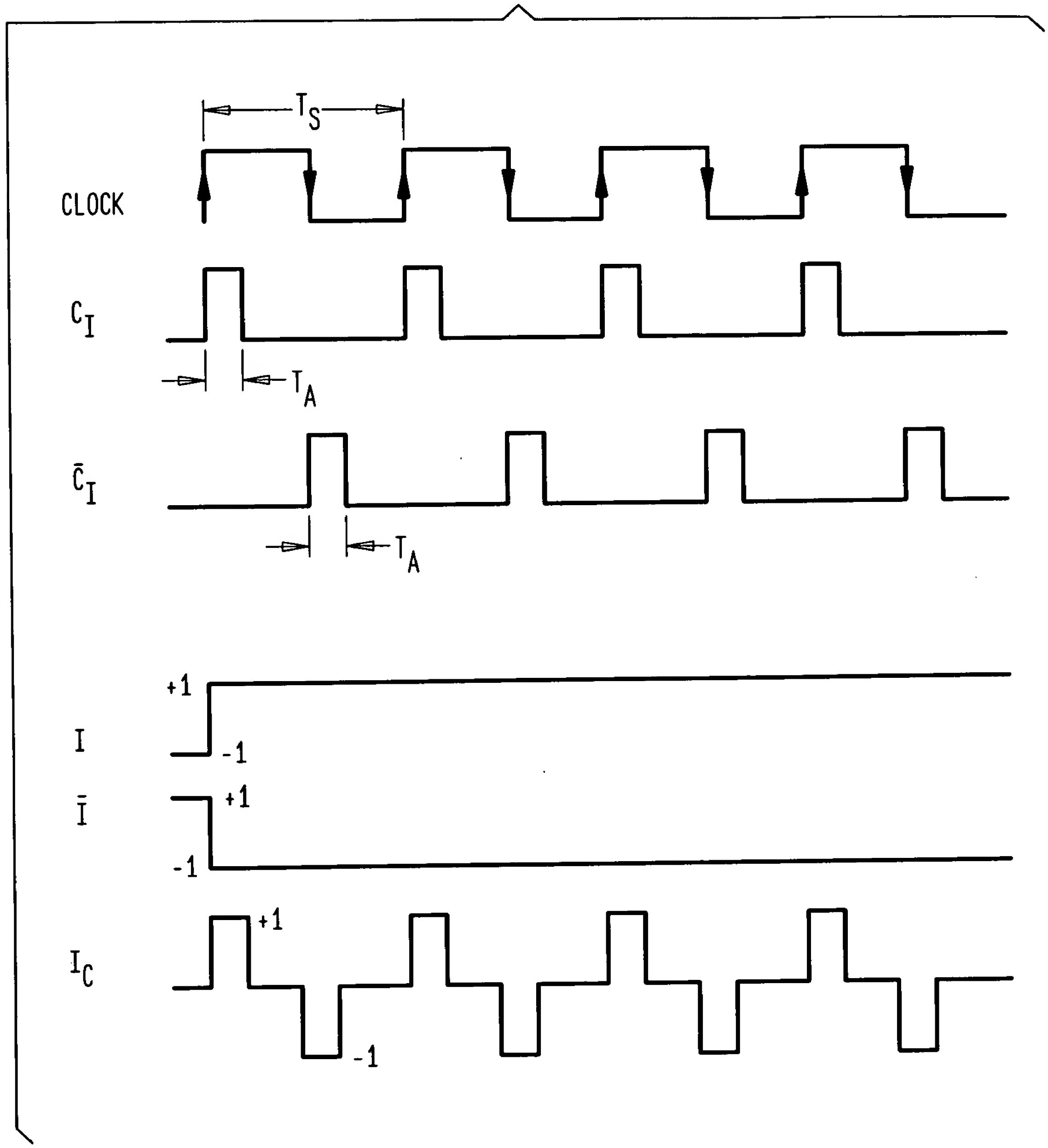

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FIG. 197

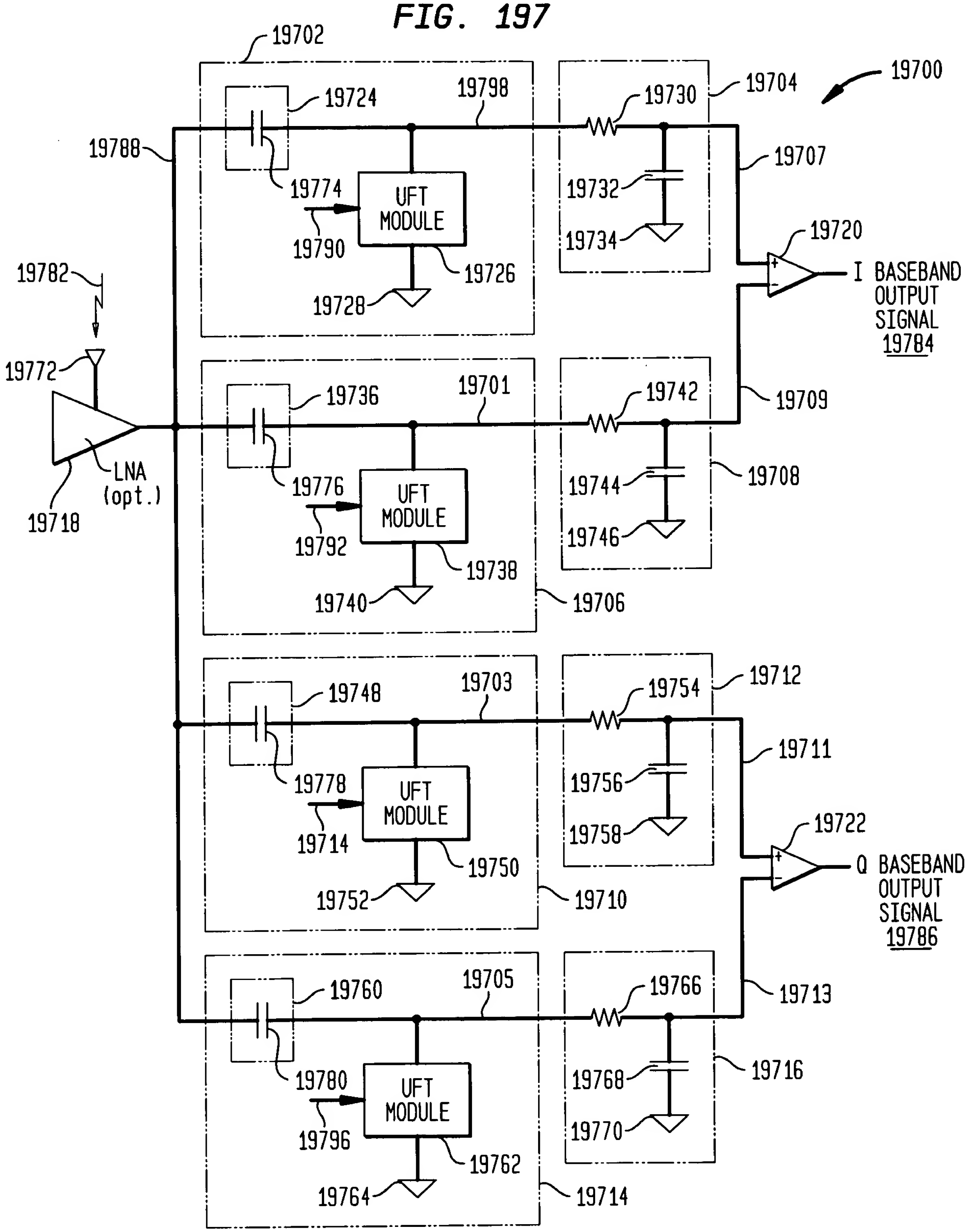

FIG. 198

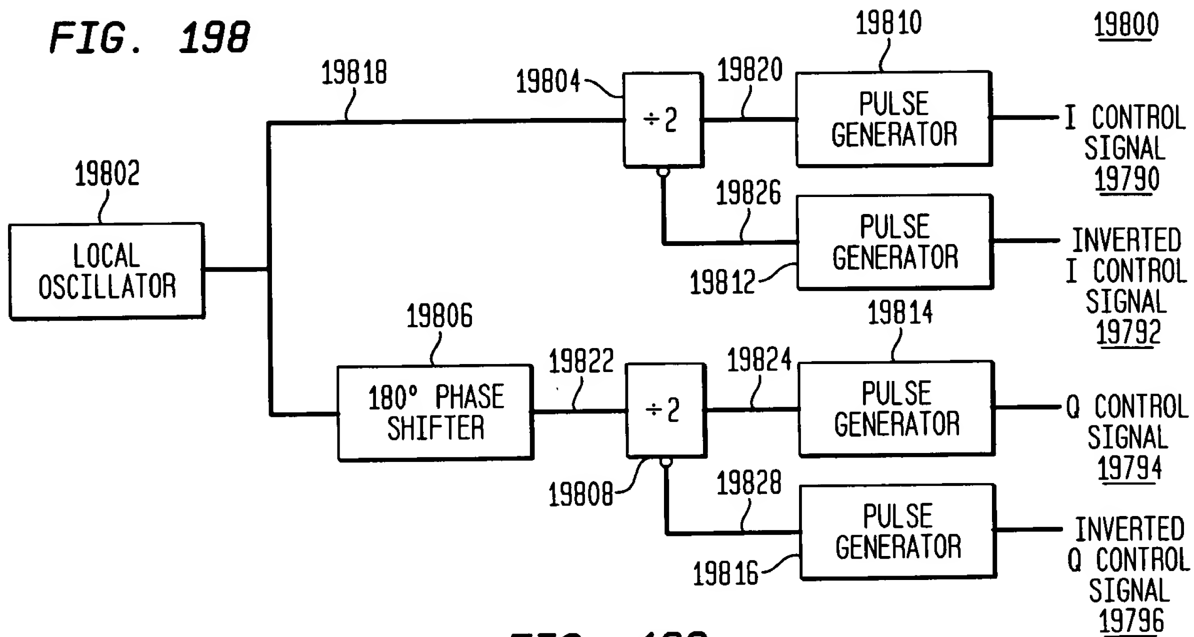

FIG. 199

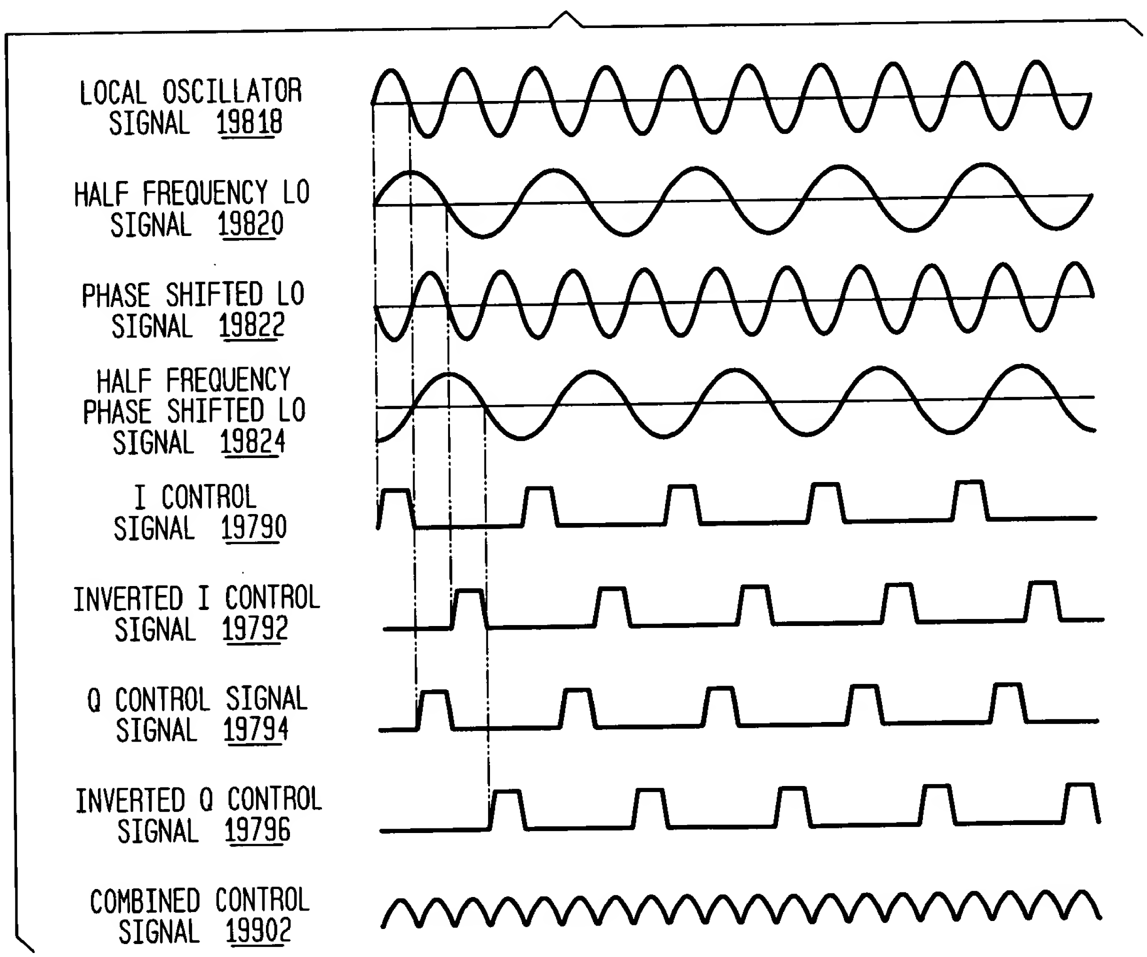

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FIG. 200

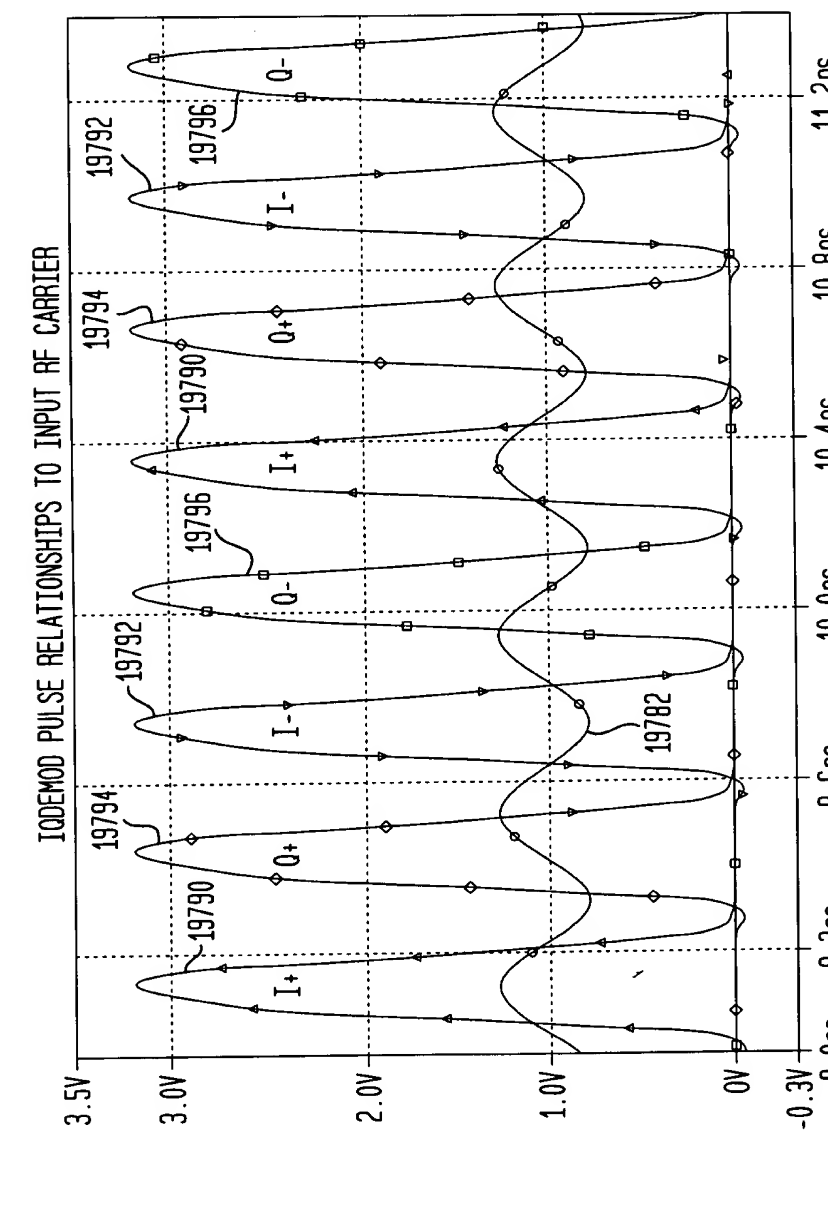


FIG. 201

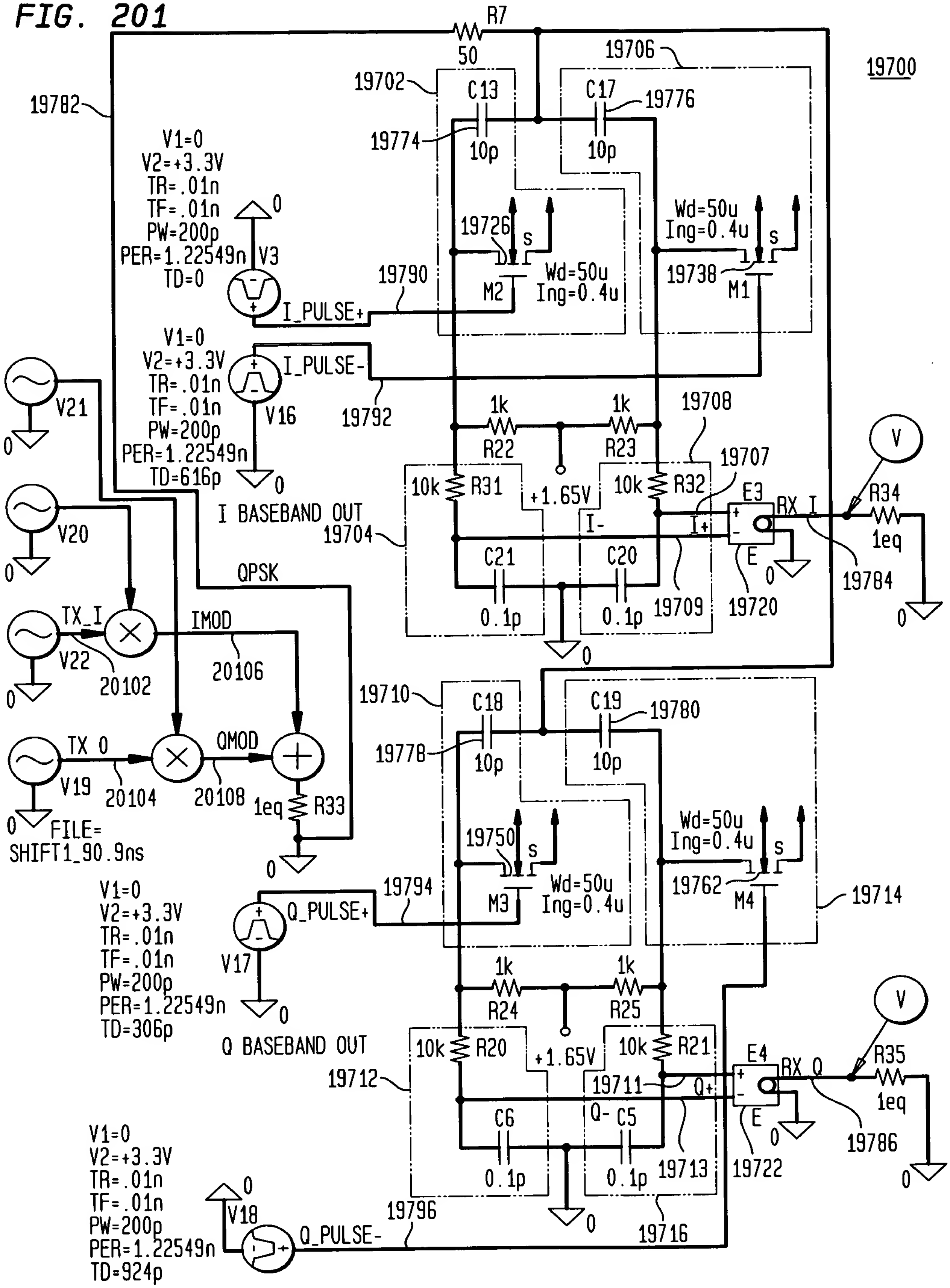

19700
R7
50
19782
19702
19706
C13
C17
19776
19774
10p
10p
V1=0
V2=+3.3V
TR=.01n
TF=.01n
PW=200p
PER=1.22549n
TD=0
V3
19726
Wd=50u
Ing=0.4u
M2
M1
19738
19790
I_PULSE+
I_PULSE-
V16
TD=616p
19792
1k
R22
R23
19708
R31
R32
10k
+1.65V
I BASEBAND OUT
19704
I-
I+
E3
RX I
R34
1eq
19707
19709
19720
19784
C21
C20
0.1p
QPSK
V21
V20
V22
V19
TX_I
TX 0
IMOD
QMOD
20102
20104
20106
20108
R33
FILE=
SHIFT1_90.9ns
19710
19778
C18
C19
19780
19750
M3
M4
19762
19714
19794
Q_PULSE+
V17
TD=306p
R24
R25
R20
R21
Q BASEBAND OUT
19712
19711
Q+
Q-
E4
RX Q
R35
19786
C6
C5
19713
19722
19716
V18
19796
Q_PULSE-
TD=924p

FIG. 202

IQDEMOD SHOWING TIME RELATIONSHIP OF TX_I DATA

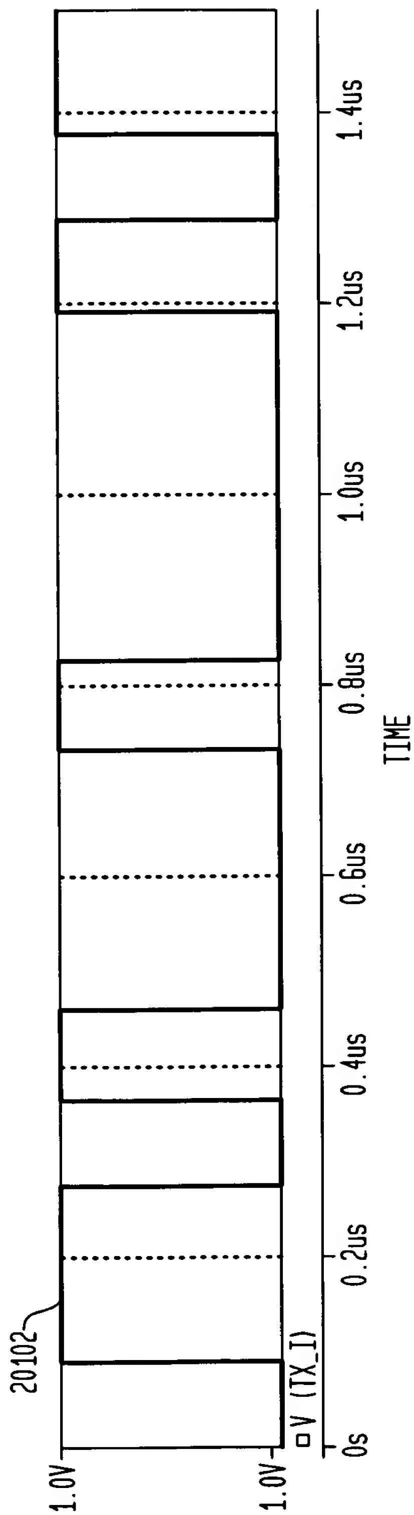
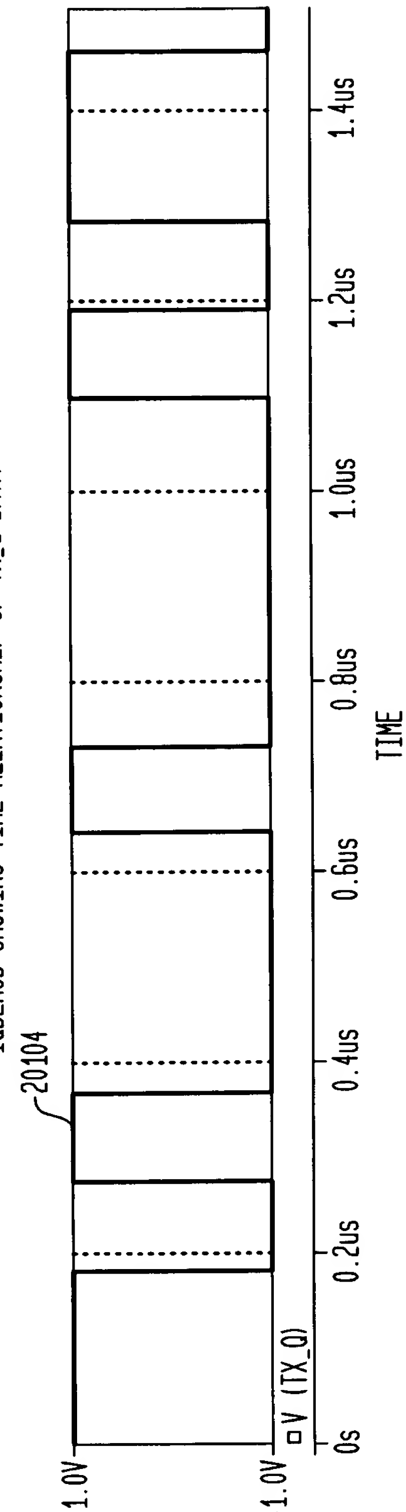


FIG. 203

IQDEMOD SHOWING TIME RELATIONSHIP OF TX_Q DATA



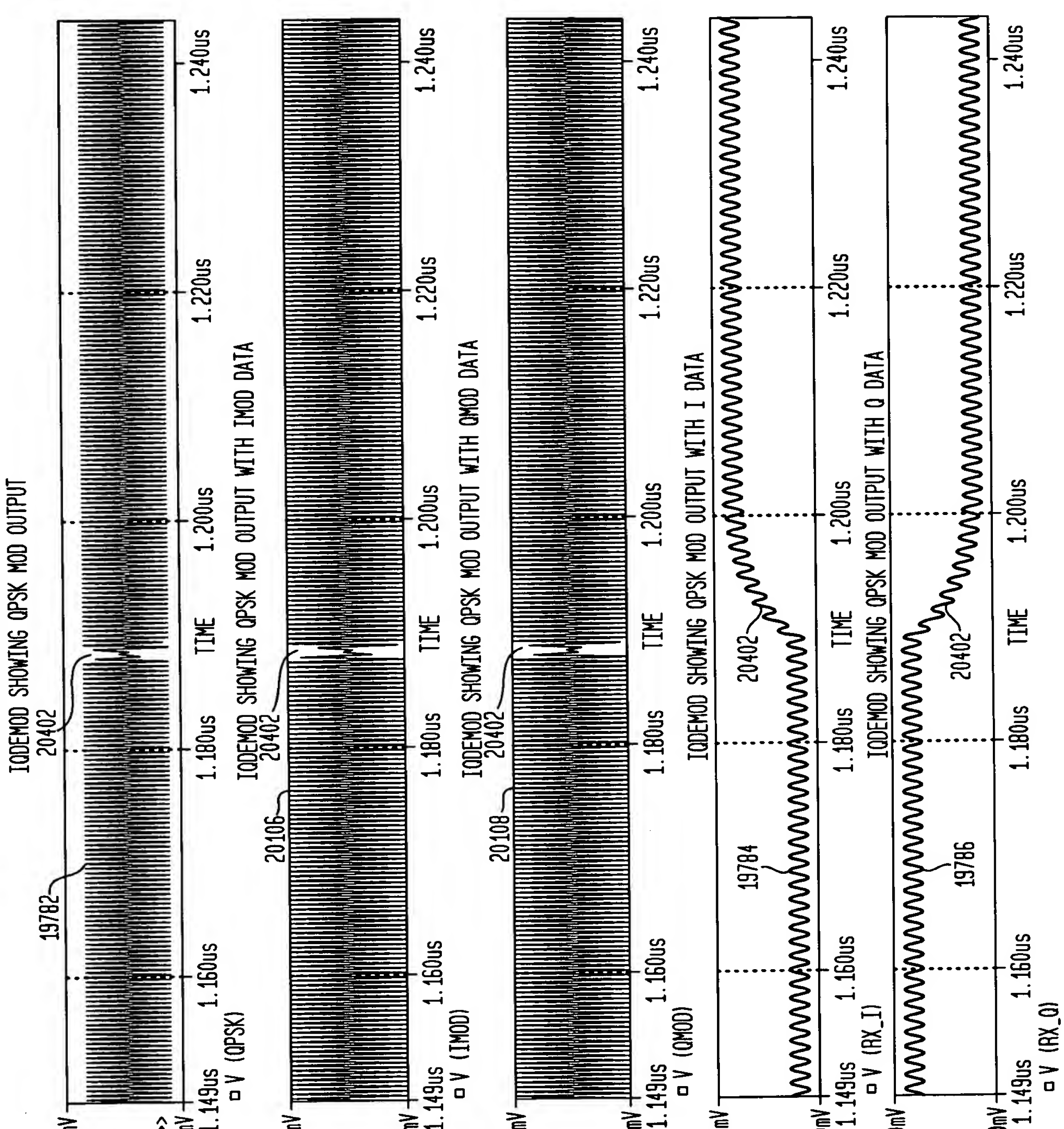


FIG. 204

FIG. 205

FIG. 206

FIG. 207

FIG. 208

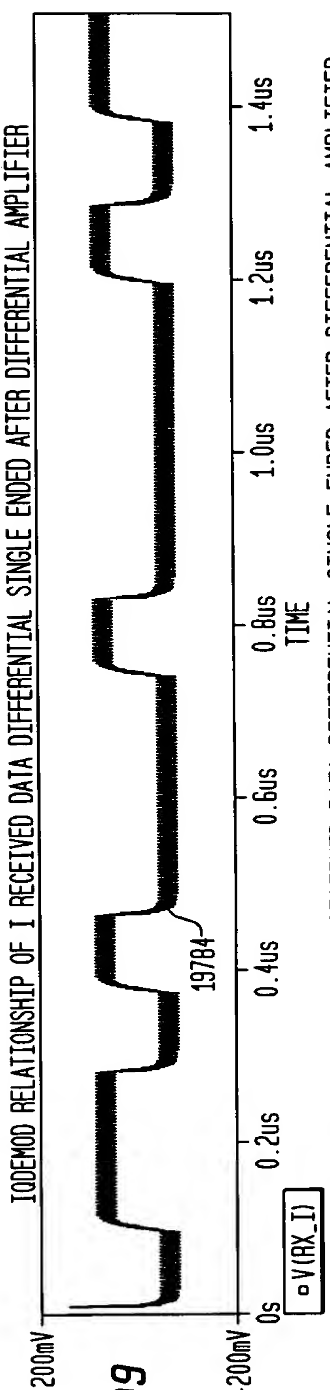


FIG. 209

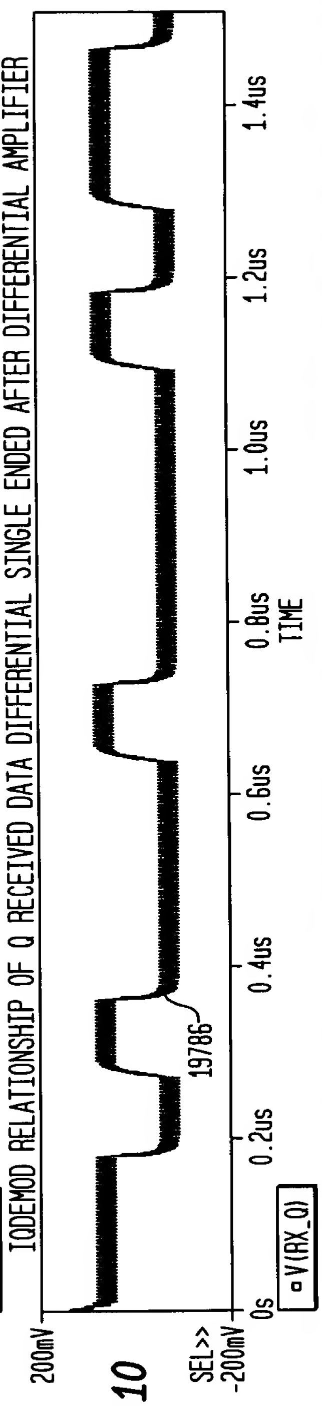


FIG. 210

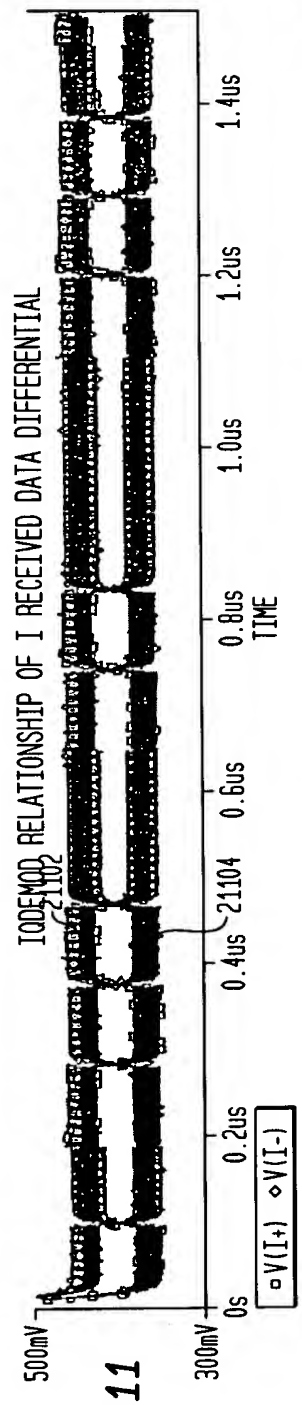


FIG. 211

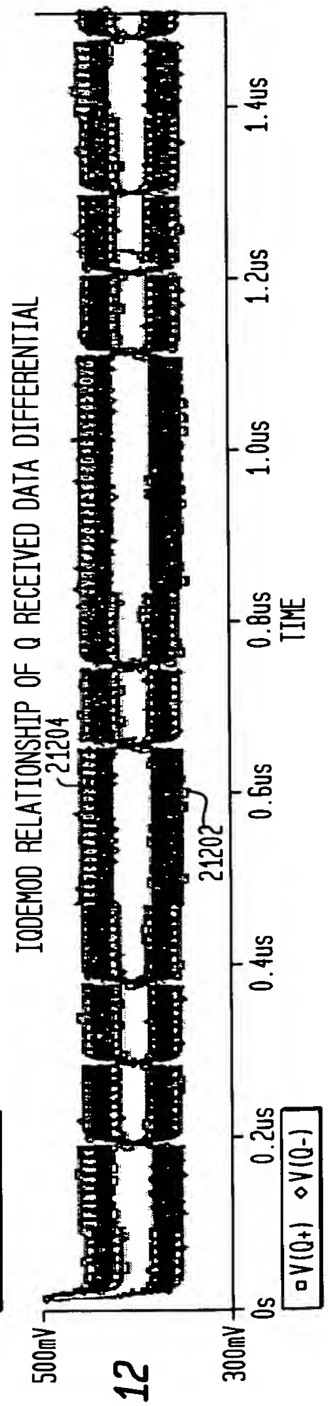


FIG. 212

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FIG. 213

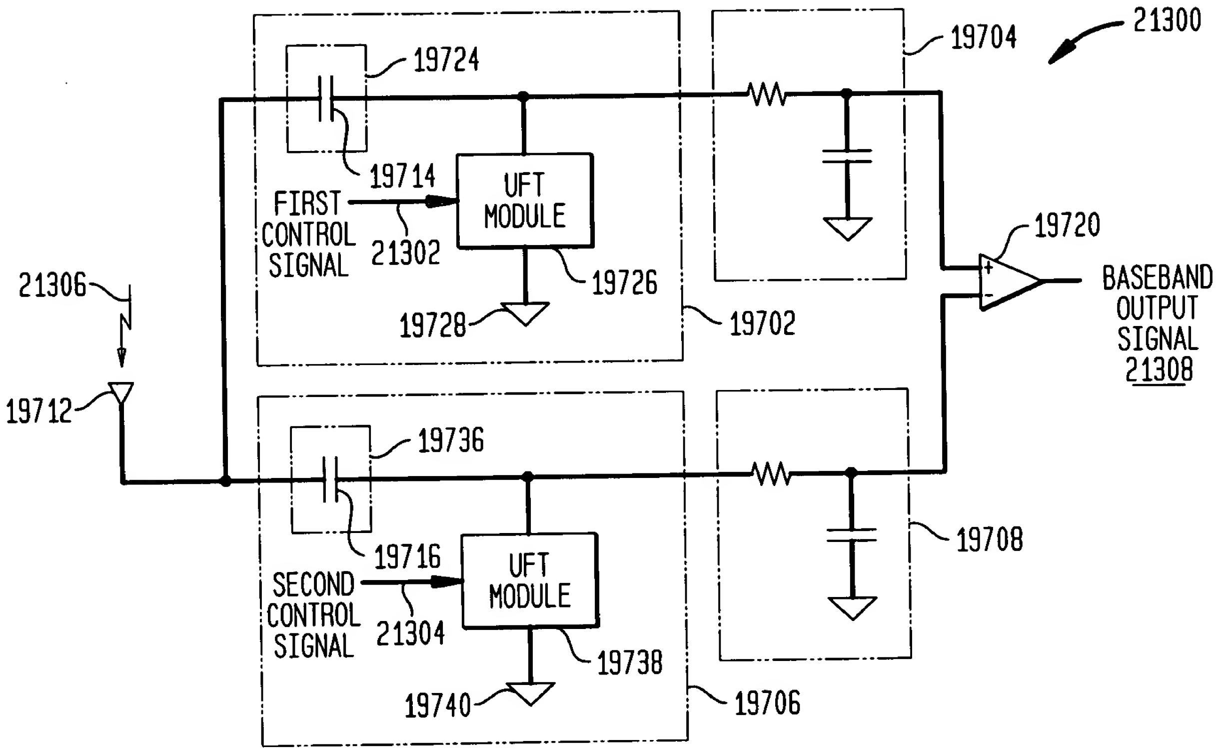

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FIG. 214

FURTHER OPTIMIZED MULTIPLE APERTURE REALIZATION

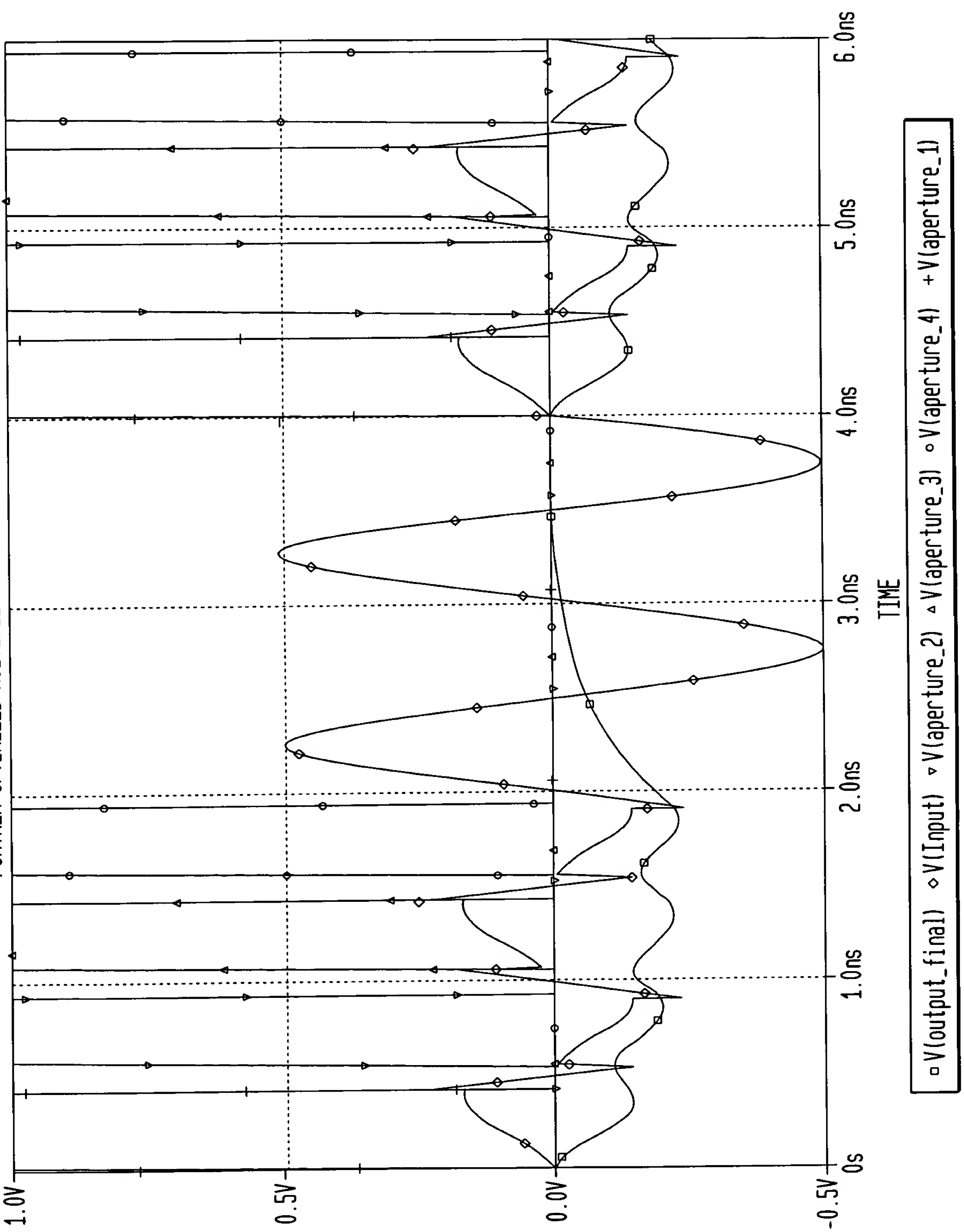

FIG. 215

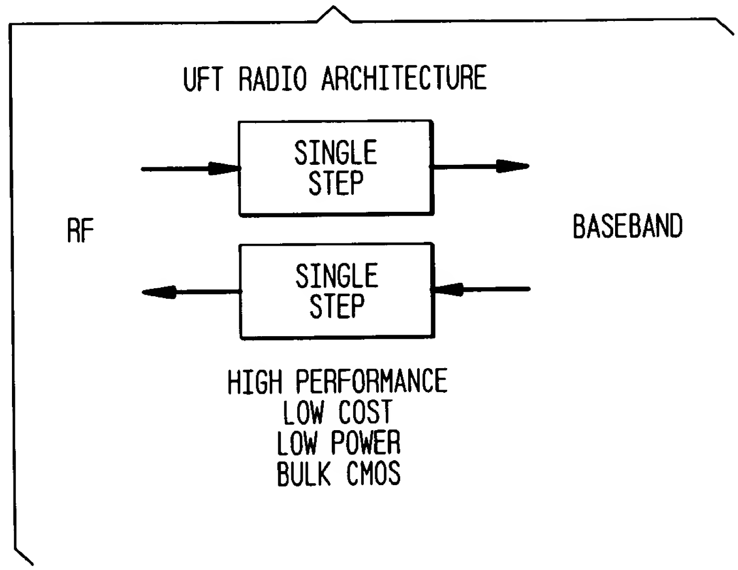

FIG. 216

WIRELESS TRADE-OFF DESIGN CONCERNS

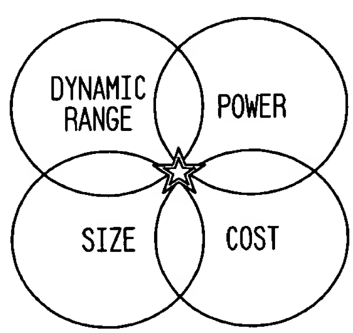

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FIG. 217

NOISE FIGURE CALCULATIONS BASED ON RMS VOLTAGE AND CURRENT NOISE SPECIFICATIONS

ENTER, THE VOLTAGE NOISE DENSITY, e_n, AND THE CURRENT NOISE DENSITY, i_n, FOR THE AMPLIFIER CHOSEN:

$e_n := 6 \cdot 10^{-9}$ V/sqrt(Hz)
$i_n := 1 \cdot 10^{-12}$ A/sqrt(Hz)

ENTER THE SOURCE RESISTANCE DRIVING THE AMPLIFIER:

$K: 1.38 \cdot 10^{-23}$ J/K $T := 290K$

$$\mathrm{PARALELL}(x,y) := \frac{x \cdot y}{x+y} \qquad NF(R_S) := 20 \cdot \log\left(\sqrt{\frac{e_n^2 + 4 \cdot K \cdot T \cdot R_S + i_n^2 \cdot R_S^2}{4 \cdot K \cdot T \cdot R_S}}\right)$$

IF WE PLOT NOISE FIGURE VERSUS SOURCE RESISTANCE WE CAN GET AN IDEA OF WHAT IS THE OPTIMUM SOURCE RESISTANCE.
IT IS NOT NECESSARILY THE LOWEST RESISTANCE!

$R_S := 100, 200 \ldots 100 \cdot 10^3$

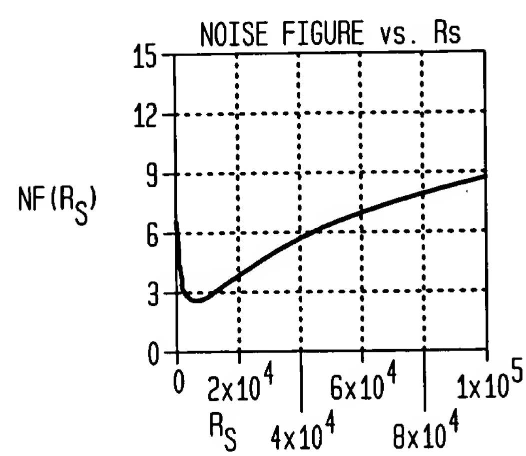

FIG. 218A

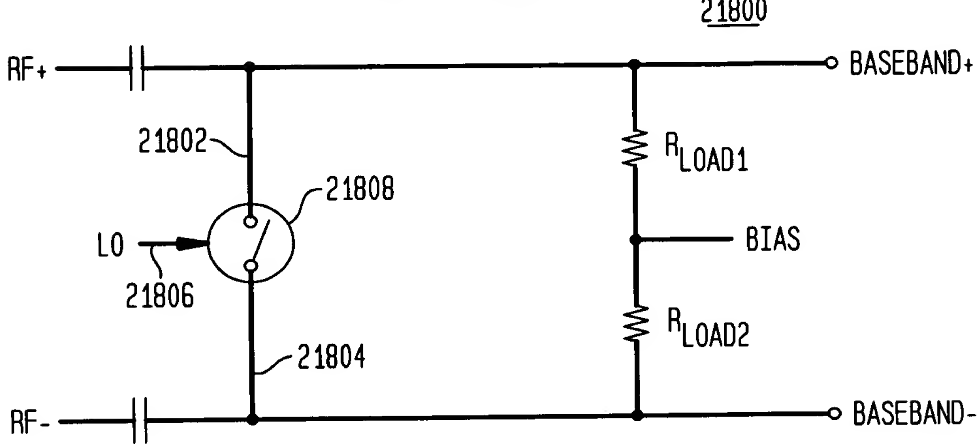

FIG. 218B

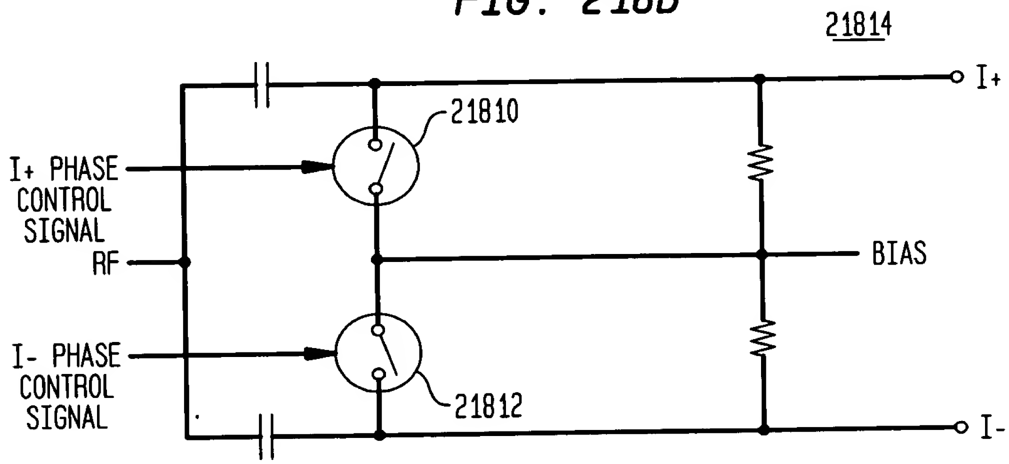

FIG. 218C

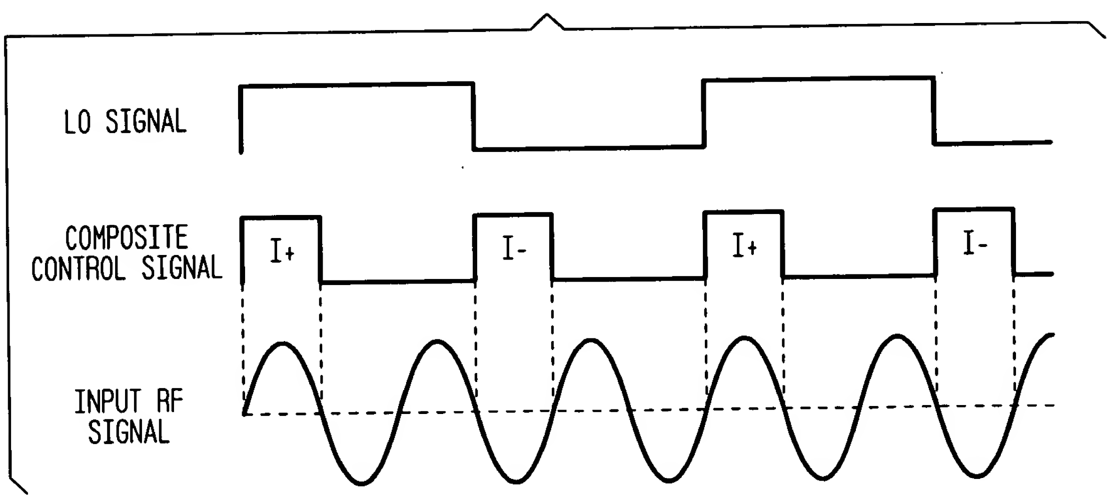

FIG. 218D

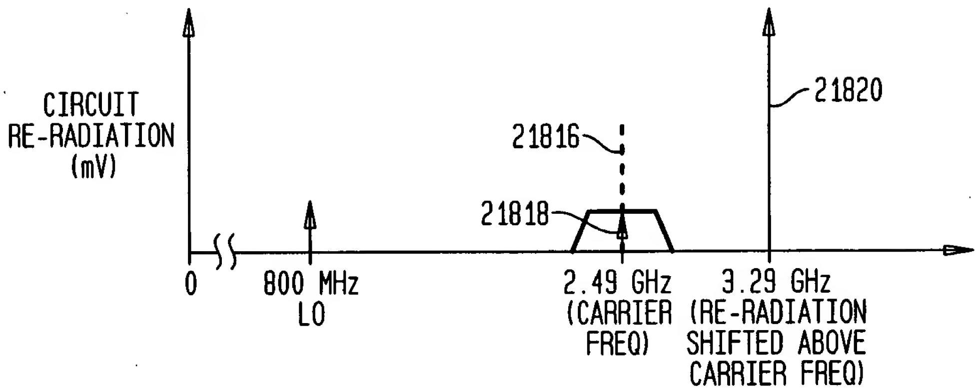

FIG. 218F

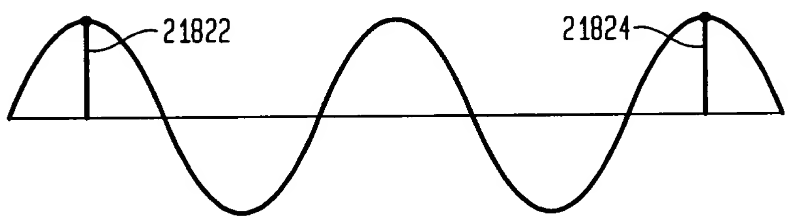

FIG. 218G

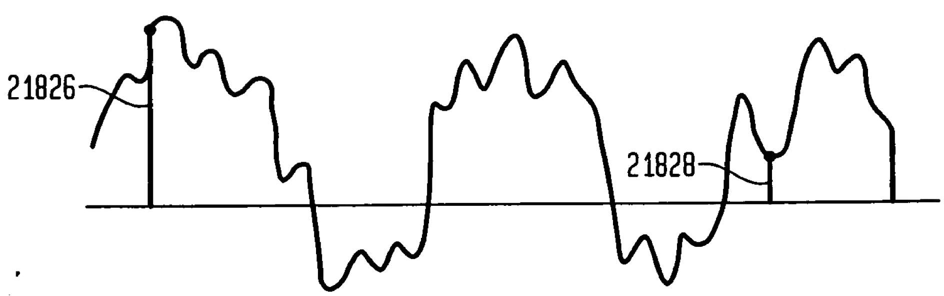

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FIG. 218E

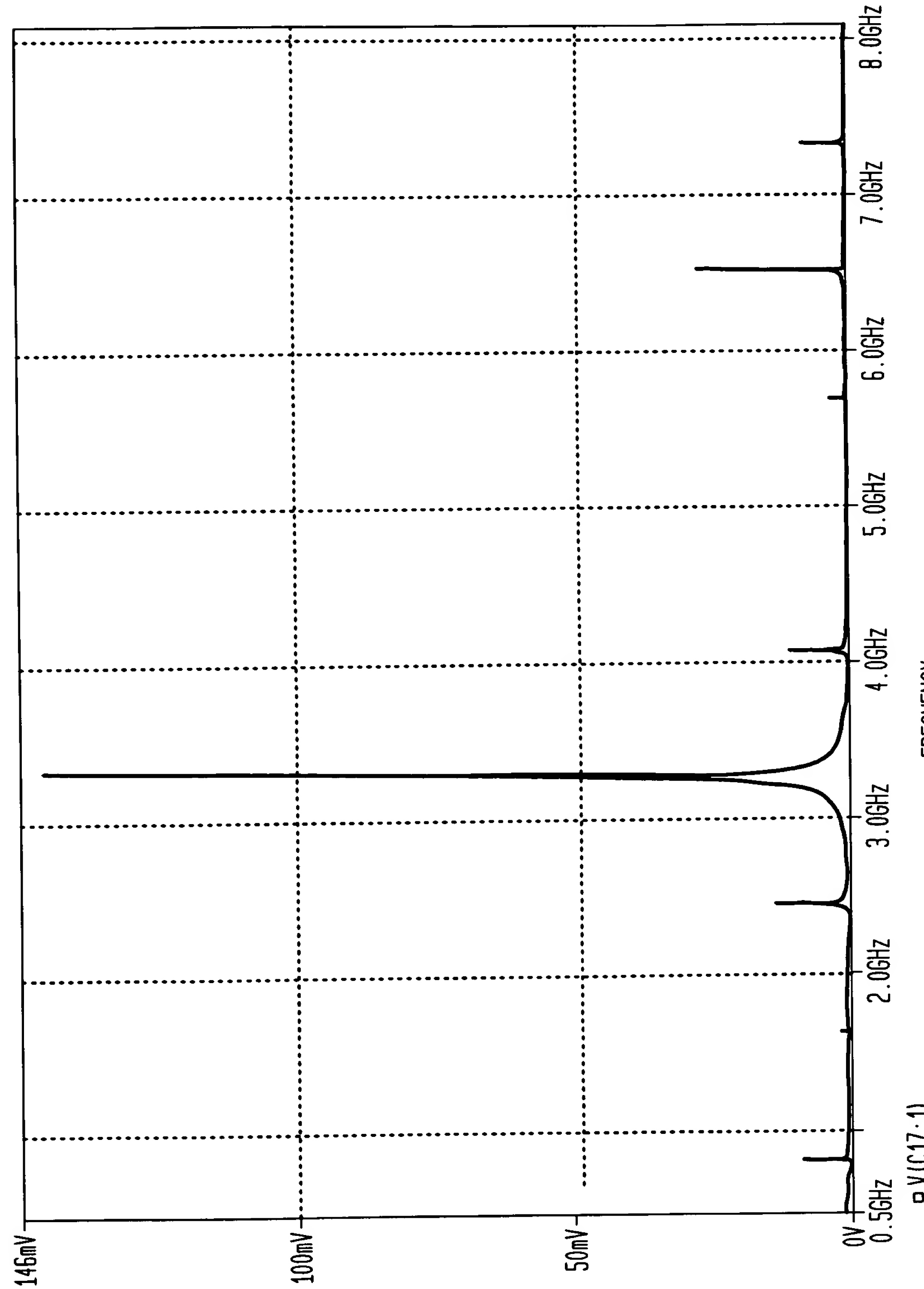


FIG. 219

IC CONCEPTUAL SCHEMATIC

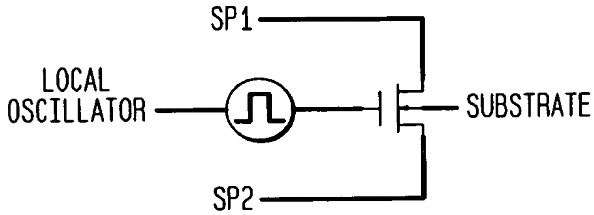
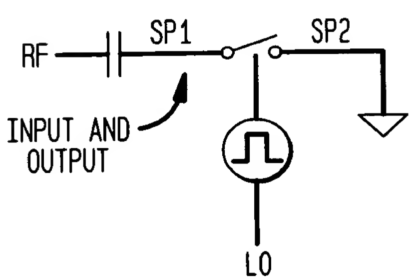


FIG. 220

BASIC ARCHITECTURE



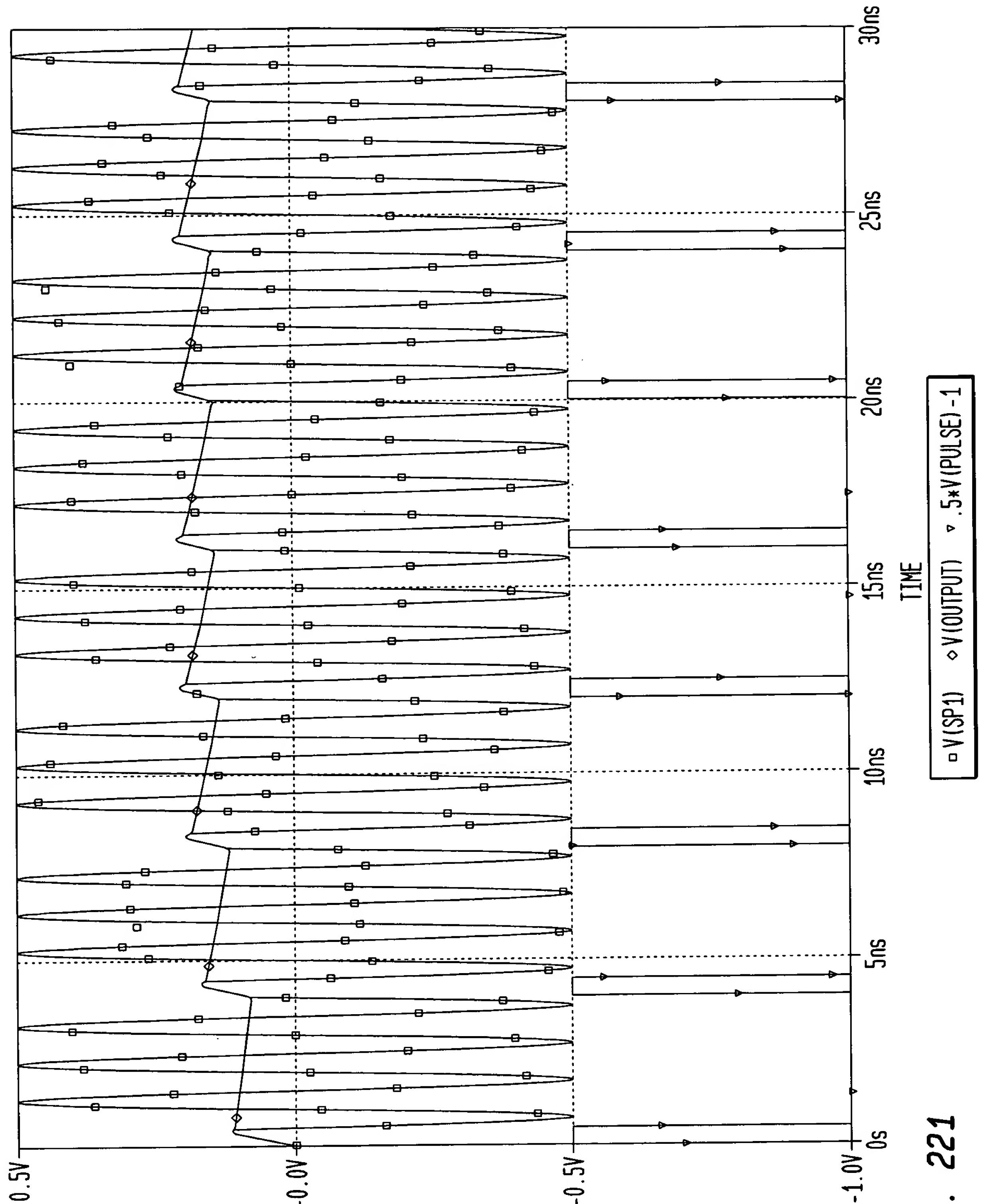

0.5V
-0.0V
-0.5V
-1.0V
0s
5ns
10ns
15ns
20ns
25ns
30ns
TIME
V(SP1)
V(OUTPUT)
.5*V(PULSE)-1

FIG. 221

FIG. 222

DC EQUATIONS

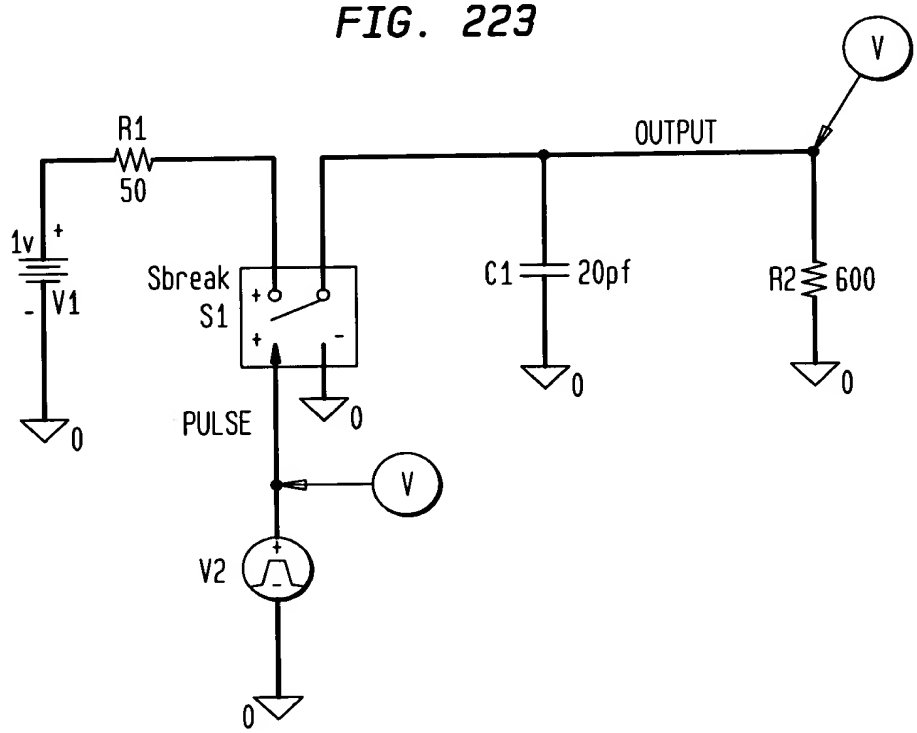
$$Vin=V\cdot\frac{Rout}{Rin+Rout}$$

$$Vc=Vin-(Vin-Vinit)\cdot\exp\left(\frac{-tc}{Rin\cdot C}\right)$$

$$Vd=Vc\cdot\exp\left(\frac{-td}{Rout\cdot C}\right)$$

DEFINITIONS:
- Rin - INPUT RESISTANCE
- Rout - OUTPUT RESISTANCE
- C - CAPACITOR
- tc - CHARGE TIME OR APERATURE
- td - DISCHARGE TIME OR LO PERIOD-tc
- V - INPUT VOLTAGE
- Vinit - INITIAL CAPACITOR VOLTAGE
- Vc - FINAL CHARGE CAPACITOR VOLTAGE
- Vd - FINAL DISCHARGE CAPACITOR VOLTAGE

FIG. 223



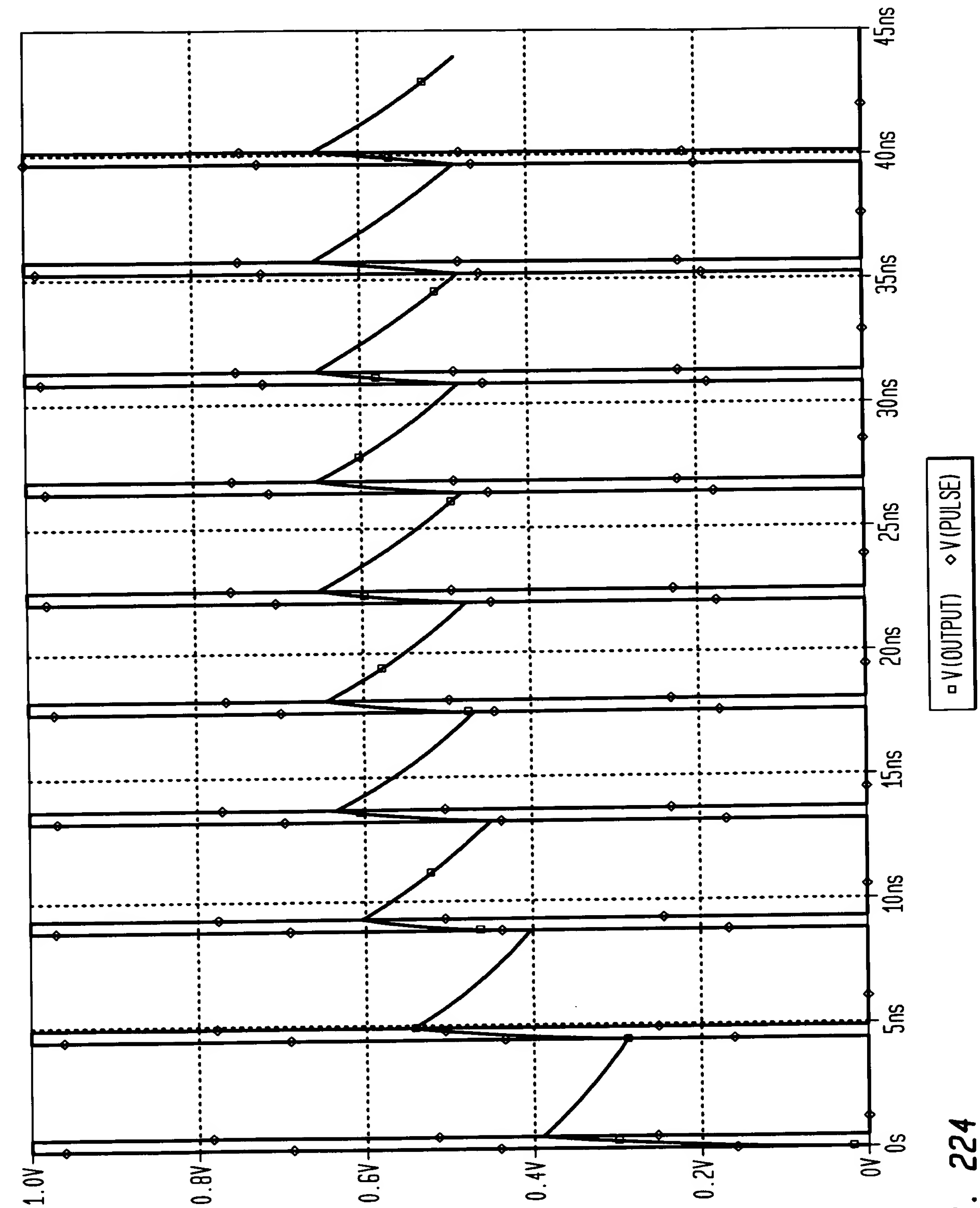
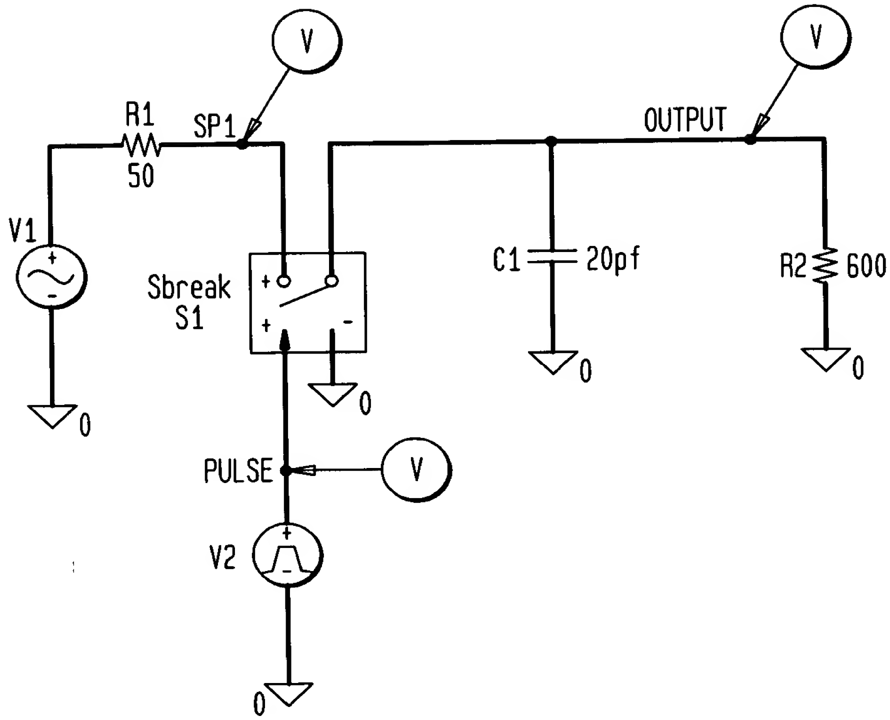

1.0V
0.8V
0.6V
0.4V
0.2V
0V
0s
5ns
10ns
15ns
20ns
25ns
30ns
35ns
40ns
45ns
□ V(OUTPUT) ◇ V(PULSE)

FIG. 224

FIG. 225


V
V
R1
SP1
OUTPUT
50
V1
Sbreak
S1
C1
20pf
R2
600
0
0
0
0
0
PULSE
V
V2
0

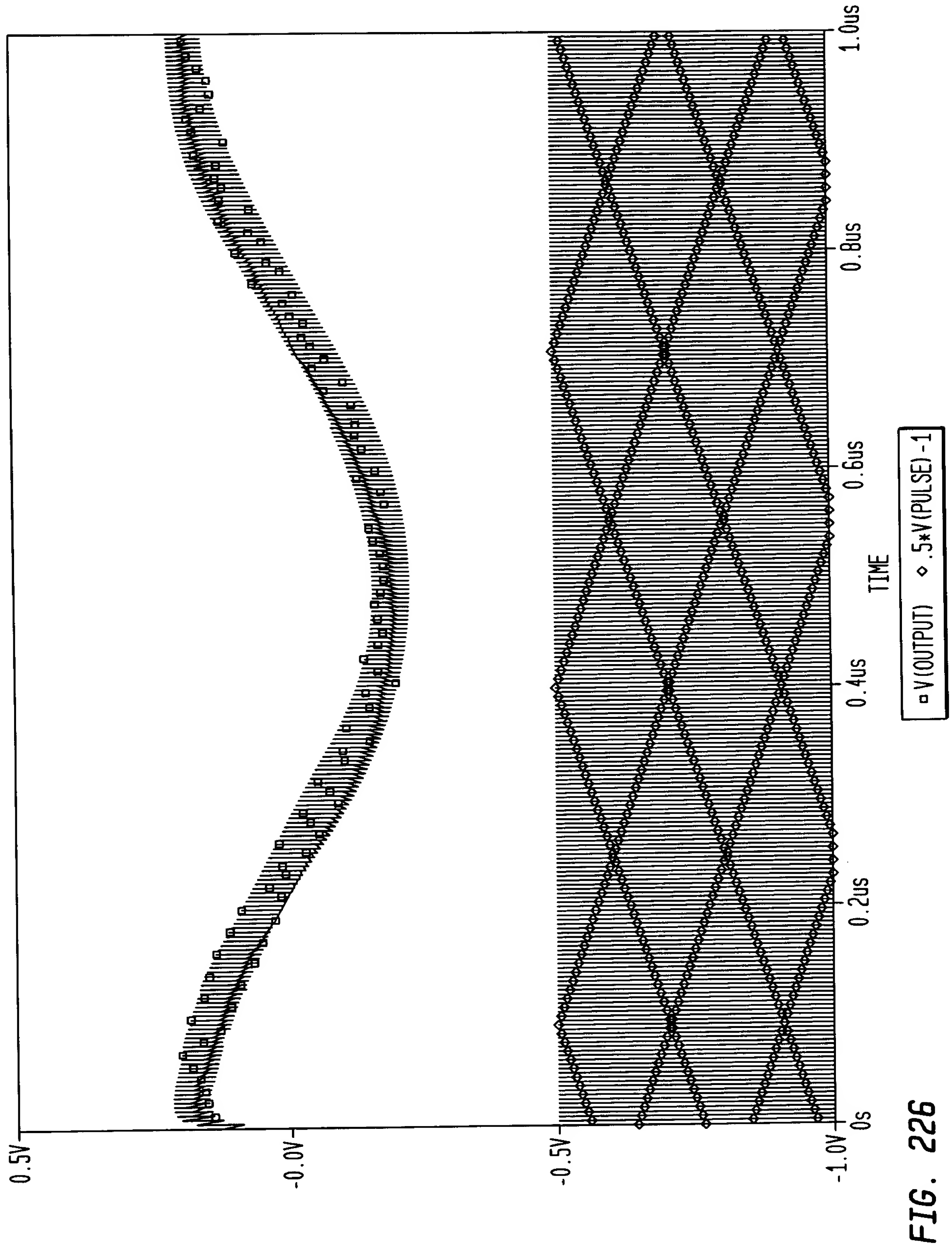

0.5V
-0.0V
-0.5V
-1.0V
0s
0.2us
0.4us
0.6us
0.8us
1.0us
TIME
□ V(OUTPUT) ◇ .5*V(PULSE)-1

FIG. 226

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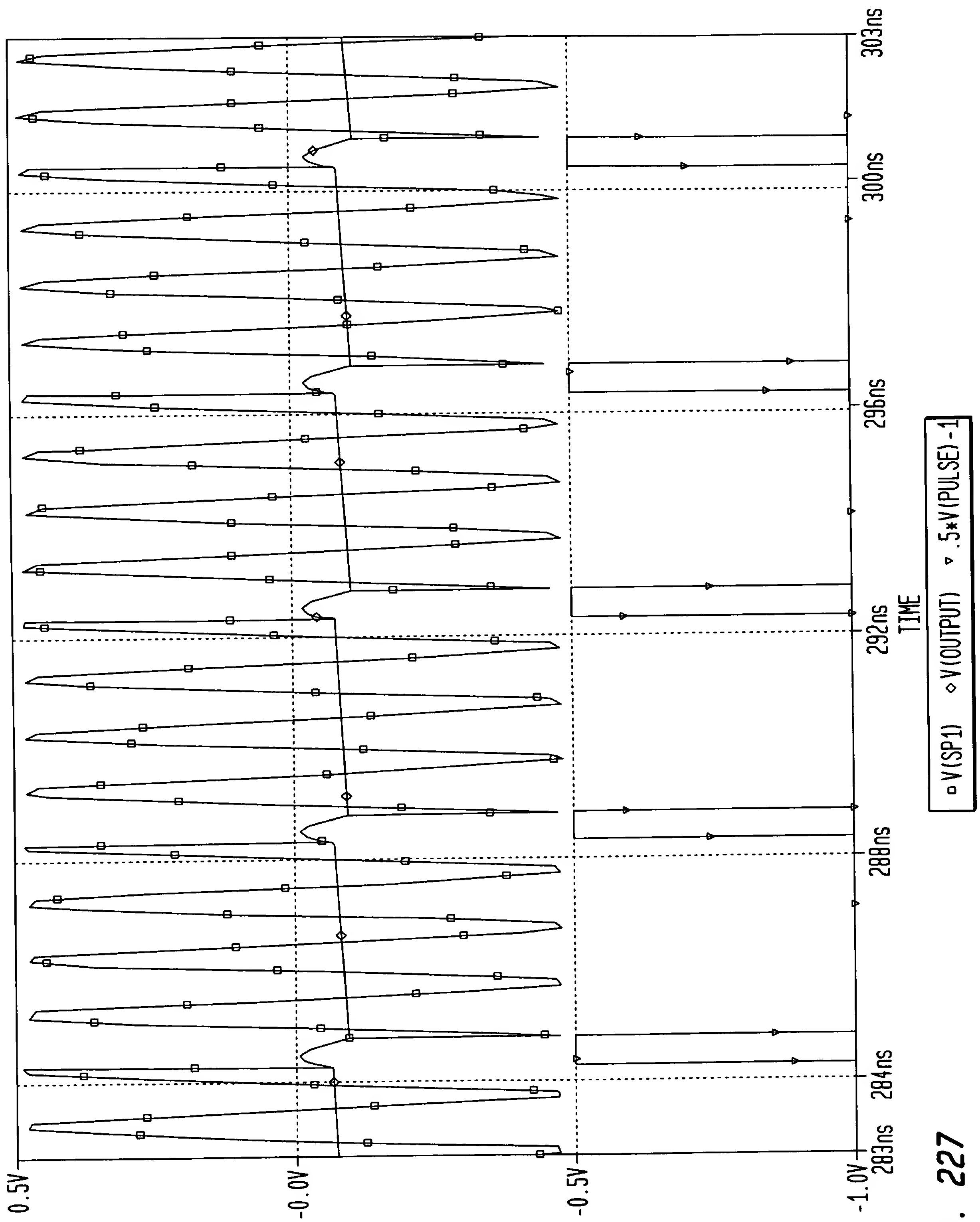

FIG. 227

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FIG. 228

CHARGE TRANSFER

DEFINITIONS:

q=CHARGE IN COULOMBS
C=CAPACITANCE IN FARADS
V=VOLTAGE IN VOLTS
A=INPUT SIGNAL AMPLITUDE

$$q=C\cdot V$$
$$V=A\cdot \sin(t)$$
$$q(t)=C\cdot A\cdot \sin(t)$$
$$\Delta q(t)=C\cdot A\cdot \sin(t)-C\cdot A\cdot \sin(t-T)$$
$$\Delta q(t)=C\cdot A\cdot (\sin(t)-\sin(t-T)) \qquad \text{EQUATION A}$$

$\Delta q(t)$ EXPRESSES THE CHANGE IN CHARGE ACROSS CAPACITOR C DURING APERTURE T. AS CAN BE SEEN, WHEN APERTURE T TENDS TOWARDS 0, $\Delta q(t)$ TENDS TOWARDS 0.

FIG. 229

USING THE SUM TO PRODUCT TRIGONOMETRIC IDENTITY,

$$\sin(\alpha)-\sin(\beta)=2\cdot\sin\left(\frac{\alpha-\beta}{2}\right)\cdot\cos\left(\frac{\alpha+\beta}{2}\right) \qquad \text{IDENTITY 1}$$

EQUATION 1 CAN BE RE-WRITTEN AS:

$$\Delta q(t)=2\cdot C\cdot A\cdot\sin\left[\frac{t-(t-T)}{2}\right]\cdot\cos\left[\frac{t+(t-T)}{2}\right]$$

$$\Delta q(t)=2\cdot C\cdot A\cdot\sin\left(\frac{1}{2}\cdot T\right)\cdot\cos\left(t-\frac{1}{2}\cdot T\right) \qquad \text{EQUATION B}$$

THE sin TERM IN EQUATION B IS A FUNCTION OF APERTURE T ONLY. IT IS EASILY SEEN THAT $\Delta q(t)$ WILL OBTAIN A MAXIMUM VALUE WHEN T IS EQUAL TO AN ODD MULTIPLE OF π i.e., π 3 π 5 π.. THEREFORE, CAPACITOR C EXPERIENCES THE GREATEST CHANGE IN CHARGE WHEN THE APERTURE HAS A VALUE OF π OR A TIME INTERVAL REPRESENTATIVE OF 180 DEGREES OF THE INPUT SINUSOID. CONVERSELY, WHEN T IS EQUAL TO 2π, 4π, 6π....MINIMAL CHARGE IS TRANSFERRED.

FIG. 230

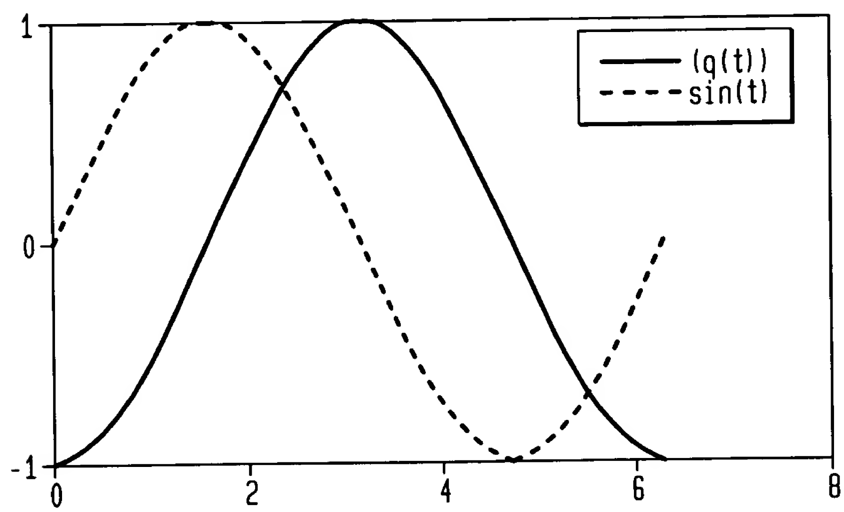
SOLVING FOR q(t) BY INTEGRATING EQUATION A ALLOWS THE CHARGE ON C WITH RESPECT TO TIME TO BE GRAPHED ON THE SAME AXIS AS THE INPUT SINUSOID sin(t).

$$q(t)=\int C\cdot A\cdot(\sin(t)-\sin(t-T))\,dt$$

$$q(t)=-\cos(t)\cdot C\cdot A+\cos(t-T)\cdot C\cdot A$$

$$q(t)=C\cdot A\cdot(\cos(t-T)-\cos(t)) \qquad \text{EQUATION C}$$

FIG. 231



GRAPH 1

C=1; A=.5, T=π

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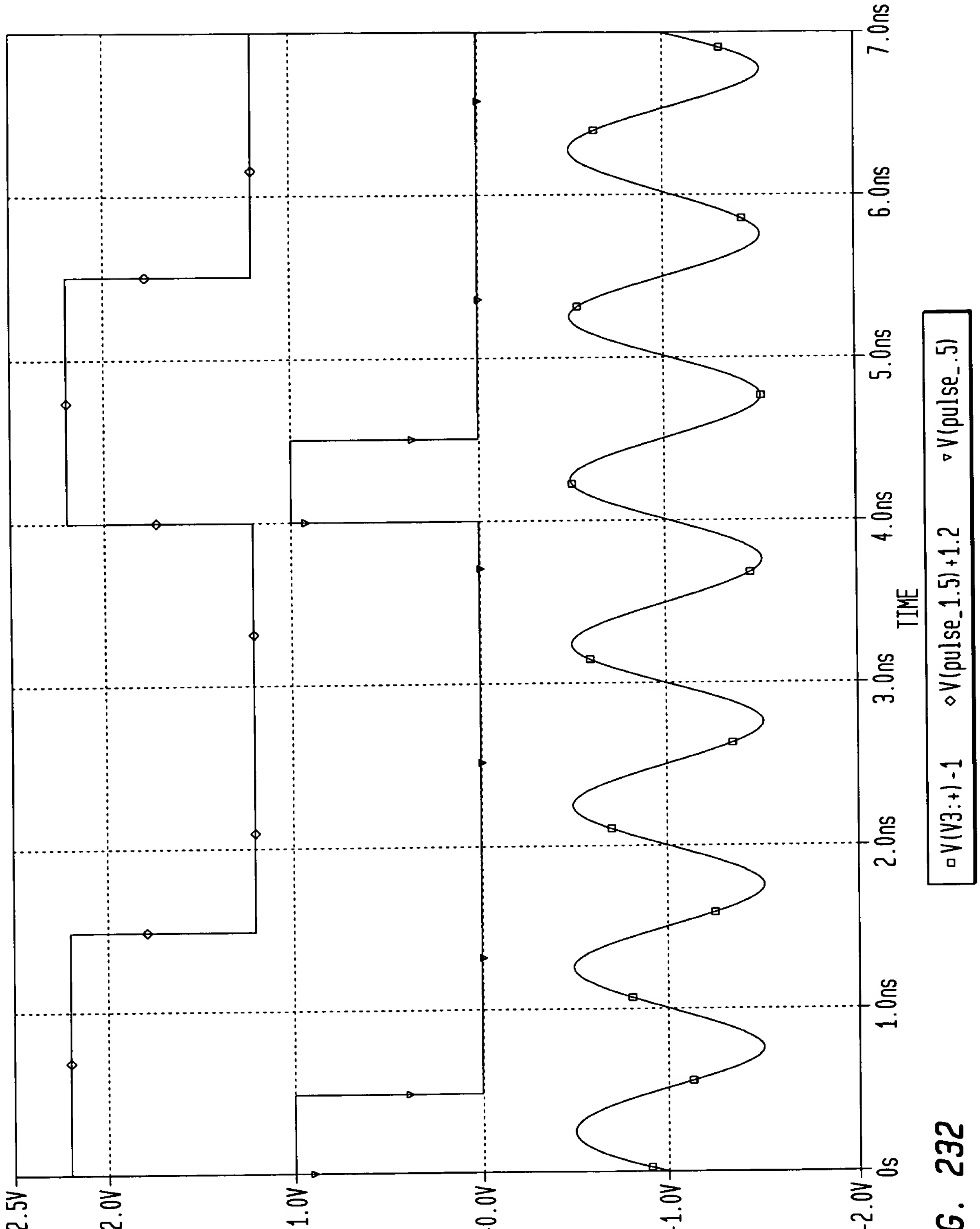

FIG. 232

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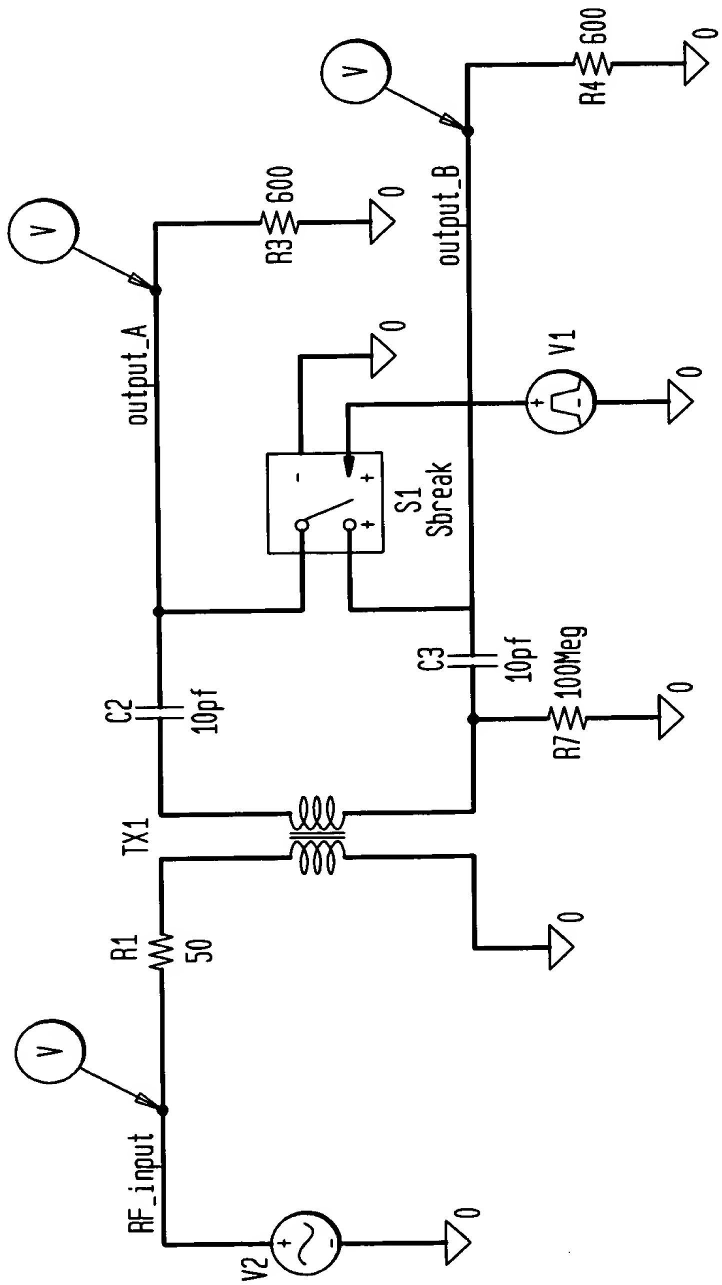
FIG. 233



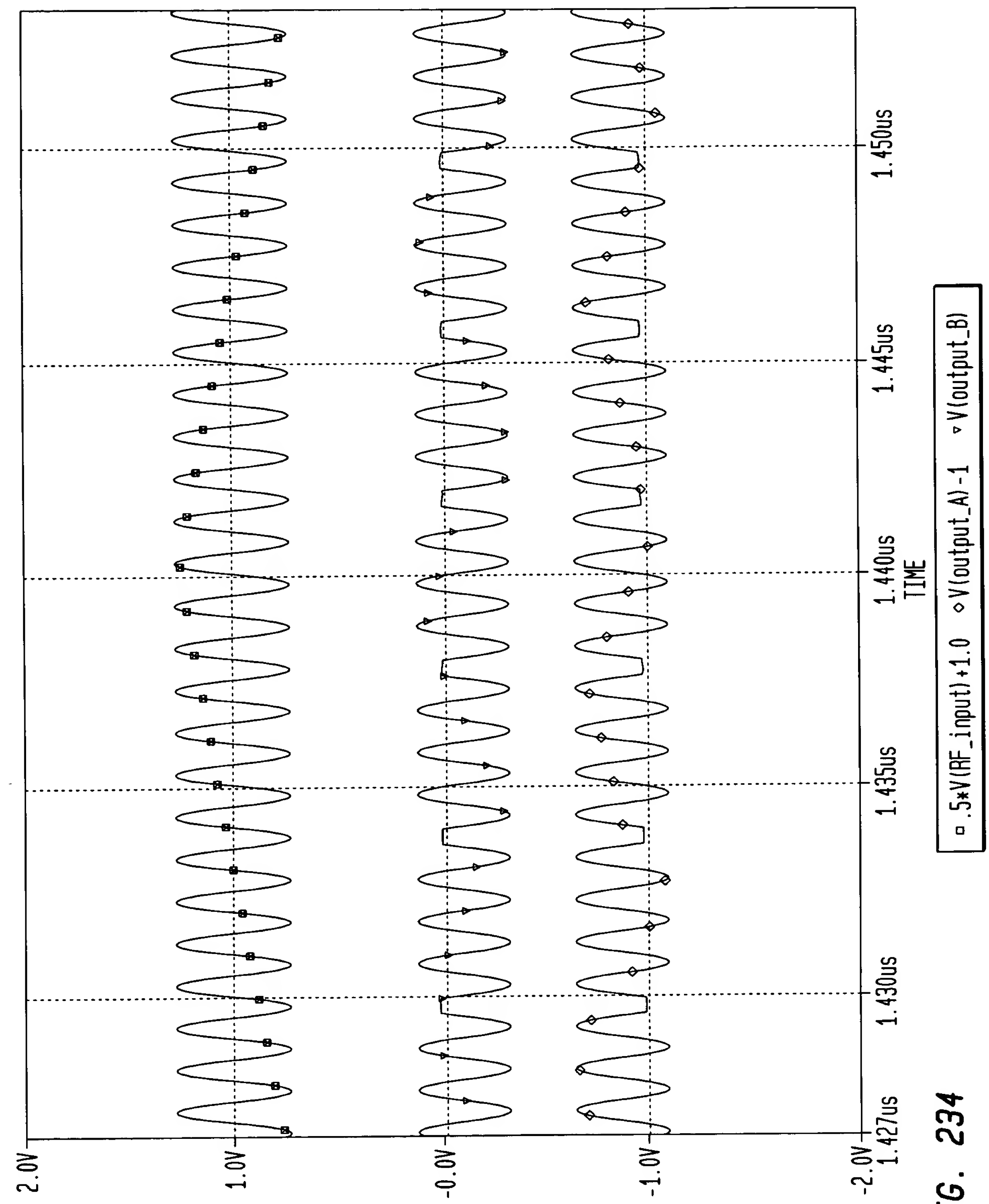

2.0V
1.0V
-0.0V
-1.0V
-2.0V
1.427us
1.430us
1.435us
1.440us
1.445us
1.450us
TIME
.5*V(RF_input)+1.0
V(output_A)-1
V(output_B)

FIG. 234

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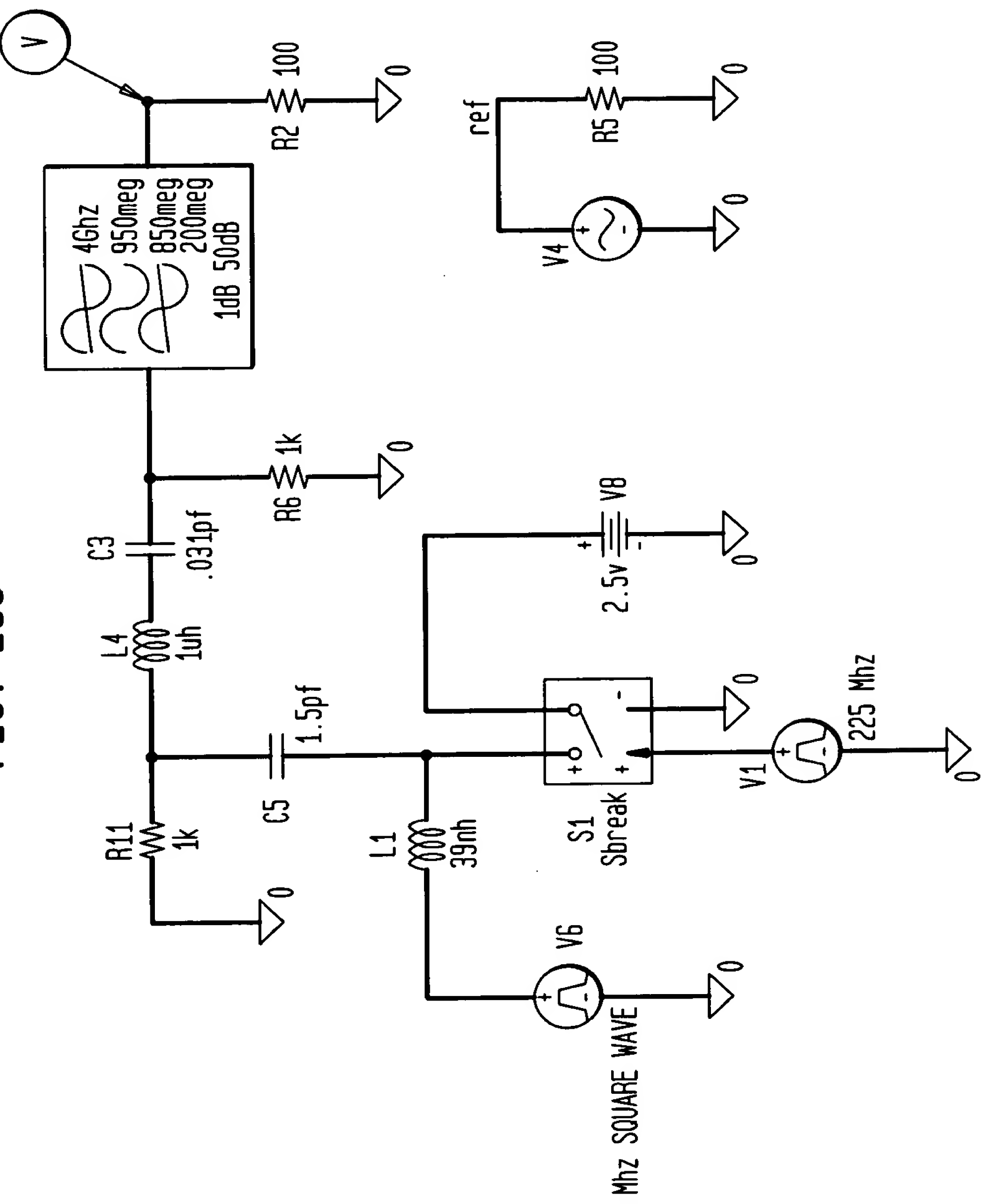

FIG. 235

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Inventors: SORRELLS et al.
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Electromagnetic Signal, and Transforms for Same

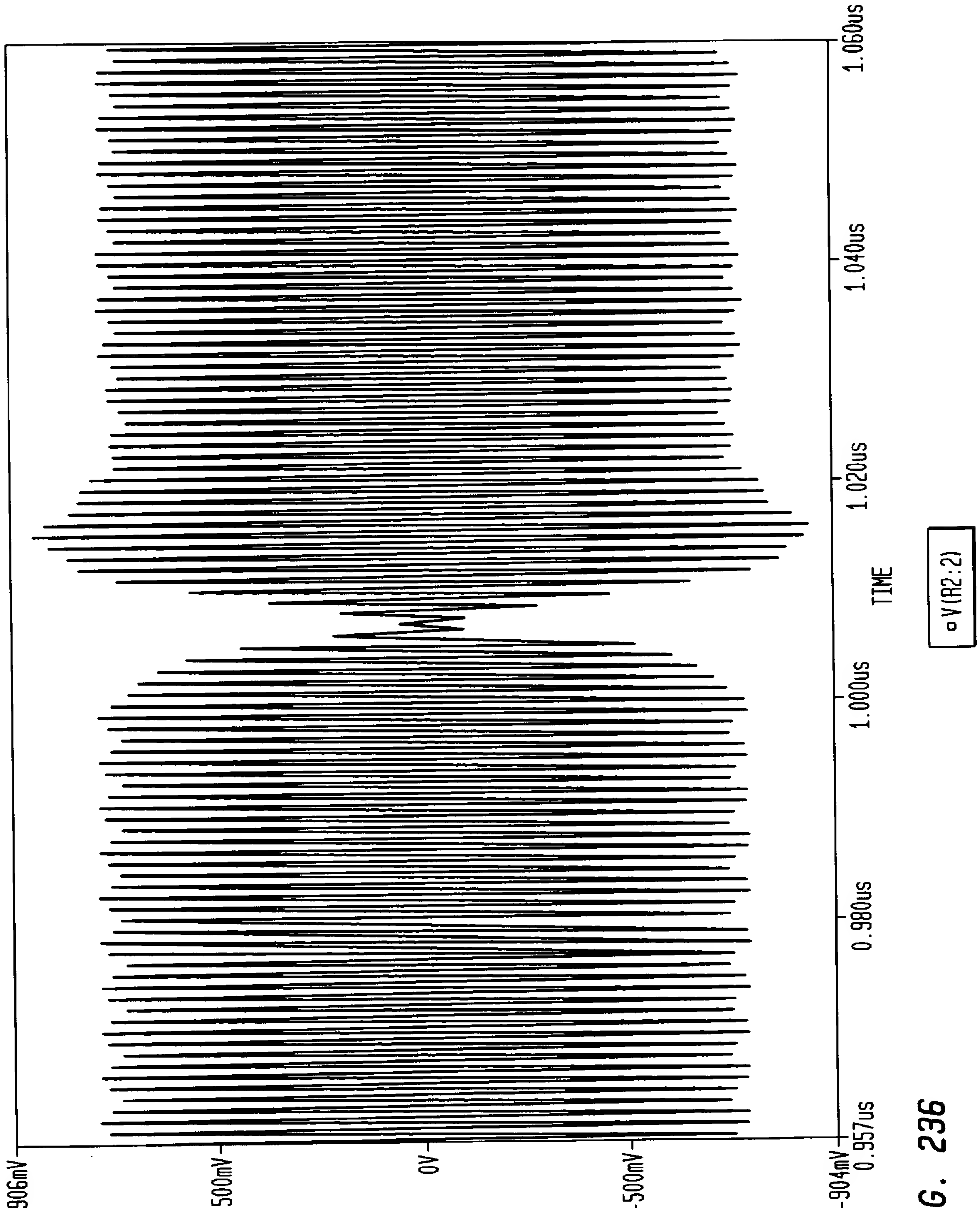

FIG. 236

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Dkt No. 1744.0920001; Group Unit: 2634
Inventors: SORRELLS et al.
Tel. No.: 202-371-2600
For: Method and System for Down-Converting an Electromagnetic Signal, and Transforms for Same

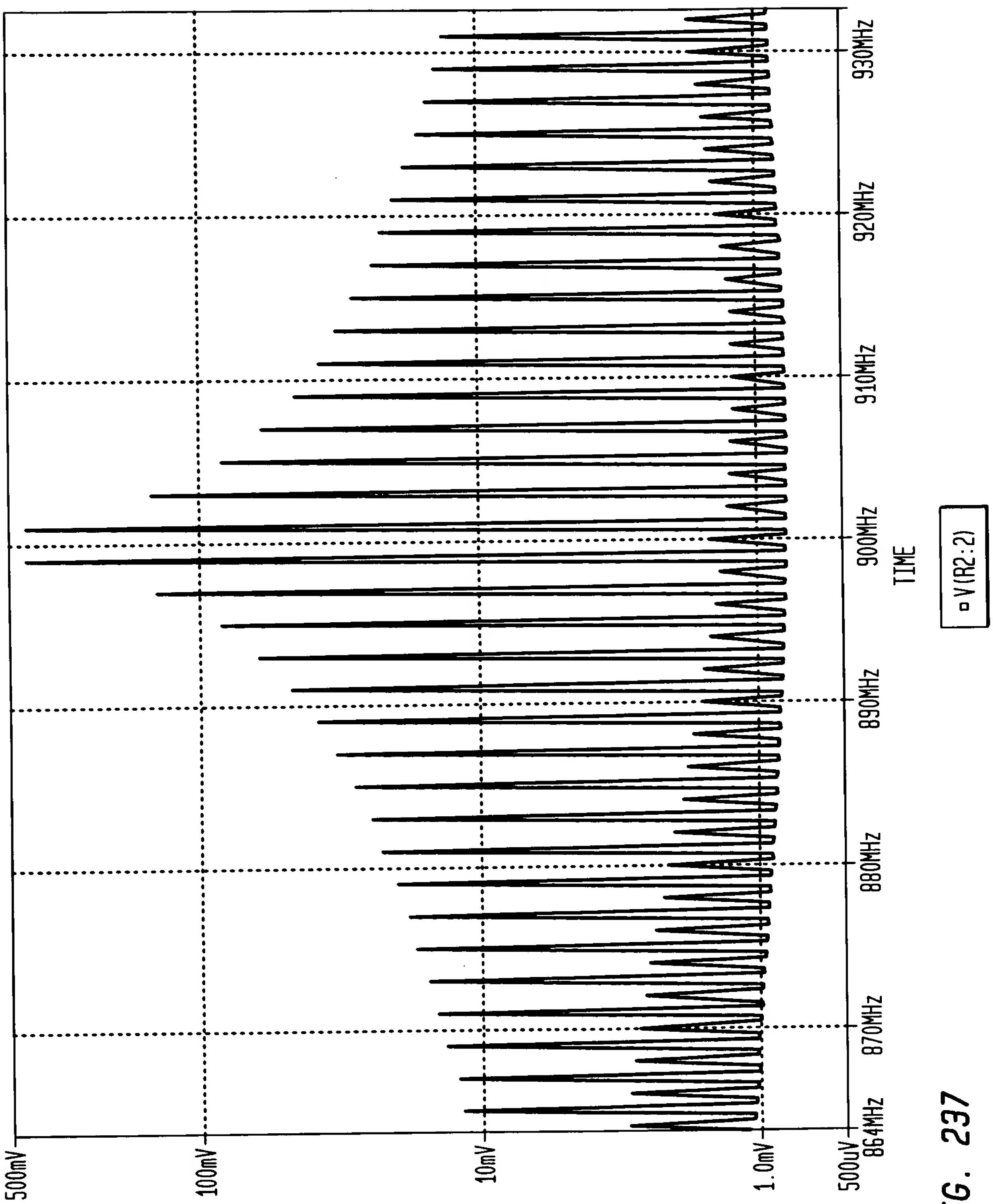


FIG. 237

FIG. 238

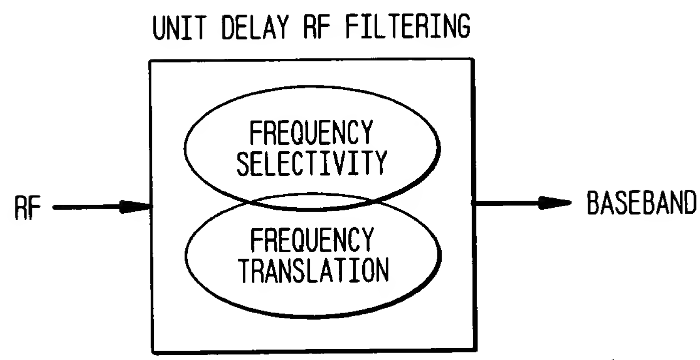


FIG. 239

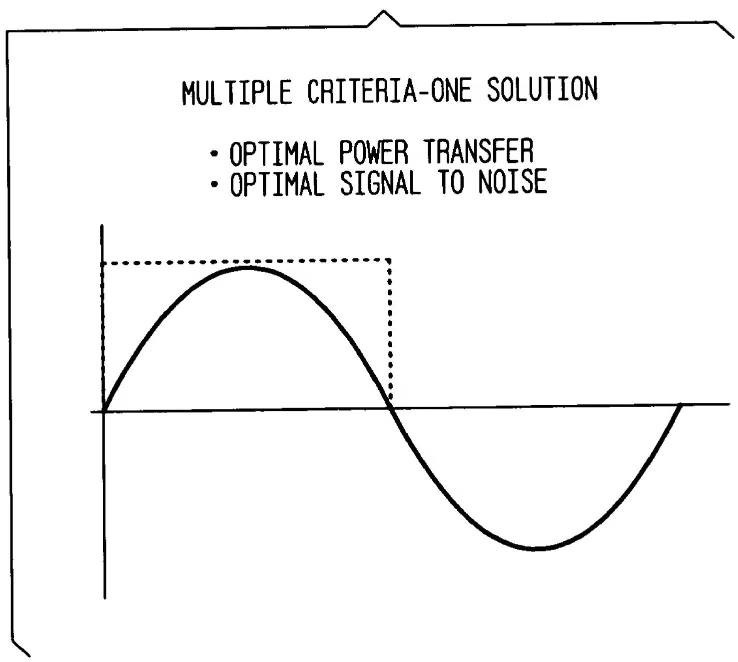


FIG. 240

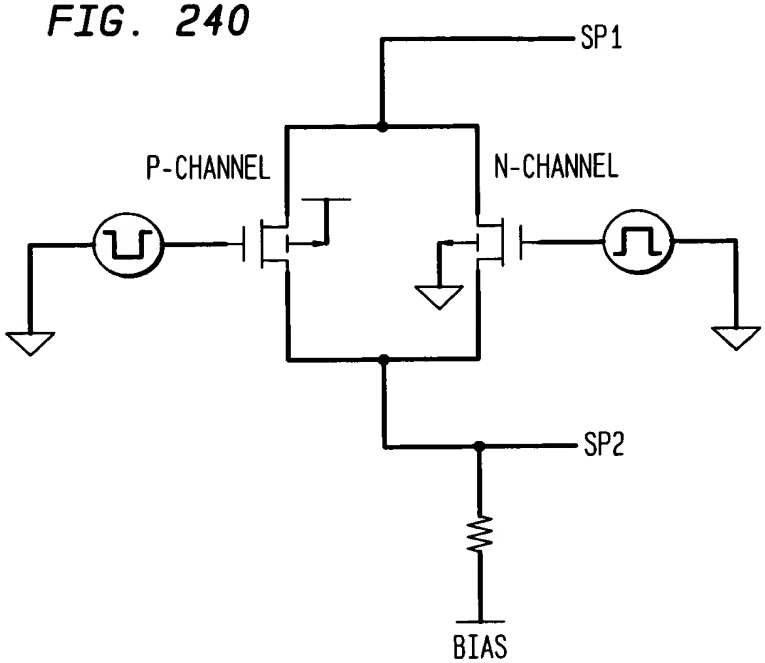


FIG. 241

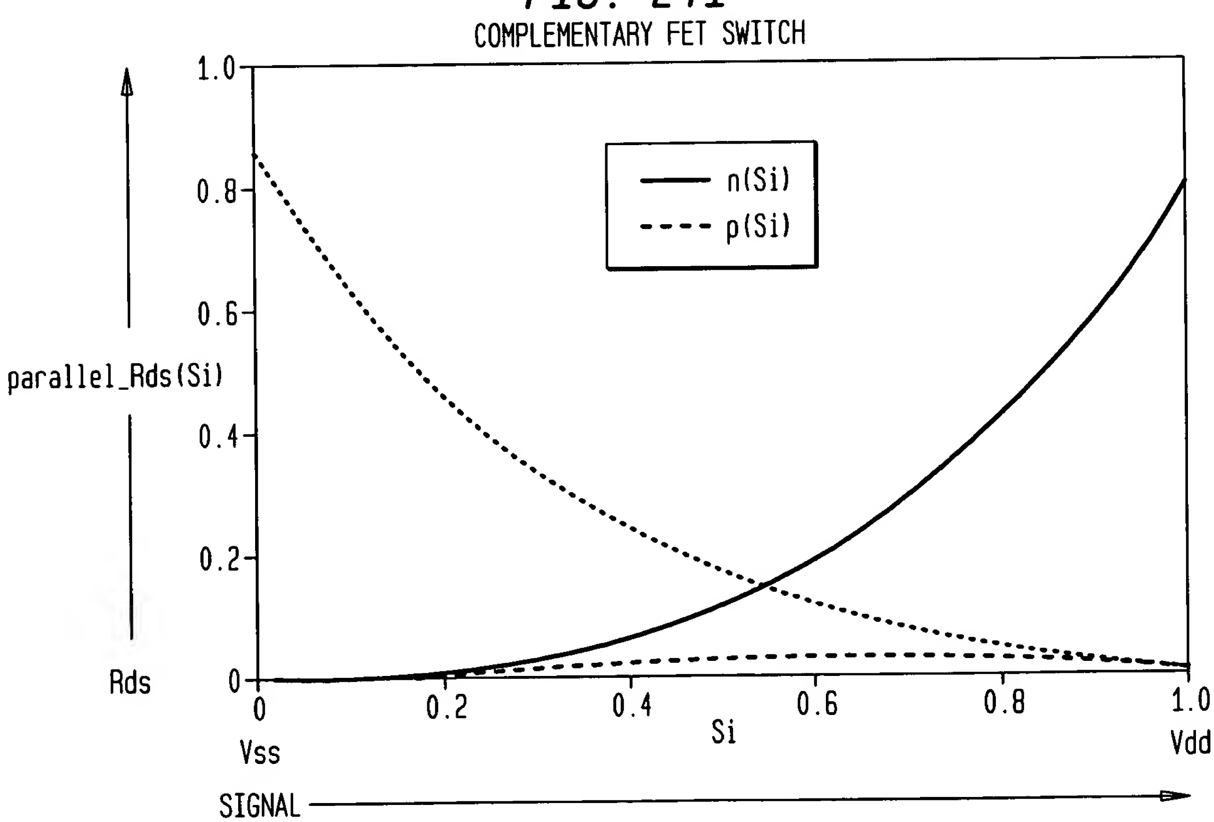
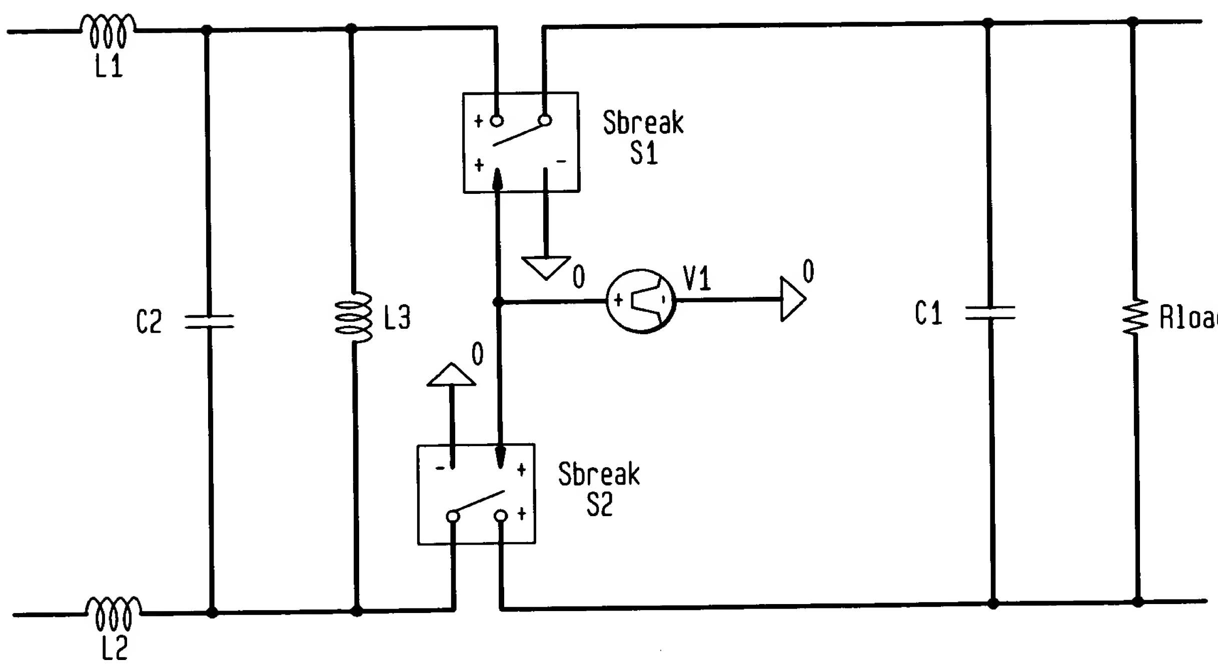


FIG. 242

DIFFERENTIAL CONFIGURATION



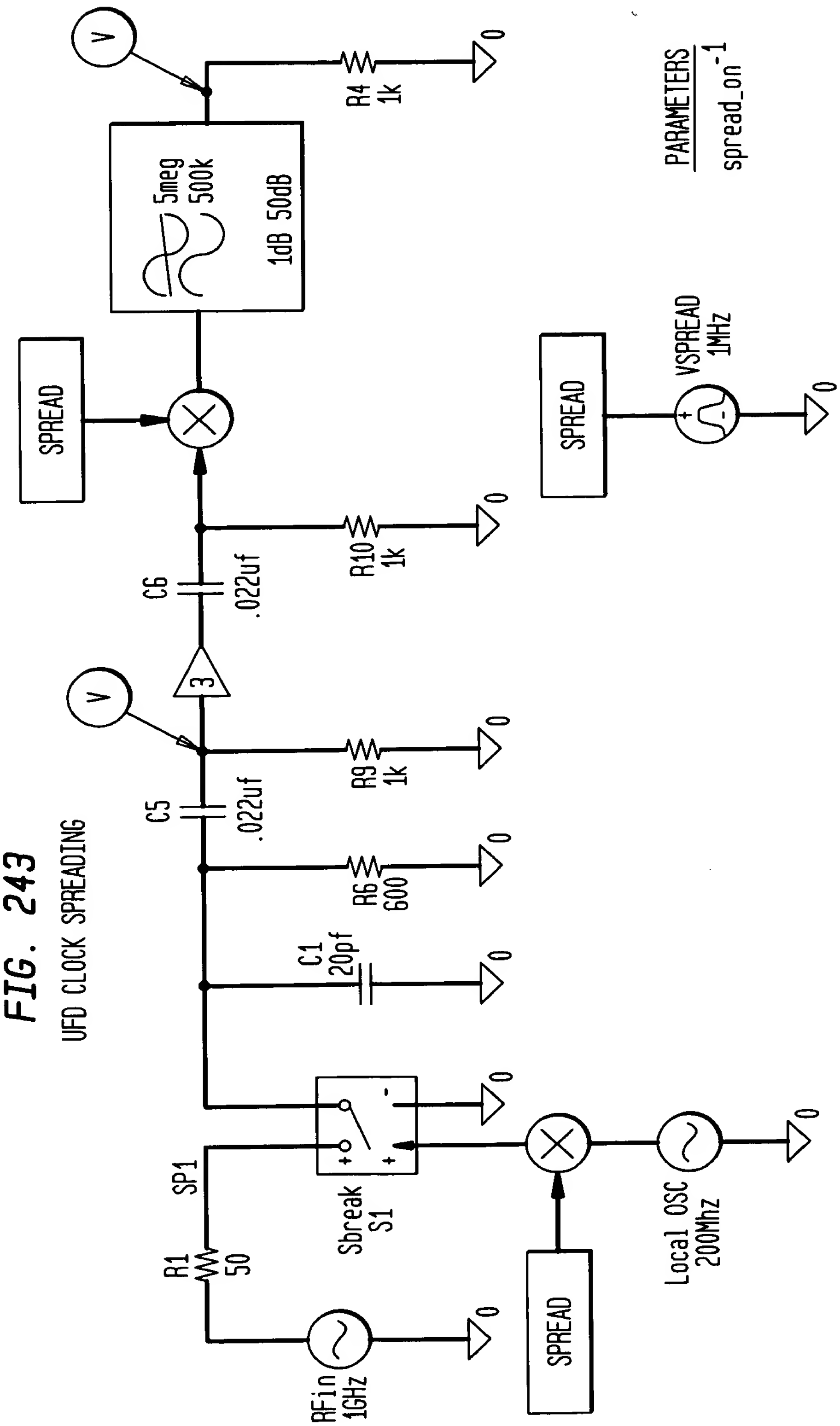


FIG. 243
UFD CLOCK SPREADING

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FIG. 244

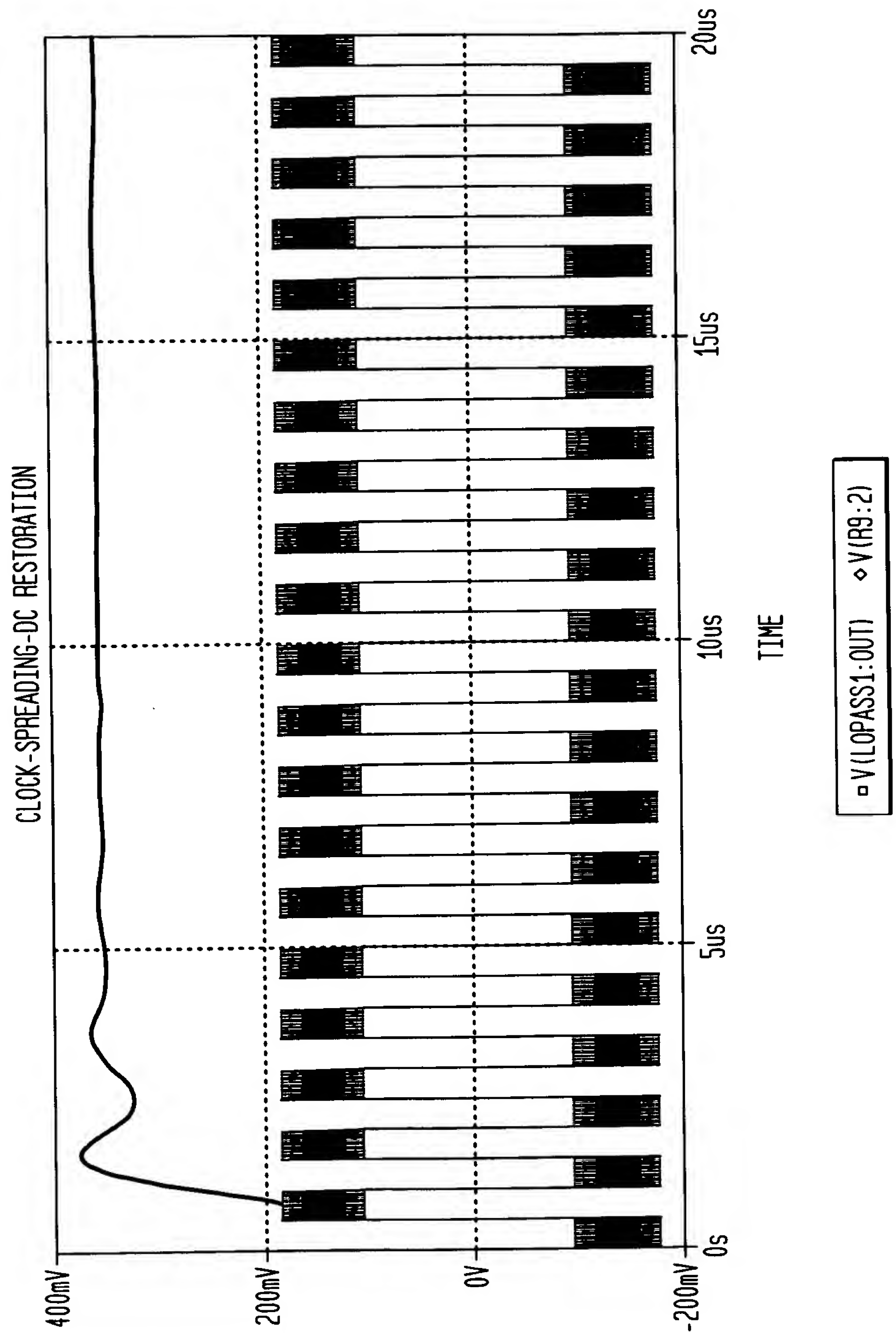

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FIG. 245

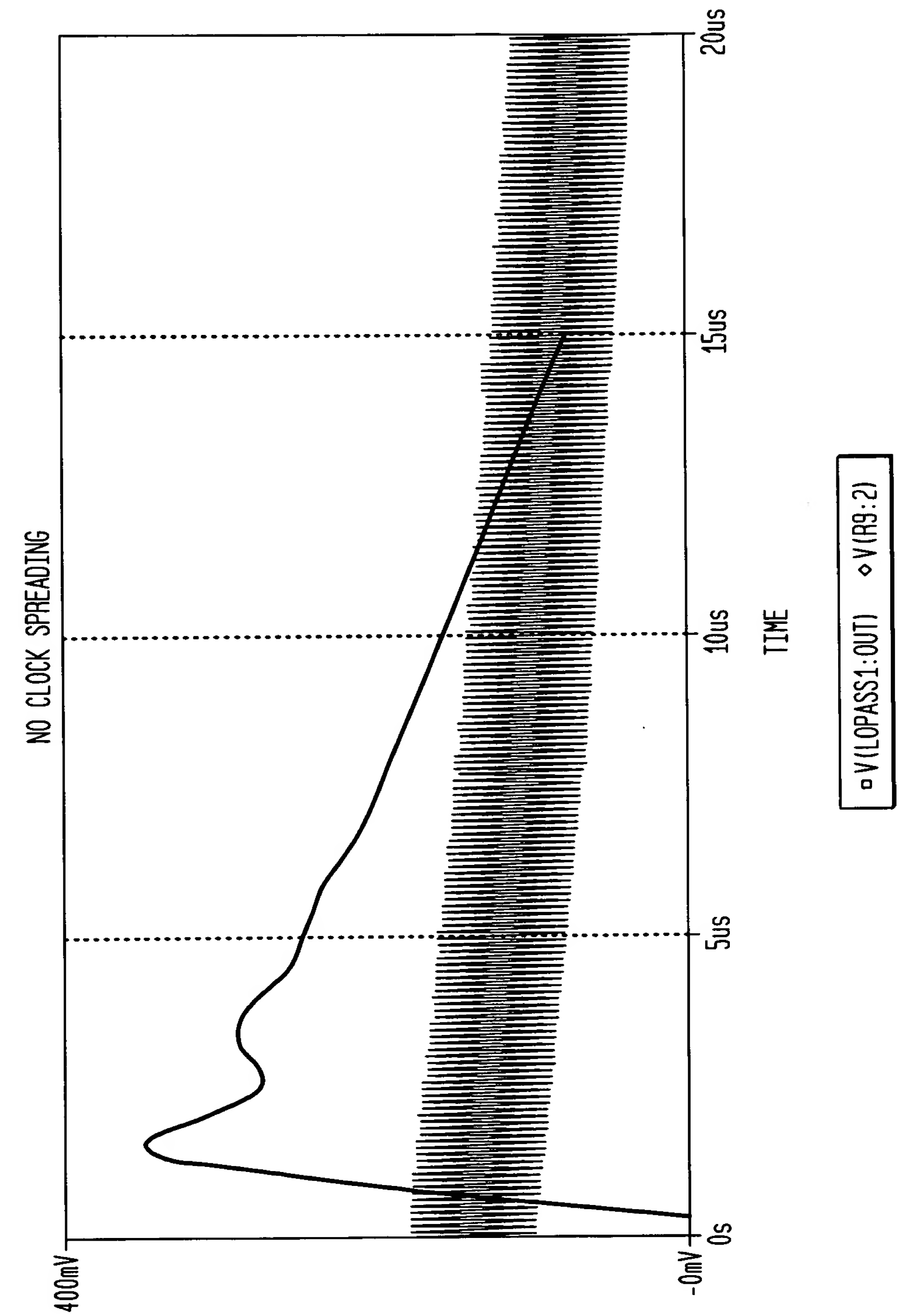

FIG. 246

B.B. RECOVERED I/Q WAVEFORMS WITH SLIGHTLY OFFSET CLOCK (CARRIER)

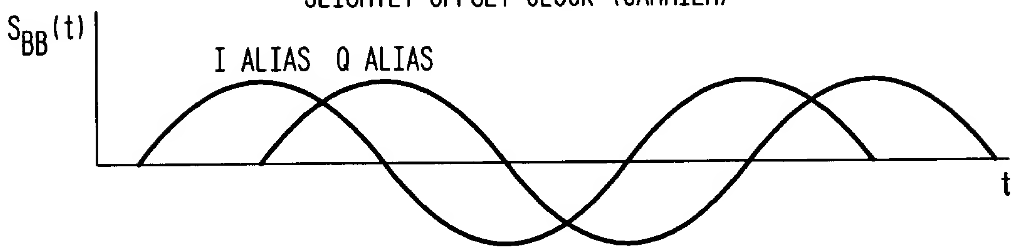

FIG. 247

CMOS IMPLEMENTATION BLOCK DIAGRAM

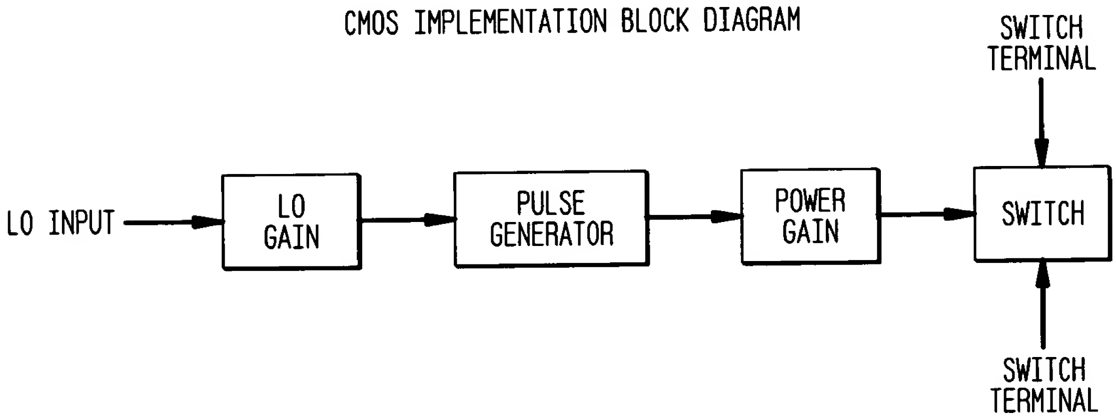

FIG. 248

LO GAIN BLOCK AT GATE LEVEL

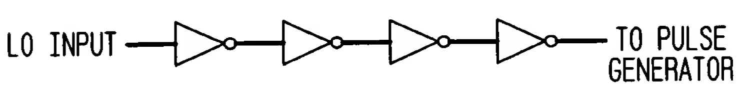

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FIG. 249

LO GAIN BLOCK AT TRANSISTOR LEVEL

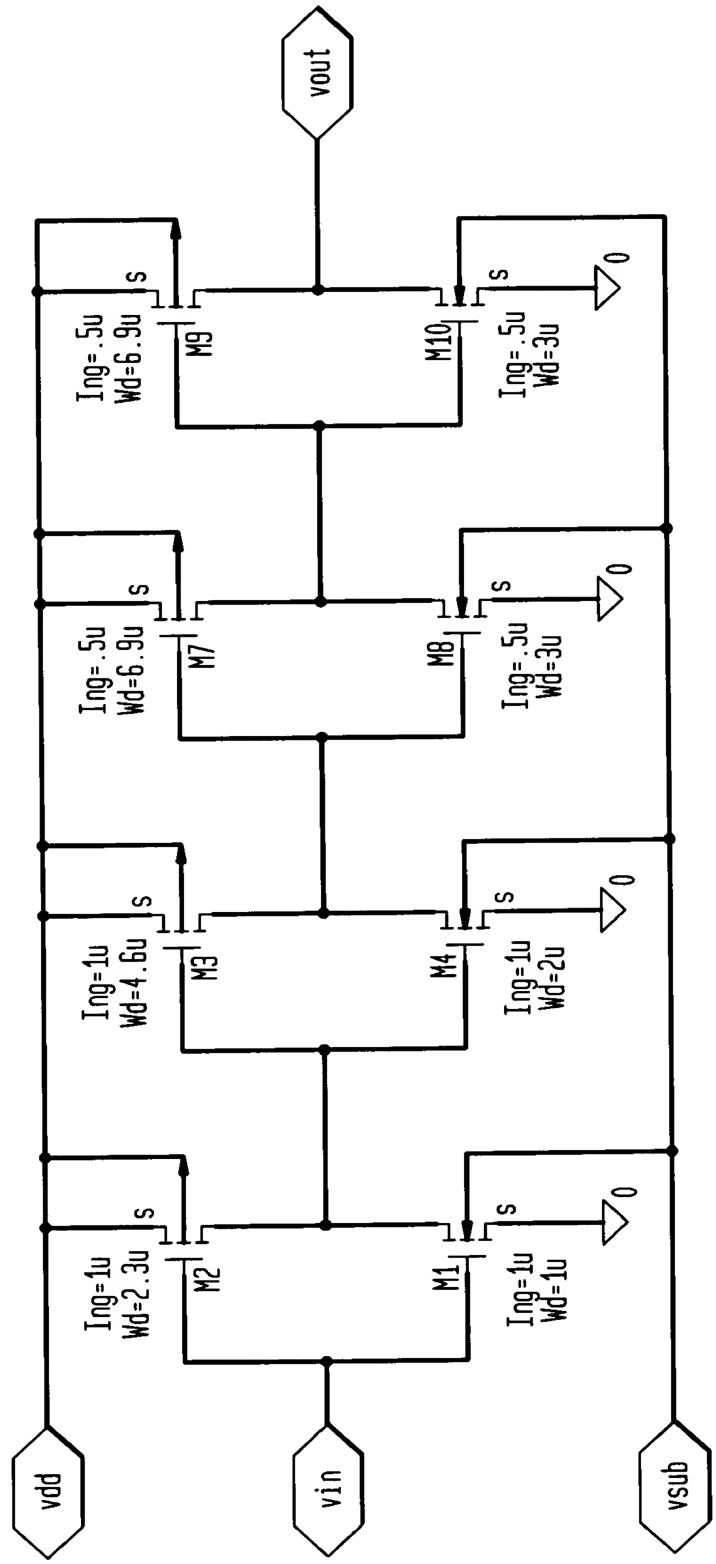

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FIG. 250

PULSE GENERATOR#1 AT GATE LEVEL

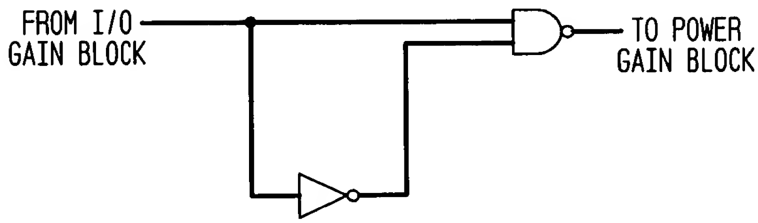

FIG. 251

PULSE GENERATOR#1 AT TRANSISTOR LEVEL

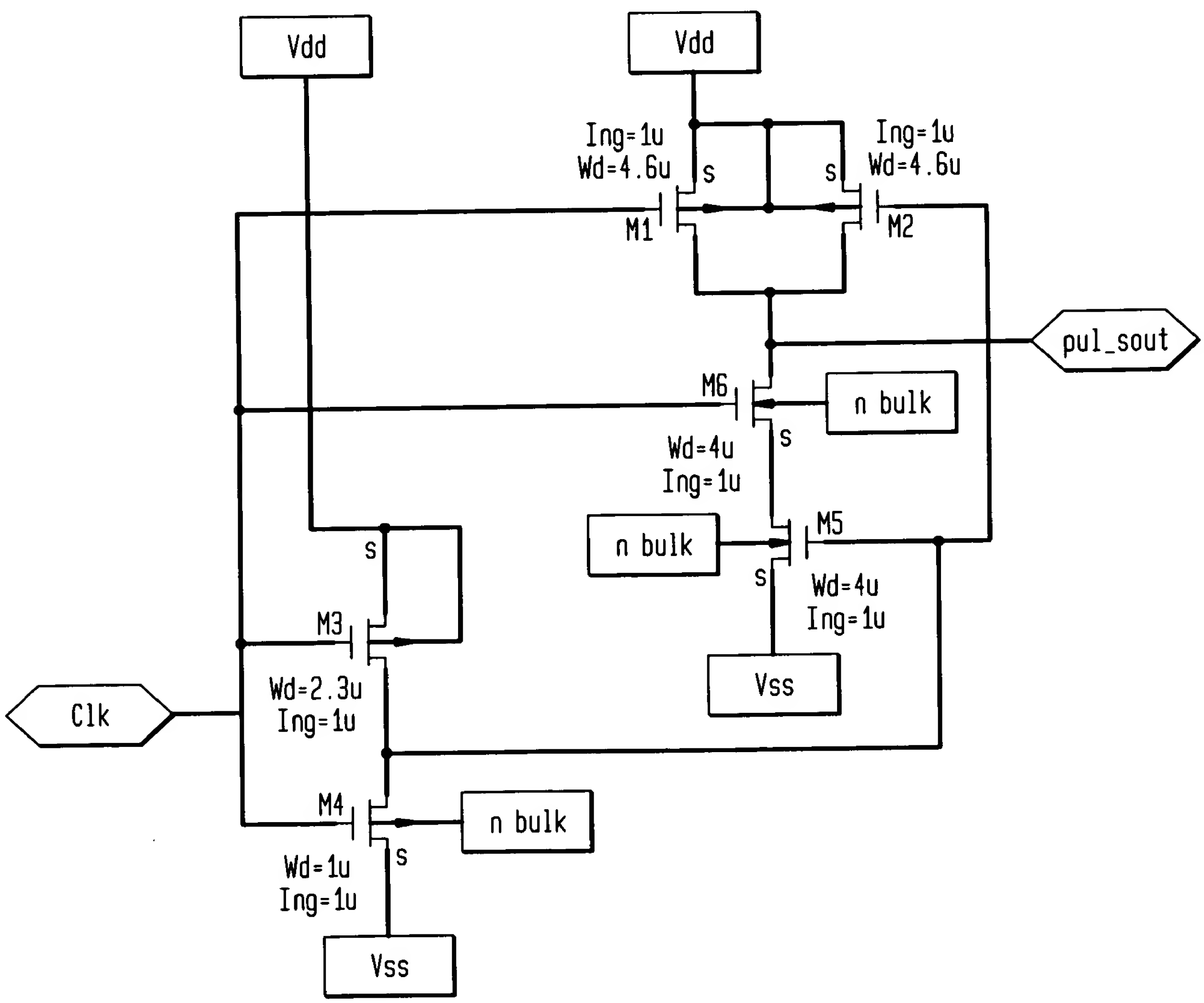

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FIG. 252

POWER GAIN BLOCK AT GATE LEVEL

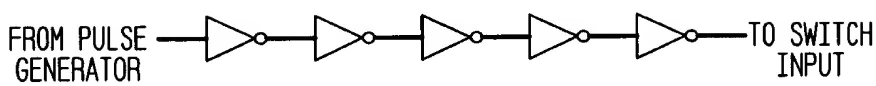

FIG. 253

POWER GAIN BLOCK AT TRANSISTOR LEVEL

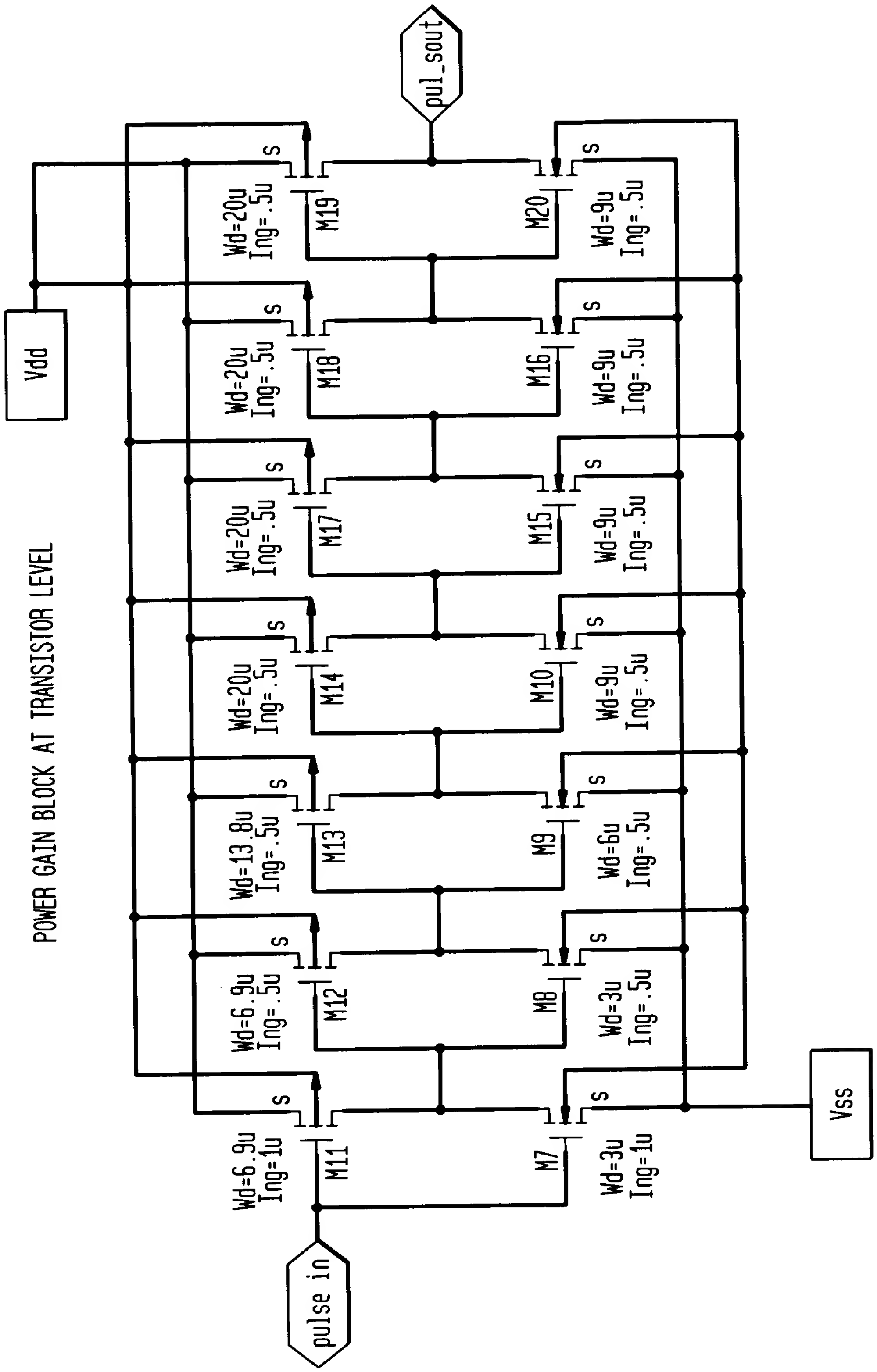

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FIG. 254

SWITCH AT TRANSISTOR LEVEL

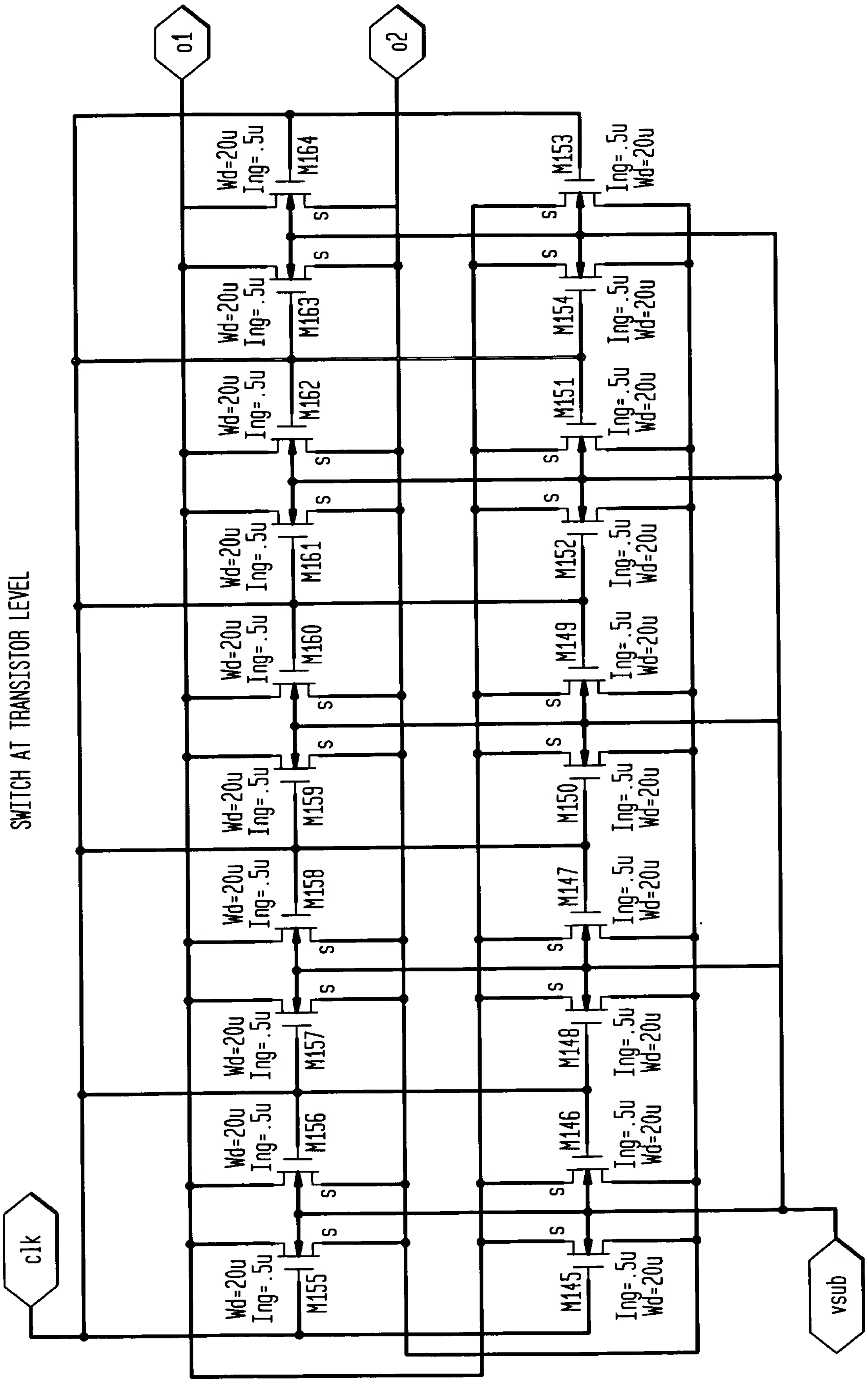

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FIG. 255

CMOS "HOT CLOCK" BLOCK DIAGRAM

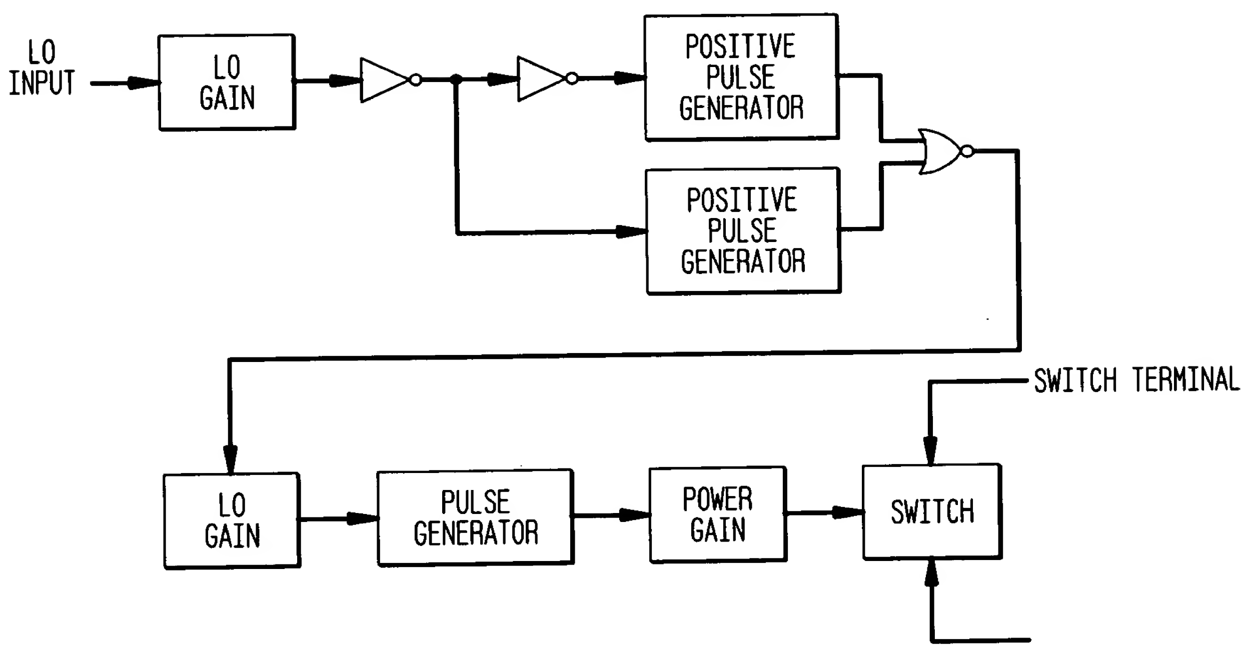

FIG. 256

POSITIVE PULSE GENERATOR AT GATE LEVEL

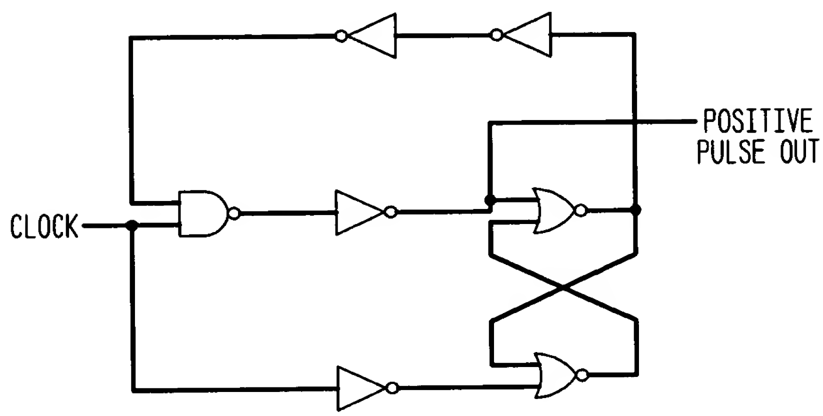

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FIG. 257
POSITIVE PULSER AT TRANSISTOR LEVEL

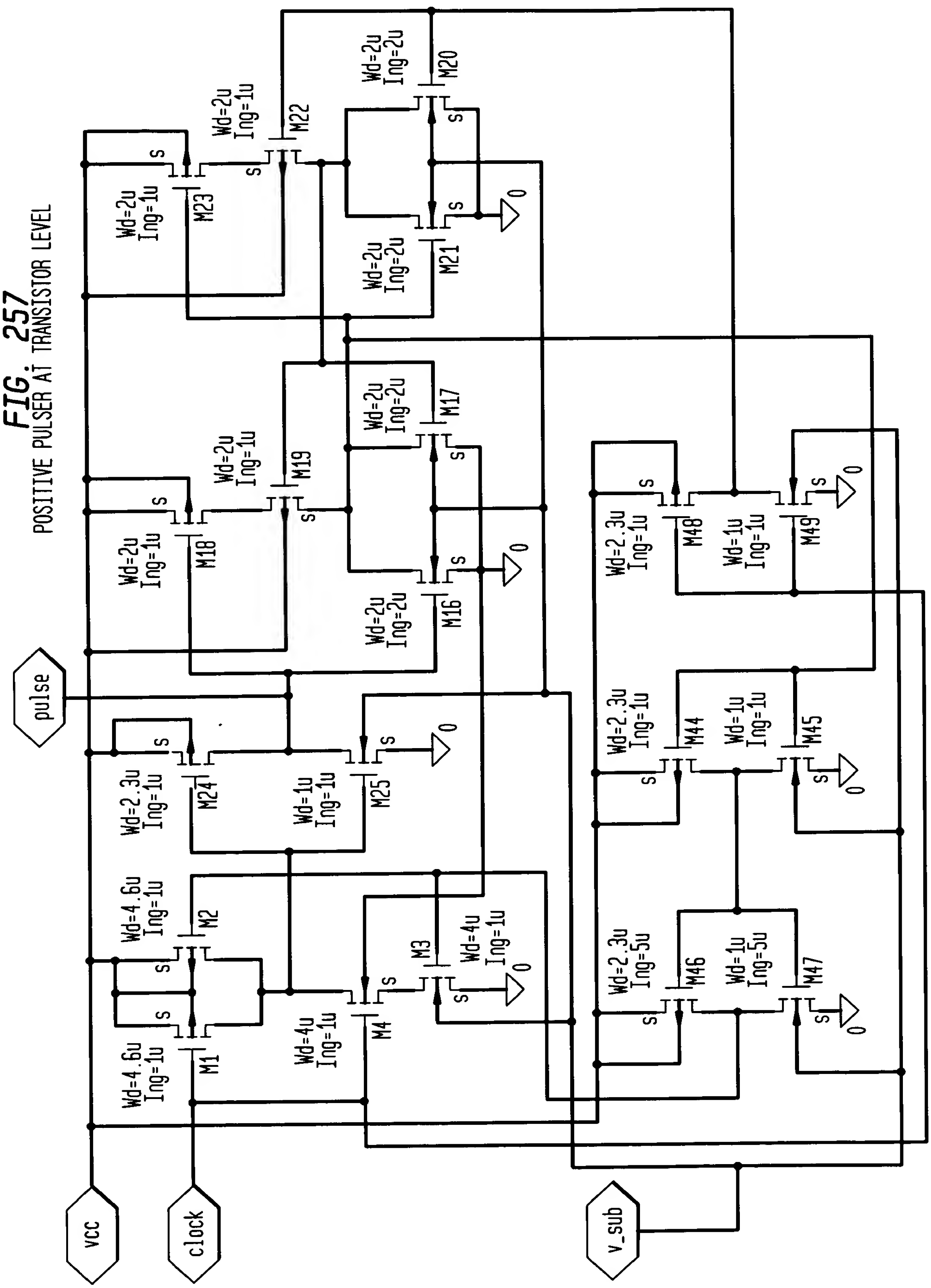

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FIG. 258

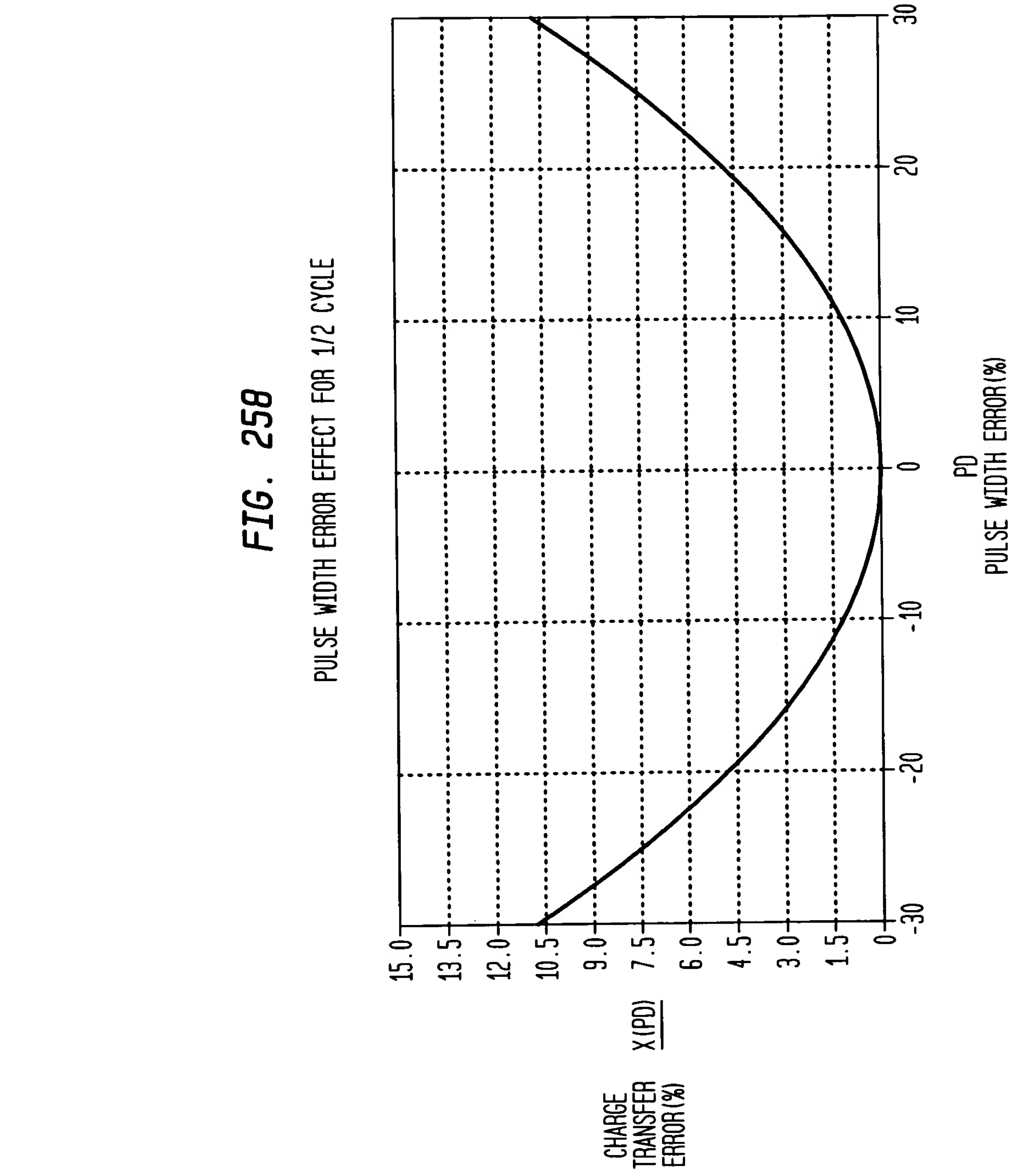
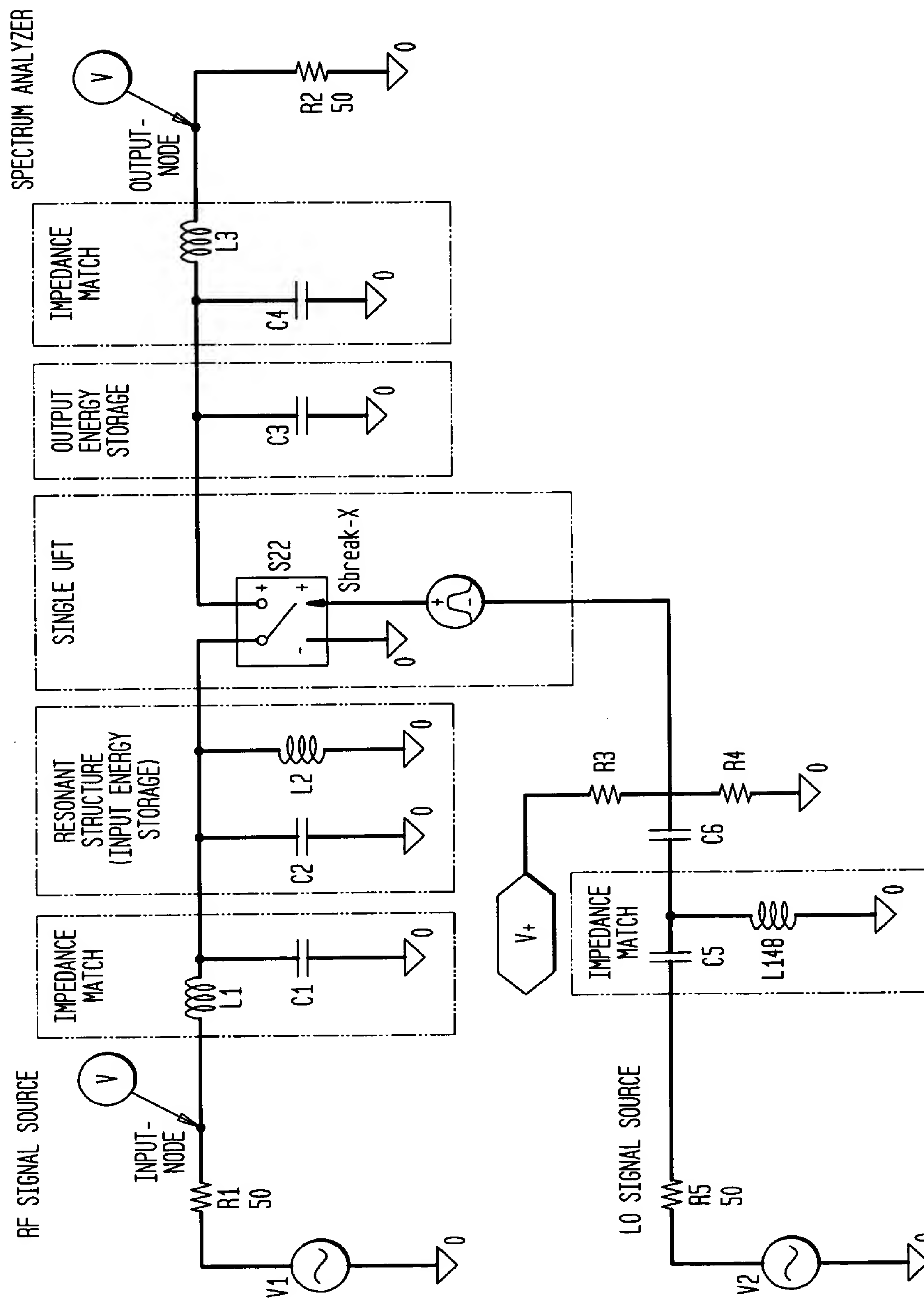


FIG. 259

SINGLE-ENDED UFD MODULE



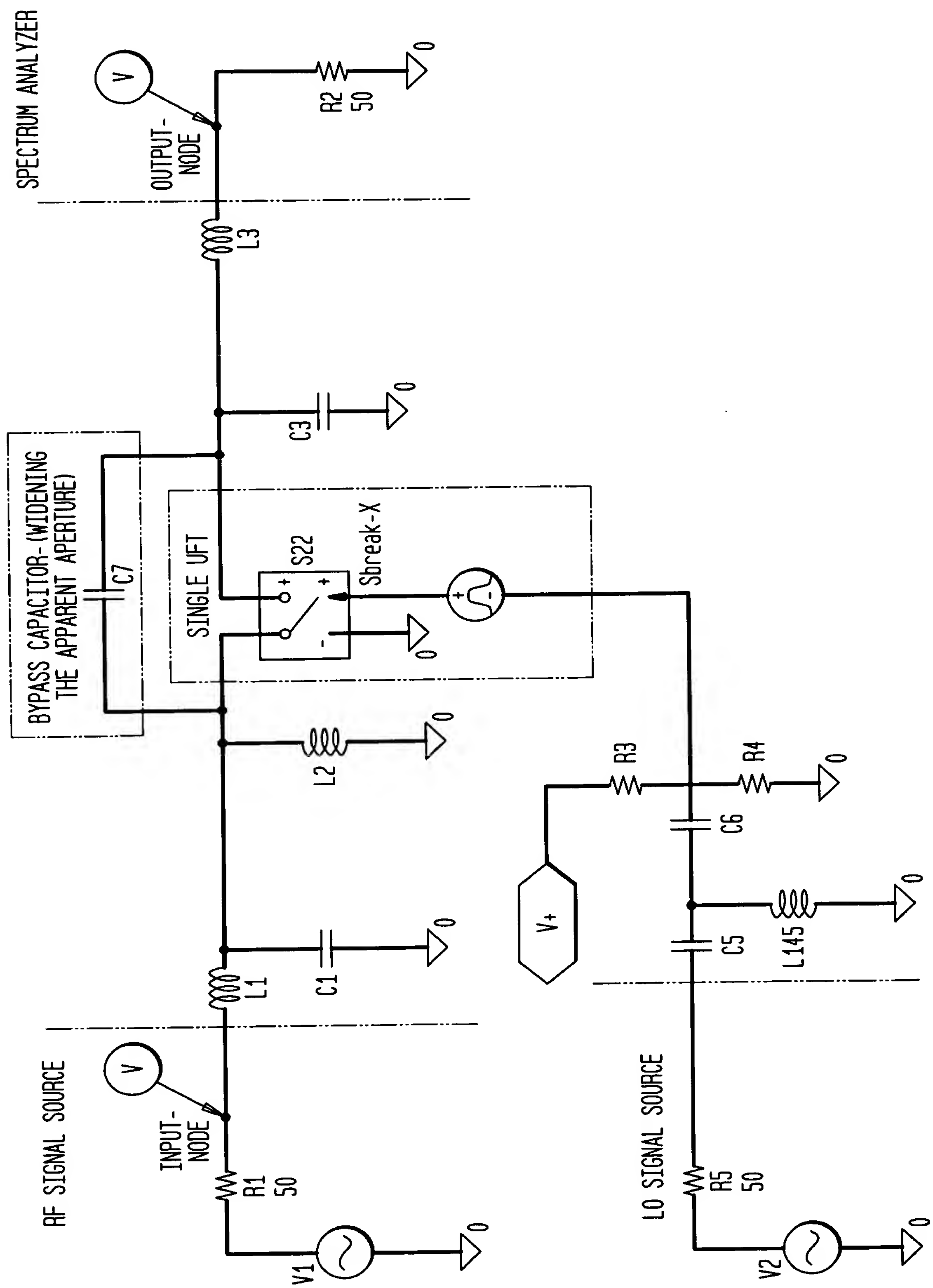
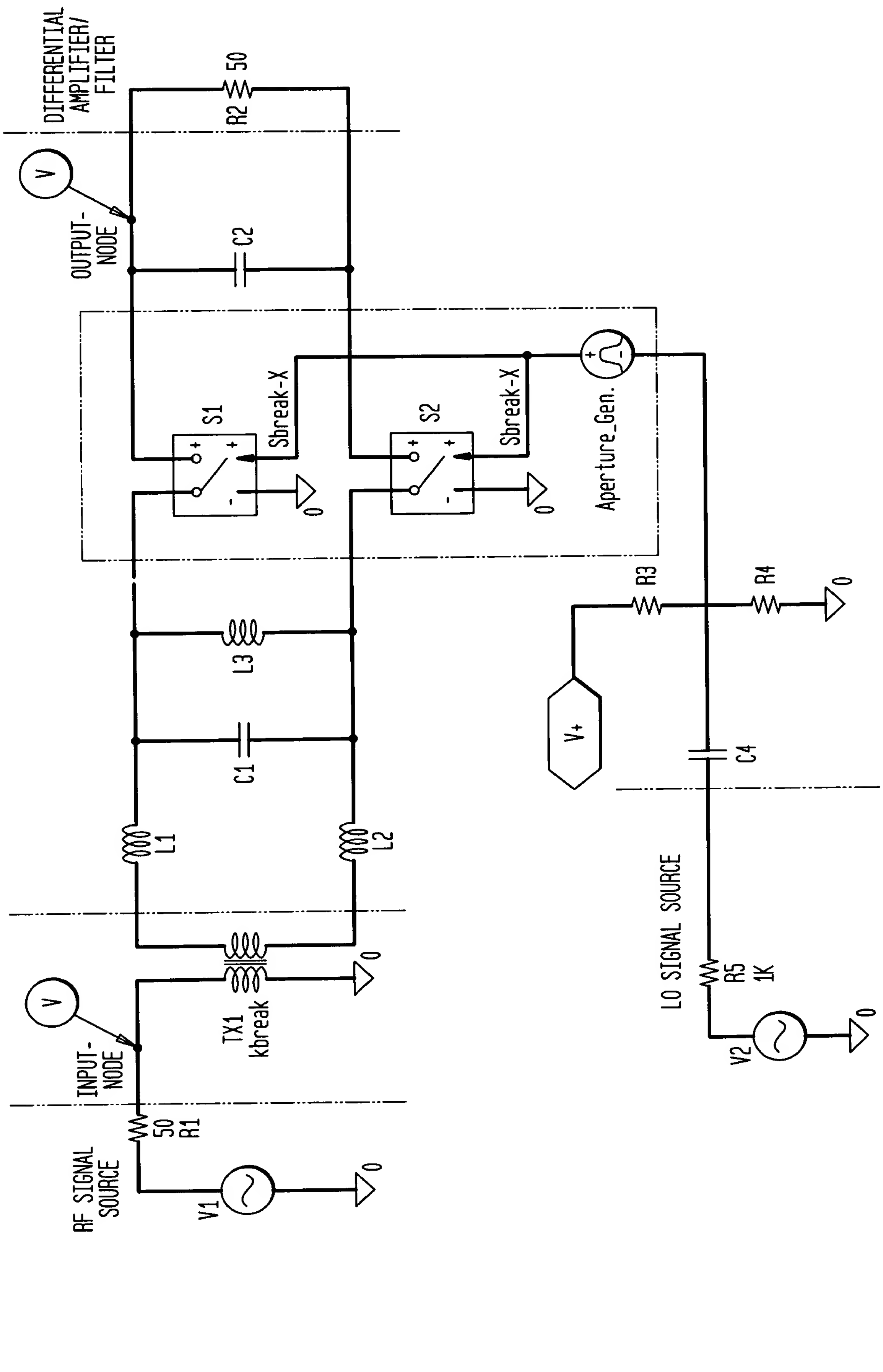


FIG. 260
SINGLE-ENDED UFD MODULE

FIG. 261
FULL DIFFERENTIAL



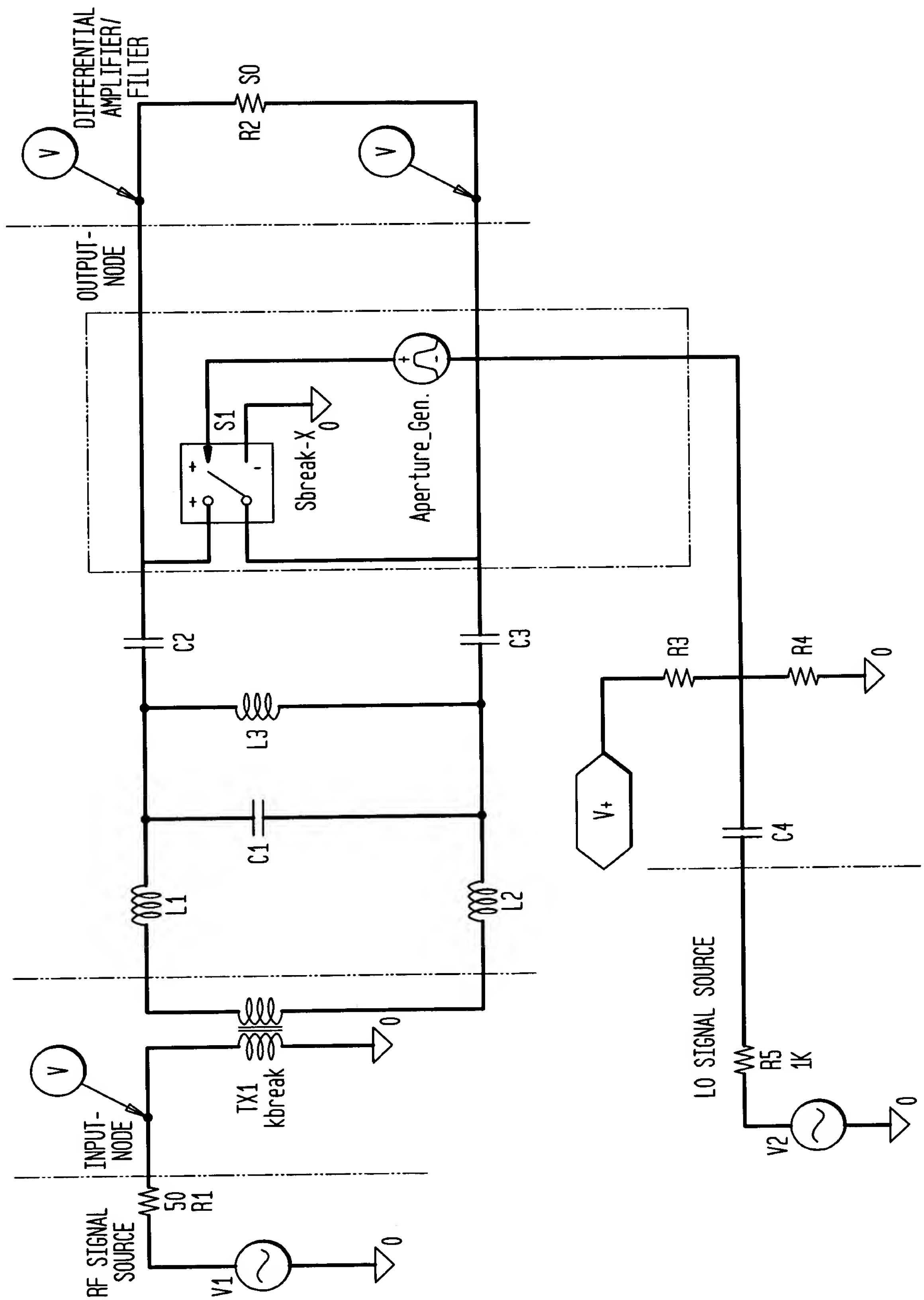


FIG. 262
FULL DIFFERENTIAL

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FIG. 263

SINGLE-ENDED, NEAR IDEAL SIMULATION

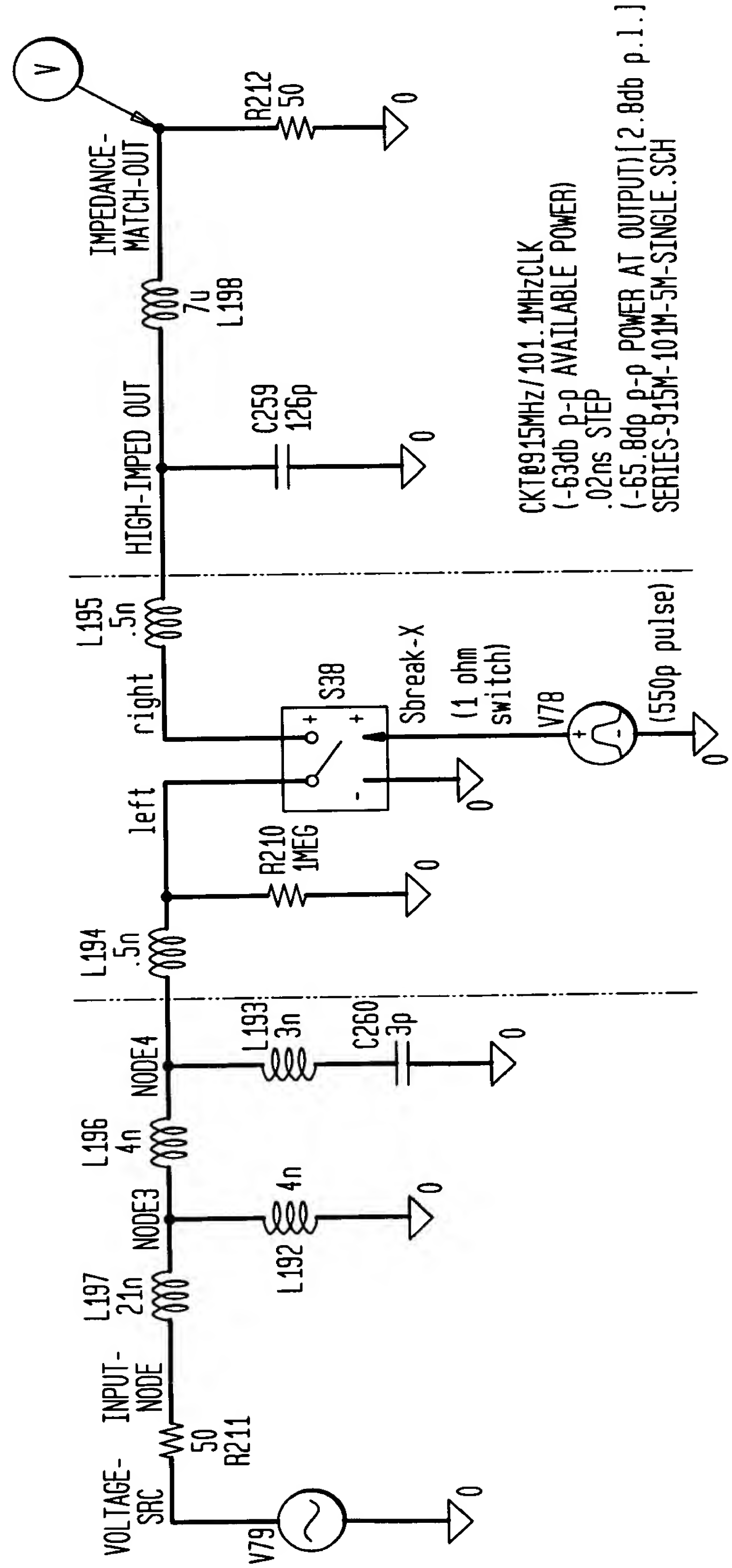

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FIG. 264

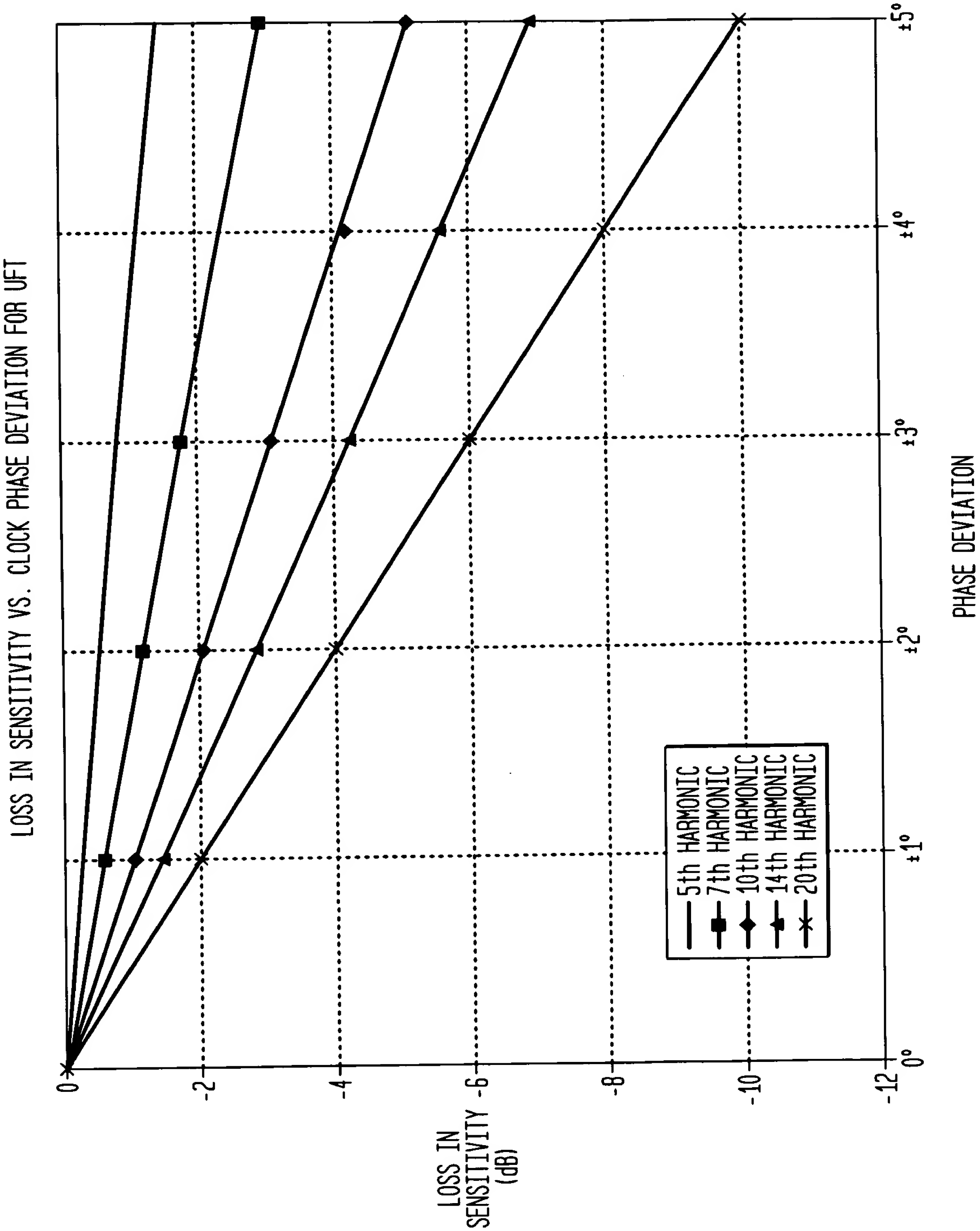

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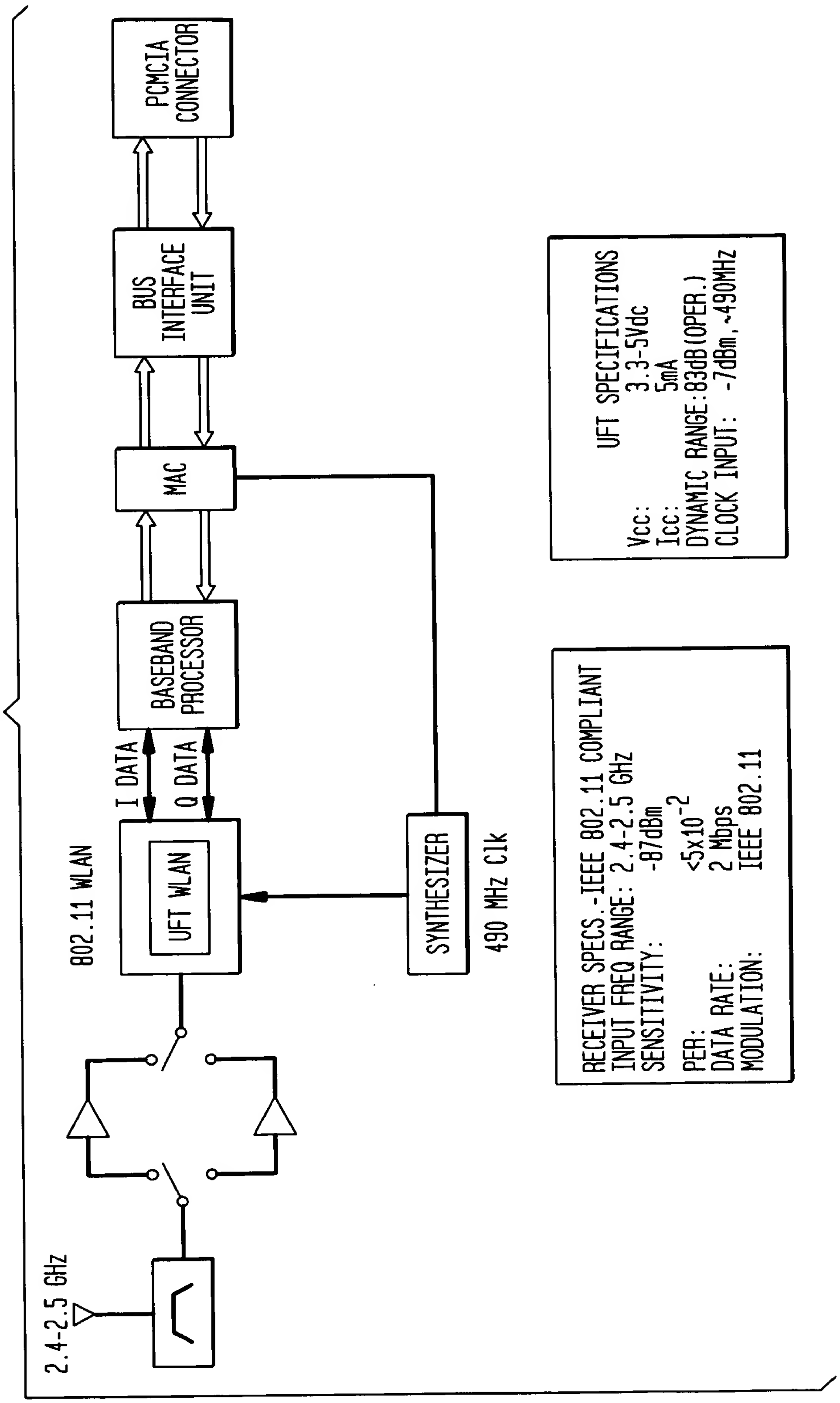
FIG. 265



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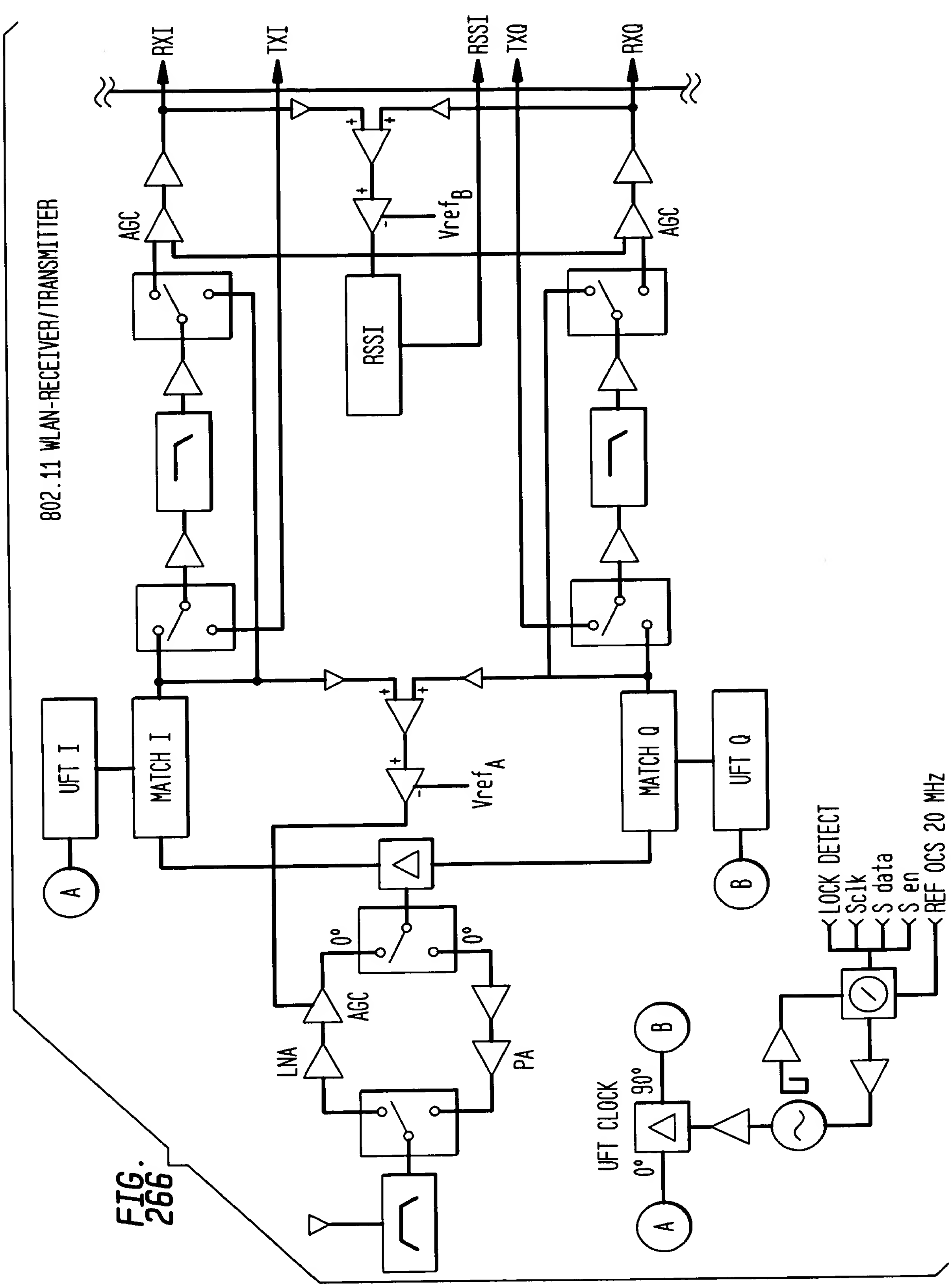

FIG. 266

FIG. 267

PARAMETER	802.11 REQUIREMENT OR INDUSTRY PRACTICE	UFT MODULE BASED RX PERFORMANCE
OPERATING BAND	2.4-2.5 GHz	2.4-2.5 GHz
CHANNELS	2.402 TO 2.495 IN 1 MHz STEPS 2.412 TO 2.484 GHz IN 5 MHz STEPS	2.402 TO 2.495 IN 1 MHz STEPS 2.412 TO 2.484 GHz IN 5 MHz STEPS
MODULATION	BPSK,QPSK,(BARKER,CCK)	BPSK,QPSK
TX SPECTRAL MASK	FIRST SIDELOBE REJECT<-30,+15dBm SECOND SIDELOBE REJECT<-50,+15dBm	-35 dBr,-55dBr
EYE OPENING	Verr<.35 FOR 1000 COMPLEX SAMPLES	<.3
OPERATIONAL DYNAMIC RANGE	76 dB (DERIVED)	83 dB
MAX. INPUT, @, 8% PER	-4 dBm	-4 dBm
SENSITIVITY	-80 dBm @ <8% PER	-87 dBm @ <5% PER
ACQUISITION	802.11 DSS AND FH	802.11 DSS AND FH
IMAGE REJECTION	>80 dB	>80 dB
LO RERADIATION	< -50 dBm	< -50 dBm
ADJACENT CHANNEL REJECTION	> 35 dB @ 30 MHz OFFSET PER <8%	> 35 dB @ 30 MHz OFFSET PER <5%
POWER	3.3,5V 1.5W (RX MODE)	3.3,5V,700mW

FIG. 268

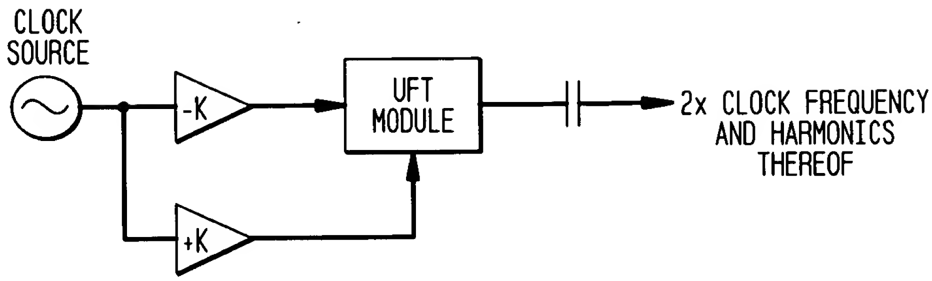

FIG. 269

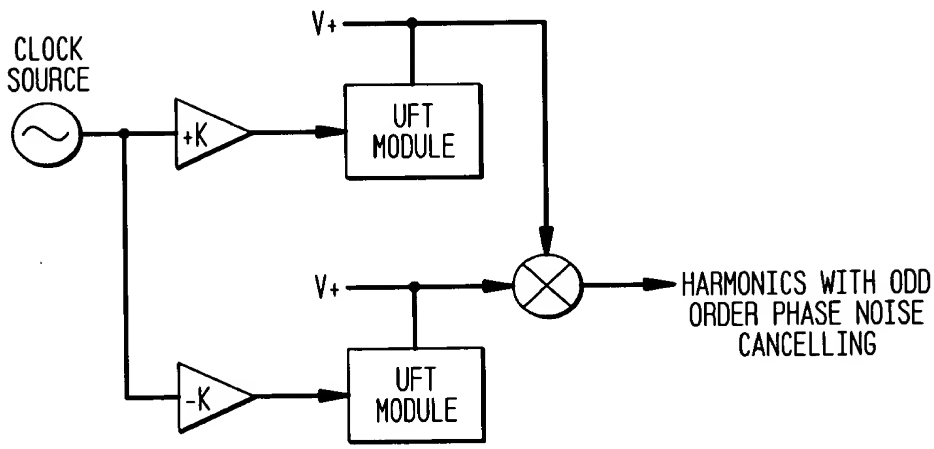

FIG. 270

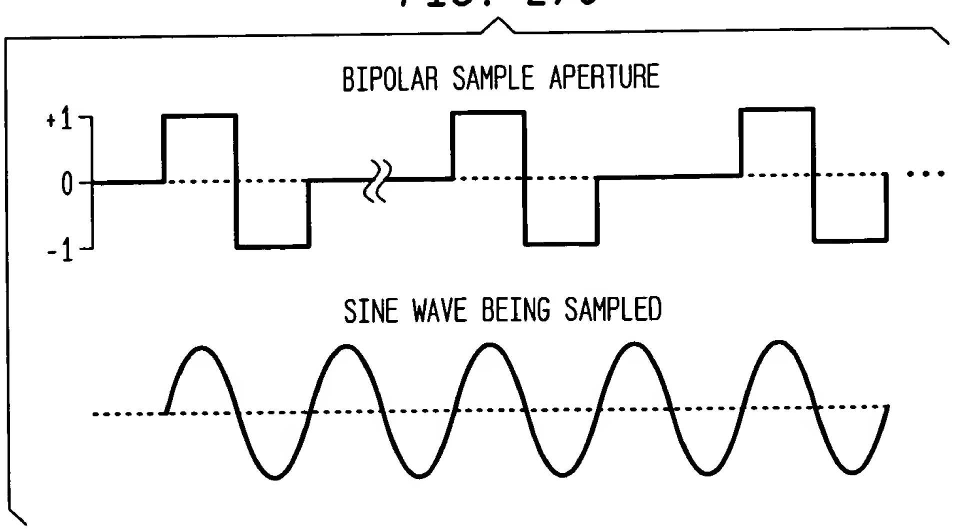

FIG. 271

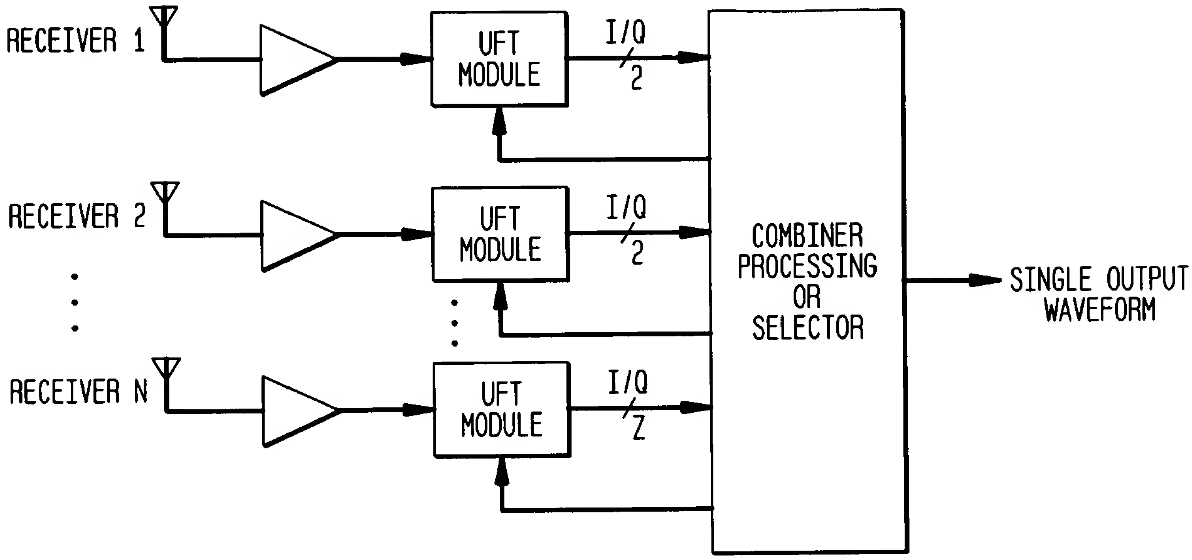

FIG. 272

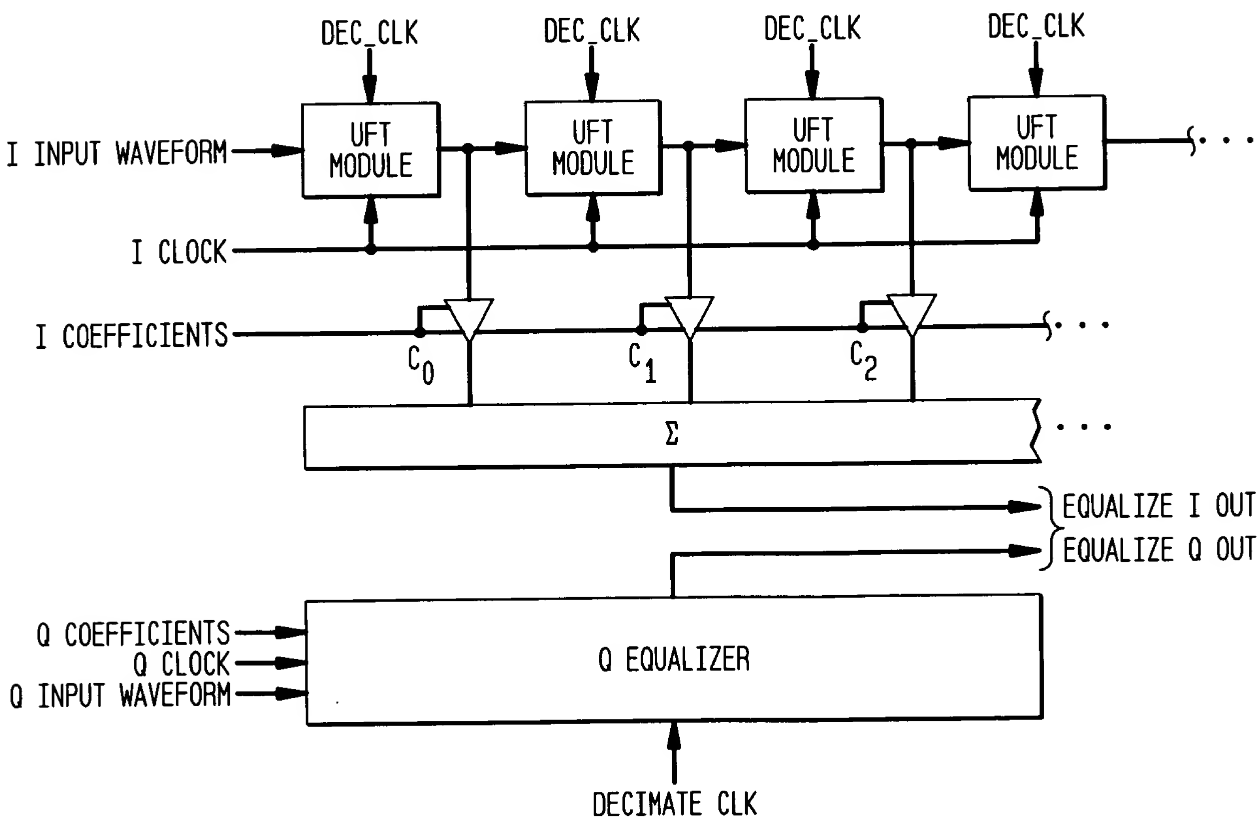

FIG. 273

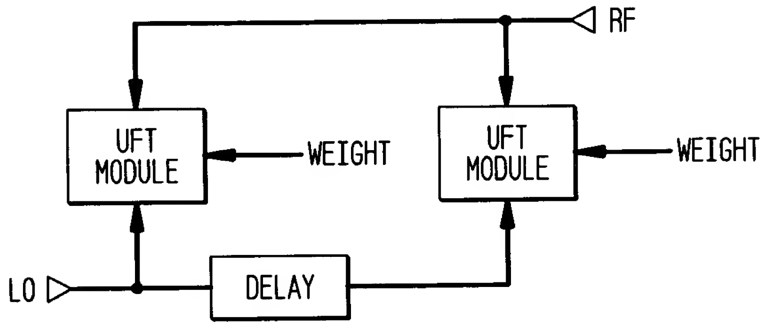

FIG. 274

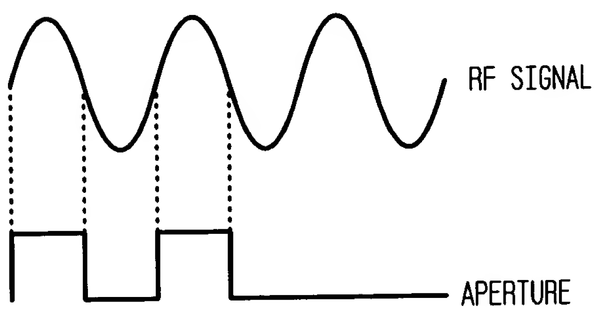

FIG. 275

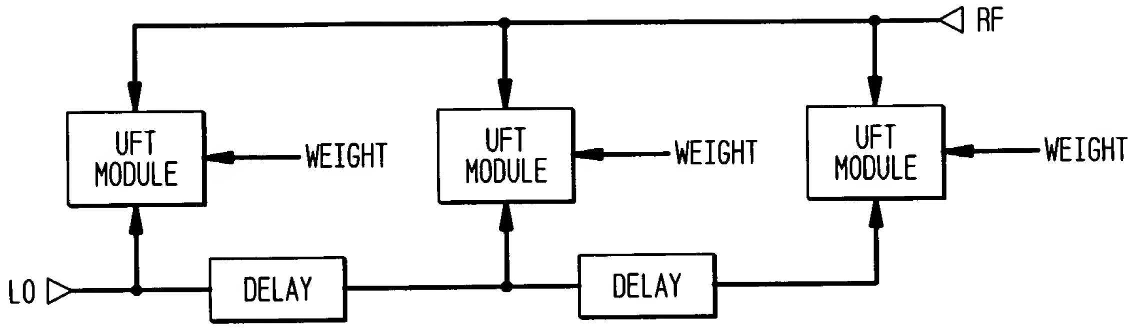

FIG. 276

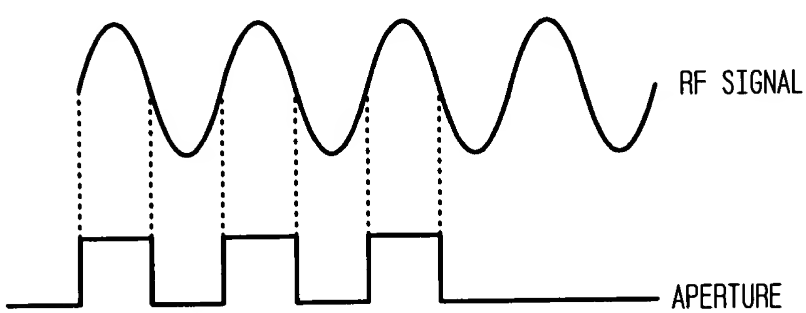

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FIG. 277

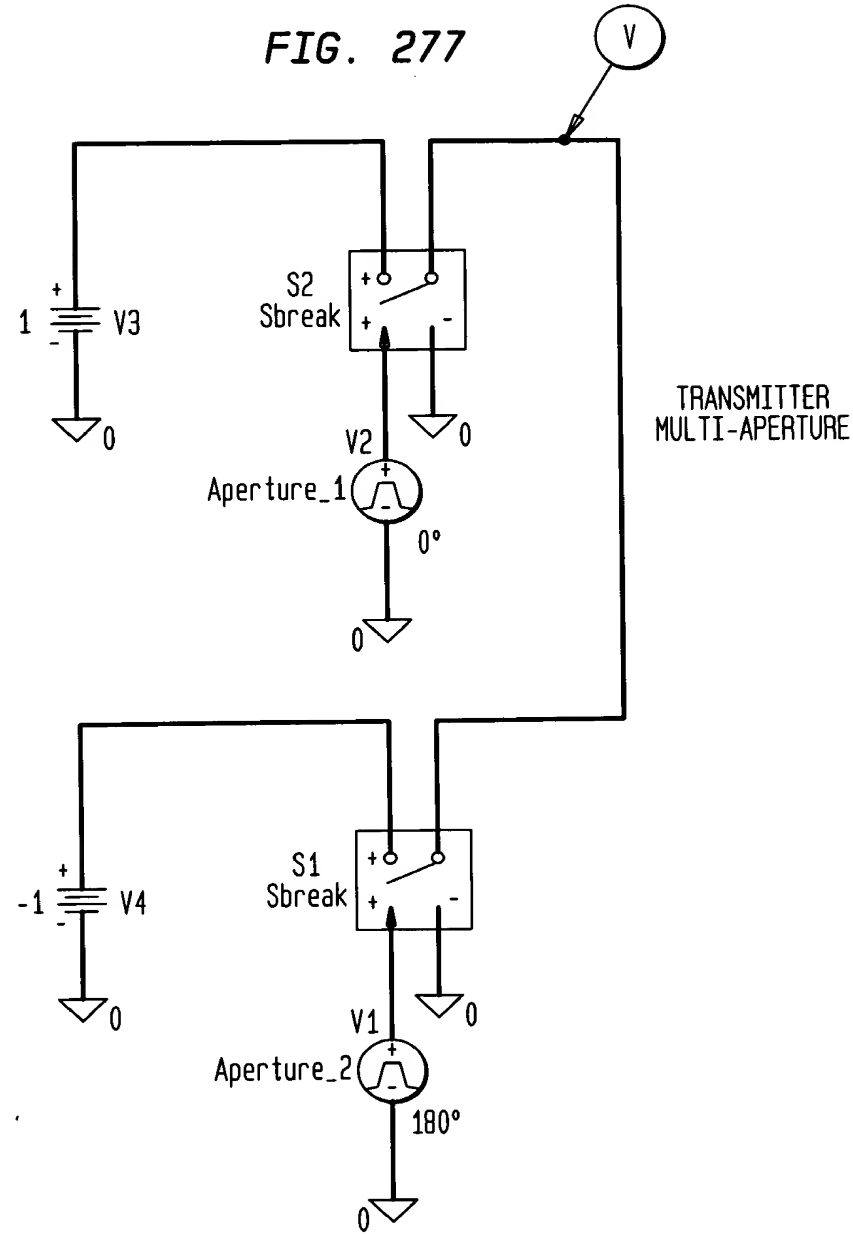

FIG. 278

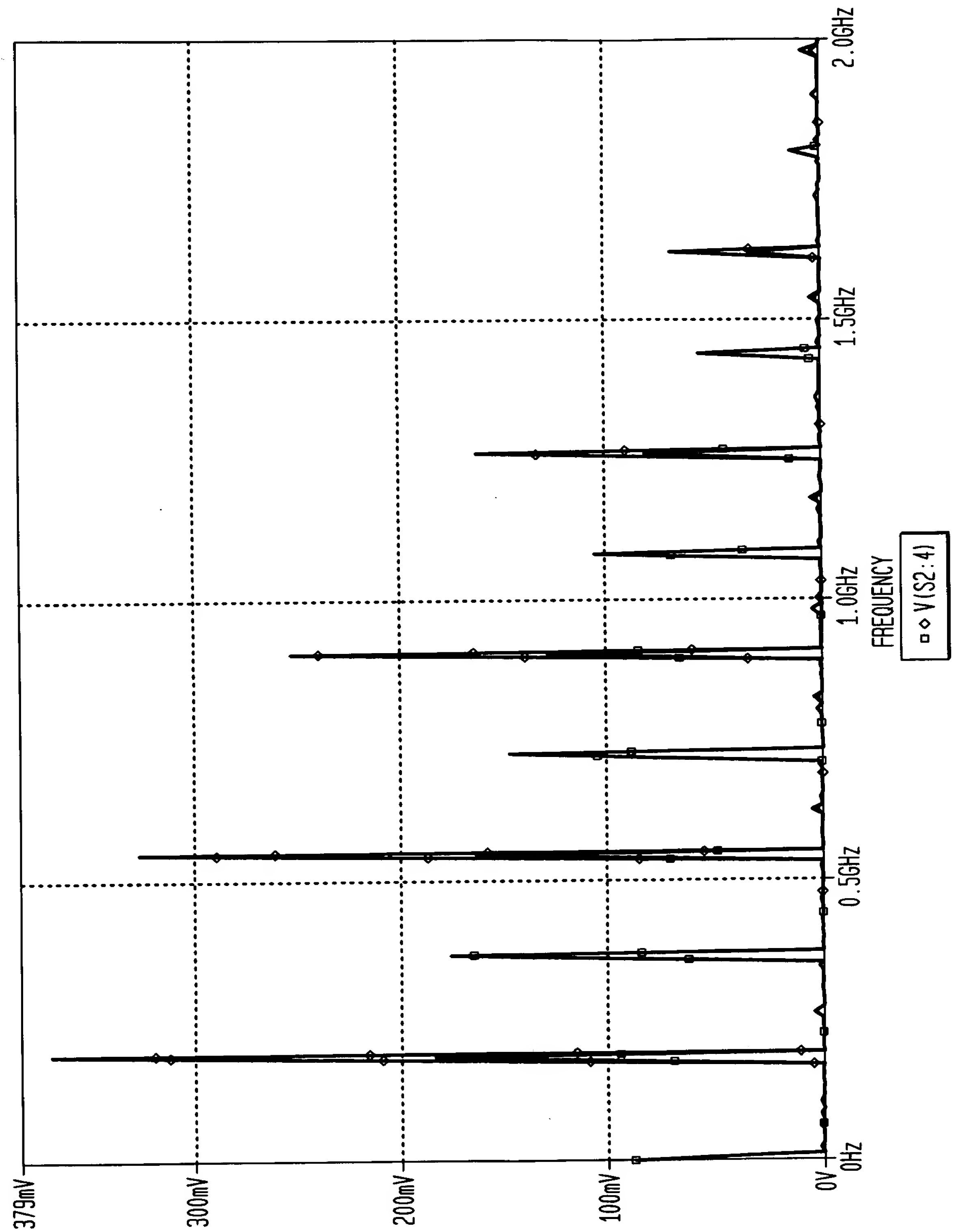
379mV
300mV
200mV
100mV
0V
0Hz
0.5GHz
1.0GHz
1.5GHz
2.0GHz
FREQUENCY
V(S2:4)

FIG. 279

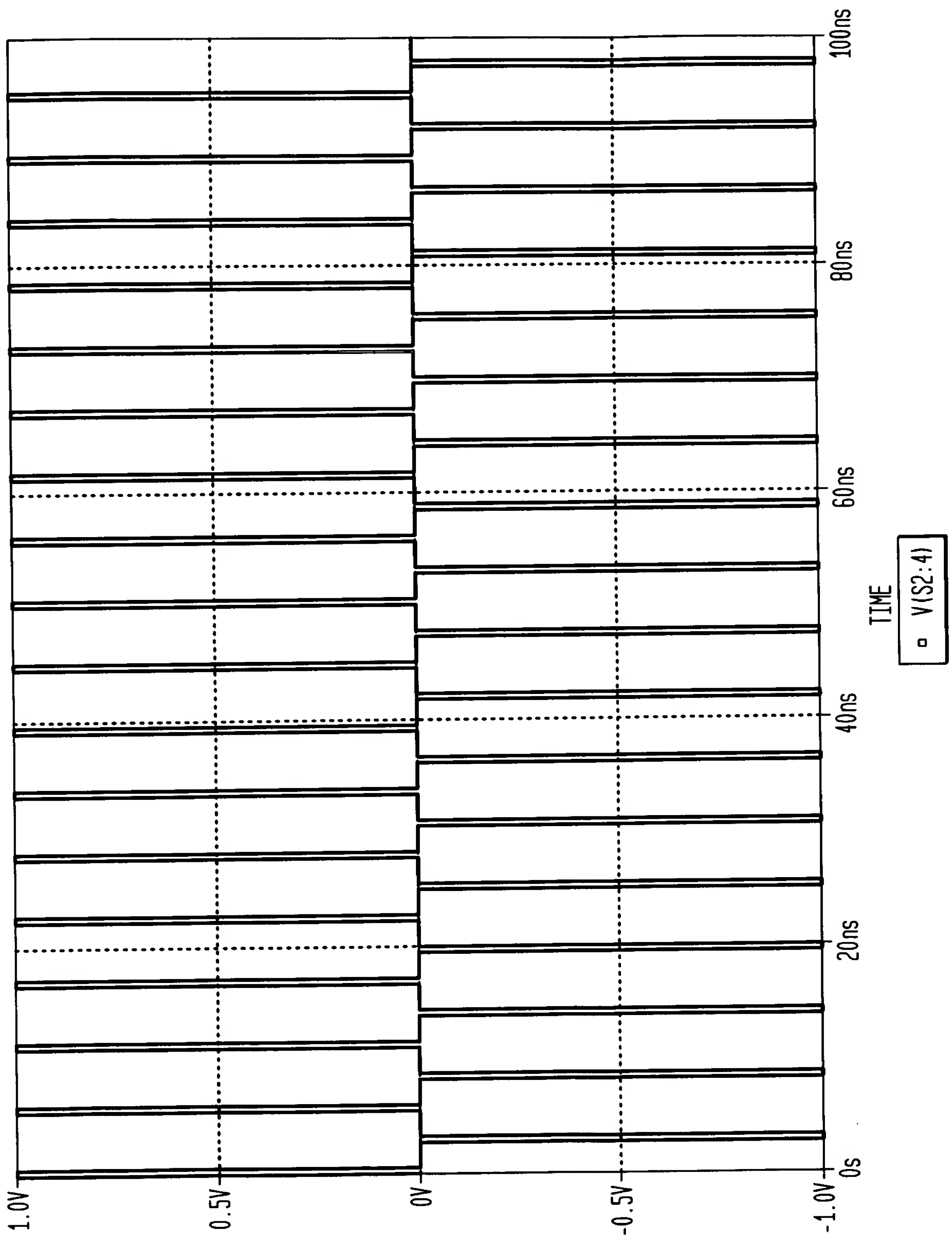

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FIG. 280

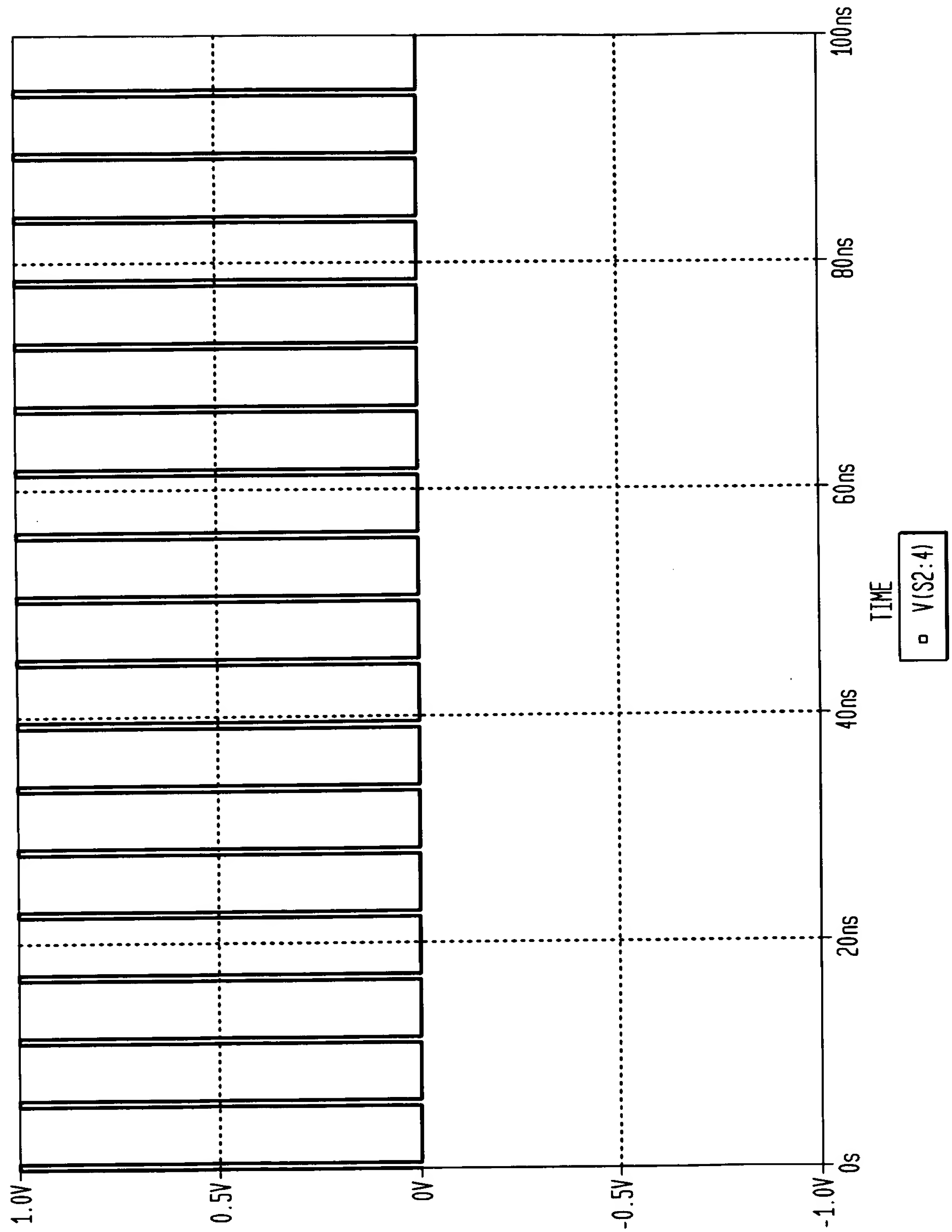

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FIG. 281

MULTIPLE APERTURE RECEIVER IMPLEMENTATION

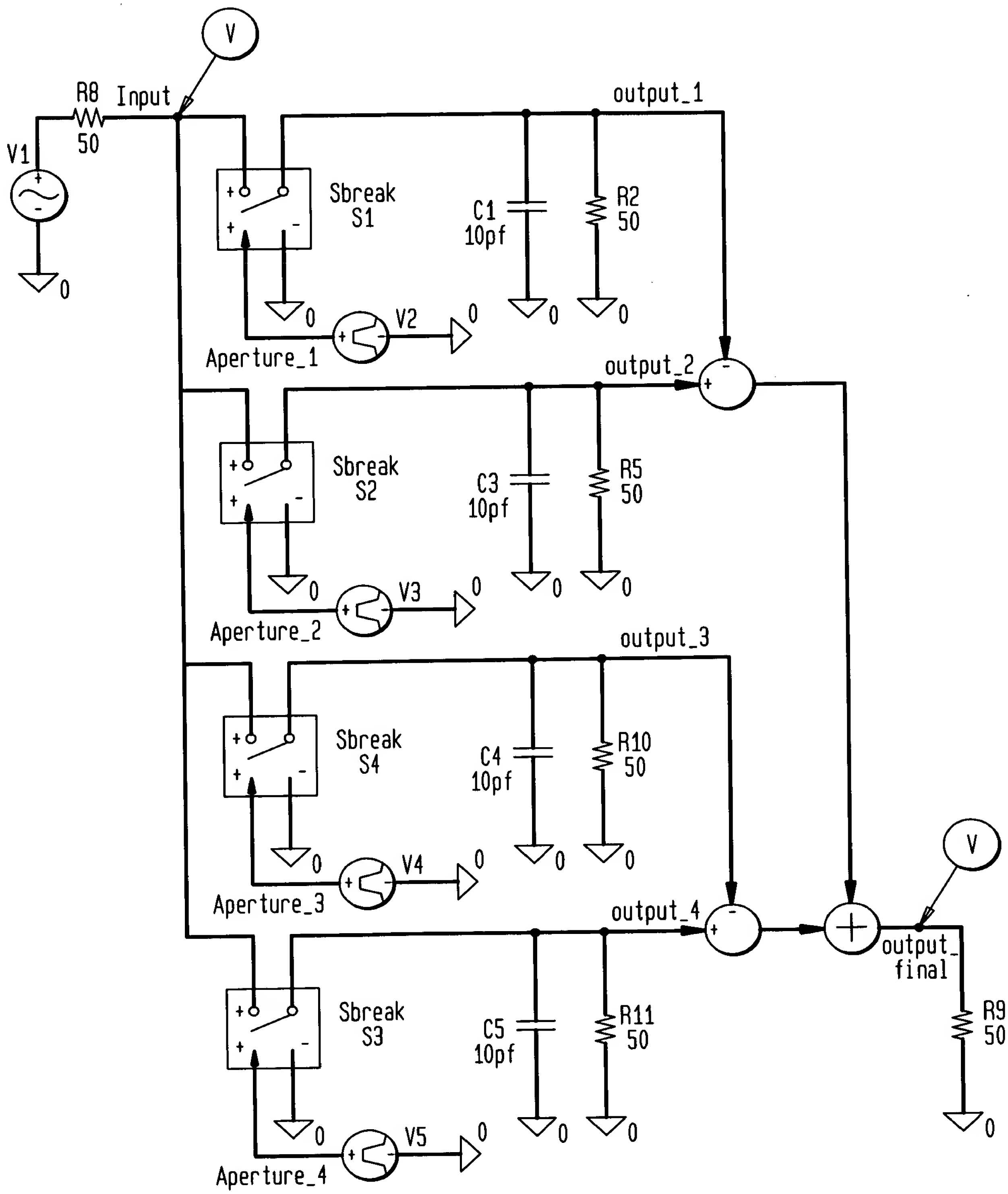

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FIG. 282

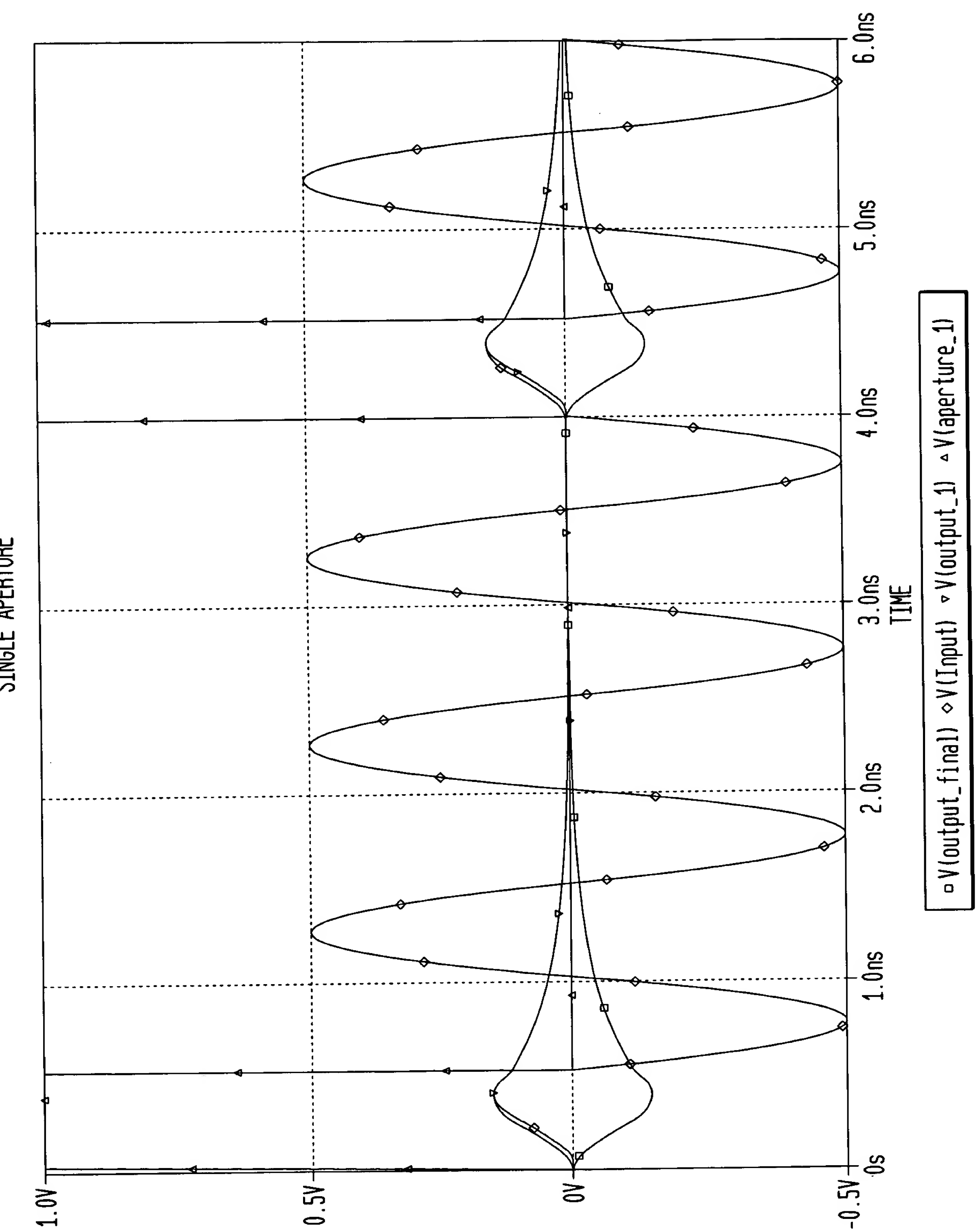

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FIG. 283

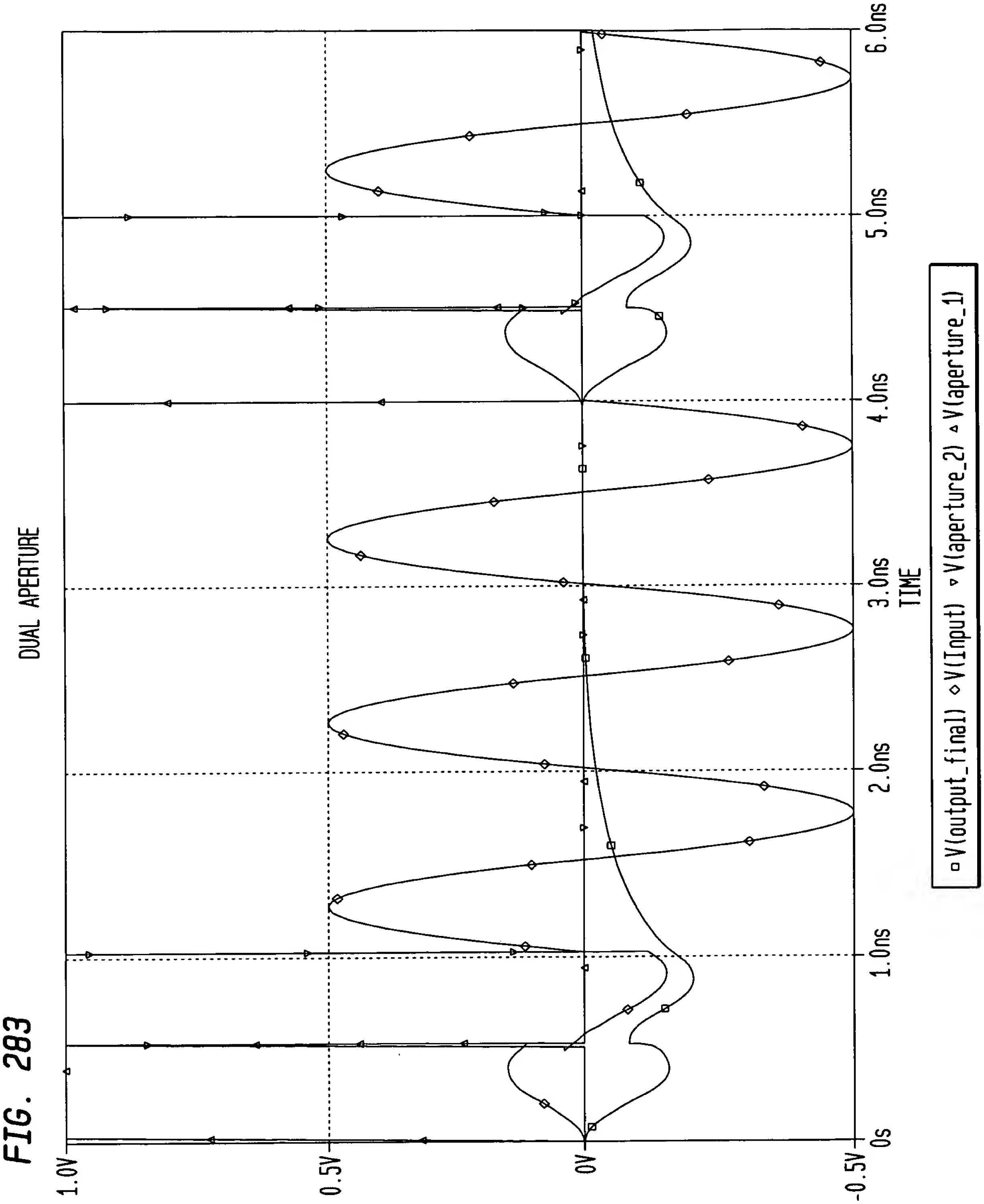

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FIG. 284

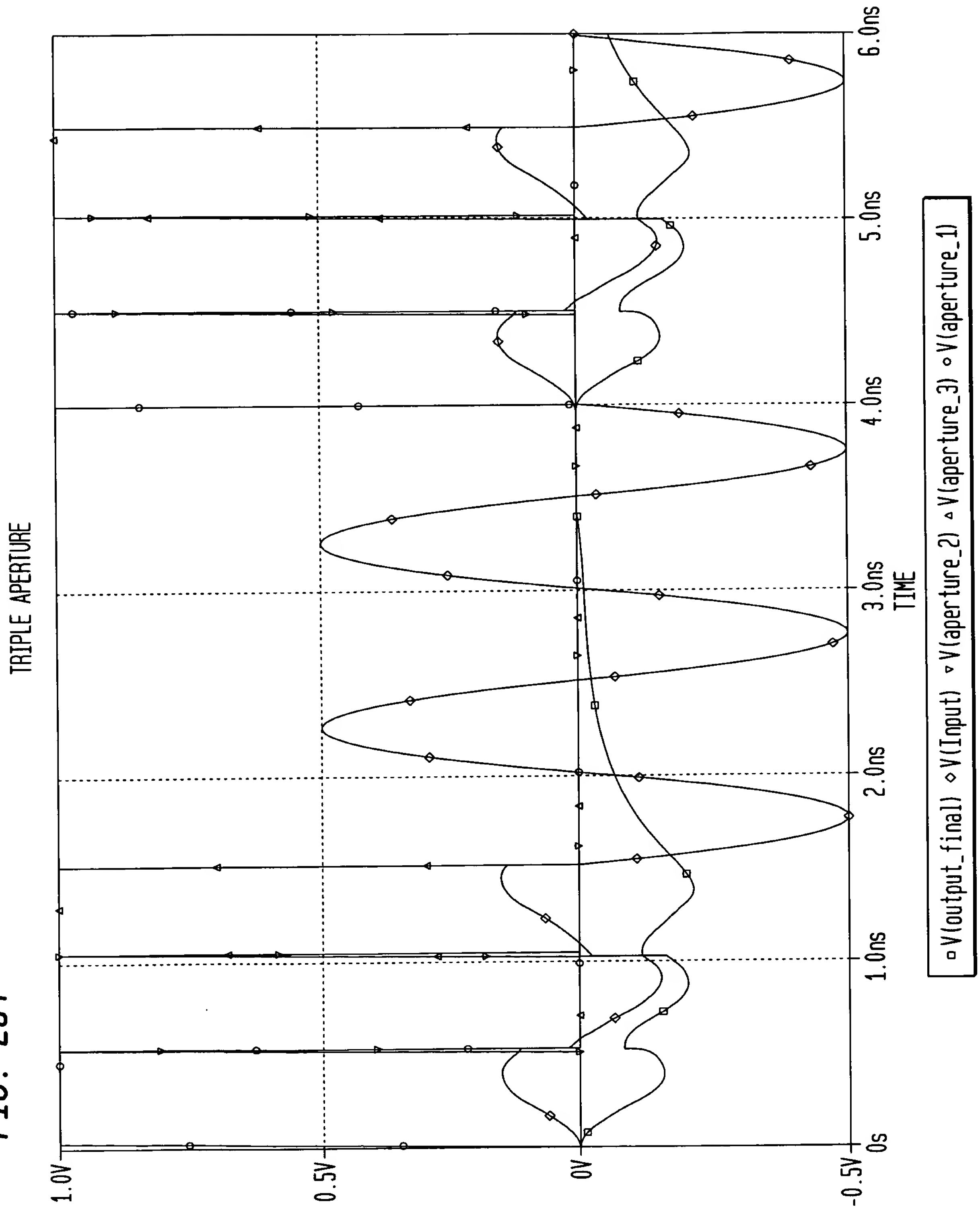

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FIG. 285

QUAD APERTURE